FRONTGRADE

DATASHEET

UT8MRQxG32

1Gbit, 2Gbit, 4Gbit, 8Gbit x 32 Parallel MRAM

5/16/2025

Version #:1.0.1

Features

- Interface
  - — Parallel Asynchronous x32
    - 45ns read/write cycle time
- True random access memory
- Technology
  - — 22nm pMTJ STT-MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: > 20 years @ 85°C (see Table 11)
- Density
  - — 1Gbit Organized as 33,554,432 x 32
  - — 2Gbit Organized as 67,108,864 x 32
  - — 4Gbit Organized as 134,217,728 x 32
  - — 8Gbit Organized as 268,435,456 x 32
- Operating Voltage Range
  - — VCC: 2.50V – 3.60V
  - — VCCIO: 1.8V, 2.5V, 3.0V, 3.3V
- Package Options:
  - — 142-ball FBGA (15mm x 17mm)
    - Moisture Sensitivity Level MSL 3
    - Available with leaded (63Sn 37Pb) balls
- Data Protection
  - — Low Voltage Write Inhibit
- Available in Frontgrade's Manufacturing Flow based on PEMS-INST-001 Level 1 and Level 2

Operational Environment

- Temperature Range: -40°C to +125°C*
- Total Dose: 100 krads(Si)
- SEL Immune: ≤ 60 MeV-cm^2/mg at 105°C and 3.0V
- SEU Immune: ≤ 83 MeV-cm^2/mg

Applications

- Reconfigurable computing image storage
- Ideal for applications needing low power, infinite endurance requiring the ability to store and retrieve data without incurring large latencies.

*All references to temperature herein are case temperature unless otherwise stated.

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Introduction

UT8MRQxG32 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in 1Gbit, 2Gbit, 4Gbit and 8Gbit density. MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings. Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution. Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C (see Table 11).

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, high endurance, high performance and scalable memory technology.

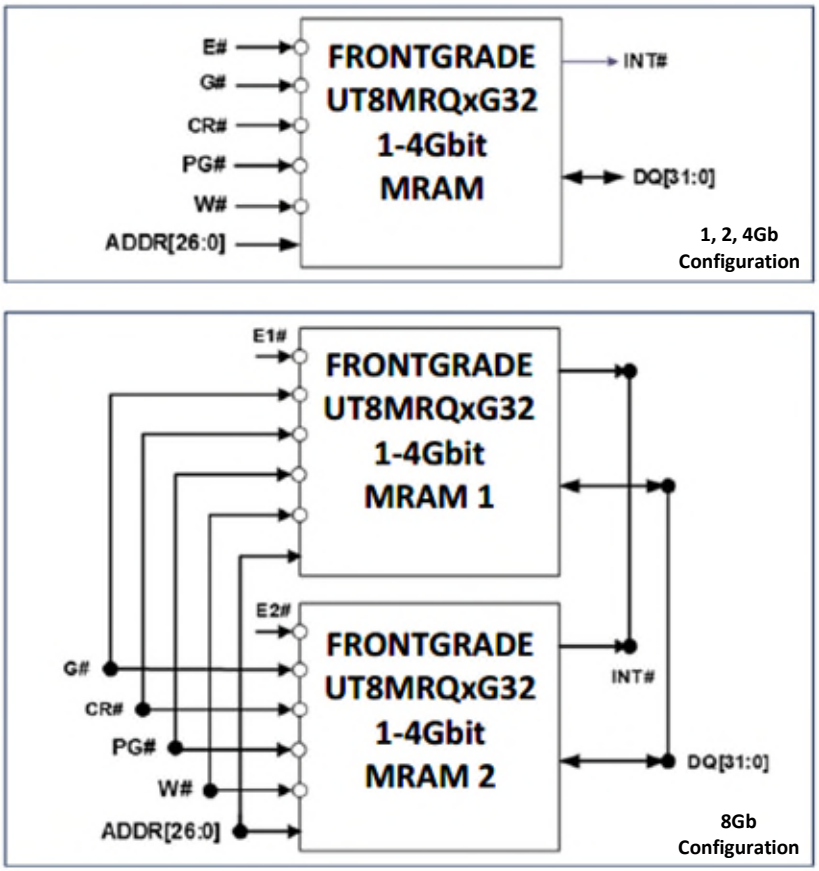


Figure 1: Simple Block Diagrams

General Description

UT8MRQxG32 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in 1Gbit, 2Gbit, 4Gbit and 8Gbit. MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings. Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution. Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, high endurance, high performance and scalable memory technology.

UT8MRQxG32 is available in small footprint (15mm x 17mm) 142 ball BGA package. In 1,2,4Gb densities the device uses one chip select E#. In this configuration one contiguous address space of 1,2,4Gb is formed. In 8Gb configuration the package has two banks of 4 dies each selectable separately and not at the same time. Each bank is selectable using either E1# and E2#. In the 8Gb configuration E1# and E2# MUST NOT be selected simultaneously as the two banks share the same I/O pins.

Architecture

UT8MRQxG32 is a high performance MRAM device. Writing to and reading from the device are performed as follows:

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[26]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[26]) to appear on I/O pins (DQ[0] to DQ[31])

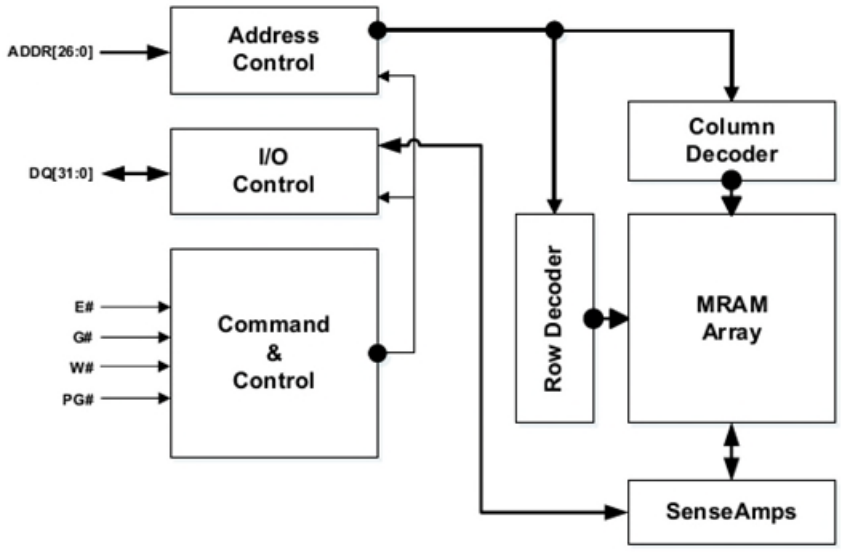


Figure 2: Functional Block Diagram

Table 2: Modes of Operation

Mode	E#	G#	W#	Current	DQ[31:0]
Not Selected	H	X	X	ISB	Hi-Z
Output Disabled	L	H	H	IREAD	Hi-Z
Read Word	L	L	H	IREAD	Data-out
Write Word	L	X	L	IWRITE	Data-in

Notes

H: High (Logic "1"), L: Low (Logic "0"), X: Don't Care, Hi-Z: High Impedance

Signal Description and Assignment

Table 3: Signal Description

Signal	Ball Assignment	Type	Description
E# / E1#	P8	Input	1,2,4Gb (E#) : Chip enable: Enables the MRAM array 8Gb (E1#) : Chip enable: Enables the 1st bank of 4 MRAM die. In this case, THIS SIGNAL MUST NOT BE ACTIVE AT THE SAME TIME AS E2#.
DNU / E2#	K5	DNU/Input	1,2,4Gb (DNU) : It can be left floating and not connected. There is an internal 10k Pullup. 8Gb (E2#) : Chip enable: Enables the second bank of 4 MRAM die. THIS SIGNAL MUST NOT BE ACTIVE AT THE SAME TIME AS E1#.
G#	P7	Input	Output enable: Enables the output drivers for data transfer I/Os.
CR#	J2	Input	Configuration Register enable: Enables access to the Configuration registers
PG#	K3	Input	Page Mode: Enables Page mode access
W#	M8	Input	Write enable: Transfers data from the host system to the MRAM when Low (Logic '0').Transfers data from the MRAM to the host system when High (Logic '1').
ADDR[26:0]	M2, L4, K13, M3, L3, M7, P12, L12, N11, N6, P6, L13, M13, P10, N10, M12, N13, L11, M11, P5, P3, N5, N4, M4, N2, N9, M9	Input	Address: I/Os for address transfer 1G: ADDR[24:0] – 25 Address pins for 1Gb x32 devices. [1] 2G: ADDR[25:0] – 26 Address pins for 2Gb x32 devices. [2] 4G: ADDR[26:0] – 27 Address pins for 4Gb x32 devices.
DQ[31:0]	E2, F2, D2, E3, E12, D10, C9, C7, G4, G3, F13, D13, C10, E8, F6, E5, E13, G11, E10, F9, C8, C6, D6, D4, G12, C12, D11, D9, E7, C5, D5, C3	Input / Output	Data inputs/outputs: The bidirectional I/Os transfer data [31:0].
INT# [3]	G13	Output	Interrupt: Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes low on error): requires to have an external pull-up resistor (4.7KΩ)
VCCIO	F12, J12, E11, M10, D8, N8, D7, N7, M5, E4, F3, J3	Supply	I/O power supply.
VSSIO	F10, L10, E9, L9, F8, L8, F7, L7, E6, L6, G5,	Supply	I/O ground supply.
VCC	C13, P13, D12, N12, C11, F11, H11, J11, K11, P11, C4, F4, H4, J4, K4, P4, D3, N3, C2, P2	Supply	Core power supply.
VSS	A14, B14, C14, H13,	Supply	Core ground supply.

Signal	Ball Assignment	Type	Description
	R14, T14, A13, T13, A12, G10, H10, J10, K10, F5, L5, A2, T2, A1, B1, R1, T1		
DNU	J13, H12, K12, P9, M6, H5, J5, H3, G2, H2, K2, L2		Do Not Use: DNUs must be left unconnected.

Notes:

1. Unused ADDR[26:25] balls should be connected to Ground
2. Unused ADDR[25] balls should be connected to Ground
3. INT# is latched and must be reset/cleared by writing to the ECC Control register. This signal is not valid during write operations.

Special Configuration Options

There are eight user accessible registers that control ECC, output drive strength and array write protection. All registers are 32-bit wide. These registers are only available during device configuration and not accessible to the user. In a multi-die configuration (2Gb, 4Gb, 8Gb) each 1Gb die has its own set of registers and need to be programmed individually. Each die needs to be selected using the upper 2 MSB address bits.

ECC Registers

There are 6 registers that allow access to the ECC engine during the life of the product to access the functionality of the circuits. During normal use, the ECC engine will correct any soft errors.

Int# Functionality

As explained in the pinout, the INT# will go active if uncorrectable error is encountered. This is an open collector output which requires a pullup. In a multi-chip configuration (2G, 4G, 8Gb) the pin is shared between the dies. The recommended next steps are up to the system architect. The host must interrogate each die to identify which one/ones caused the interrupt to clear the INT Flag register.

Table 4: ECC Control Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:2]	RSVD	Reserved	R	31'b0	Reserved for future use
[1]	Interrupt Reset	Resets the interrupt generated in response to detection of an unrecoverable error and clears the interrupt flag.	W		0: Don't reset 1: Reset ECC unrecoverable error interrupt
[0]	Error_Count_Reset	Resets the ECC Error Count Register	W	0	0: Don't reset 1: Reset ECC Error Count Register to zero

To prevent inadvertent INT# trigger, E# must remain high (inactive) except during read operations. INT# is only valid during read operations and cannot be sampled during Write operations.

The ECC control register must be reset/cleared before checking the INT# signal. To sample INT#, the following timing must be adhered.

INT# Timing During a Read Cycle

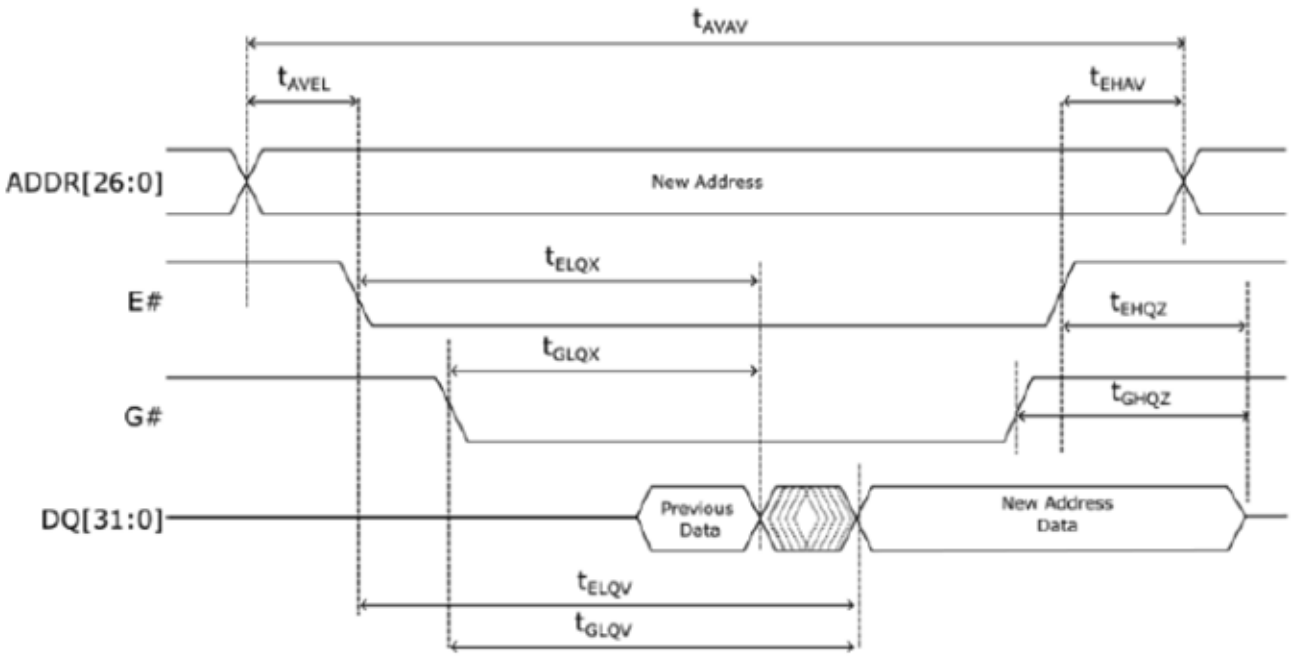


Figure 3: INT# Read Operation

Table 5: INT# Read Operation Timing

Parameter	Symbol	Minimum	Maximum	Units
Address Valid to Address Valid	tAVAV	45		ns
Address Hold to E# High	tEHAV	0		ns
Address Hold to E# Low	tAVEL	0		ns
Chip Enable Access Time	tELQV		45	ns
Output Enable Access Time	tGLQV		25	ns
Chip Enable Low to Output Active	tELQX	3		ns
Chip Enable Low to Output Hi-Z	tEHQZ	0	15	ns
Output Enable High to Output Hi-Z	tGHQZ	0	15	ns

Output Drive Strength Register

The default setting of this register is 00.

Table 6: Output Drive Strength Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options			
[31:3]	RSVD	Reserved	R	0	Reserved for future use			
[2]	Enable_ Drive_Strength	Enables or disables the drive strength setting	R/W	0	0: Default setting 1: Use output drive strength setting			
						1.8V	2.5V	3.3V
[1:0]	Output_Drive_ Strength_Setting	Output drive strength	R/W	00	00	1mA	2.5mA	4mA
					01	3mA	5mA	8mA
					10	5mA	10mA	14mA
					11	7mA	14mA	18mA

Device Protection Register

It is possible to write protect the Memory array as shown in the table below. Note; The term full array is defined as an array of 1Gb.

Table 7: Device Protection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:3]	RSVD	Reserved	R	29'b0	Reserved for future use
[2:0]	BPSEL[2:0]	Enables or disables block protection	R/W	3'b0	000 – Disabled 001 – Protect upper 1/64 array 010 – Protect upper 1/32 array 011 – Protect upper 1/16 array 100 – Protect upper 1/8 array 101 – Protect upper 1/4 array 110 – Protect upper 1/2 array 111 – Protect full array

Package Pinout

142-Ball FBGA – 1,2,4Gb

UT8MRQ1G32, UT8MRQ2G32, UT8MRQ4G32 (Balls Up, Bottom View)

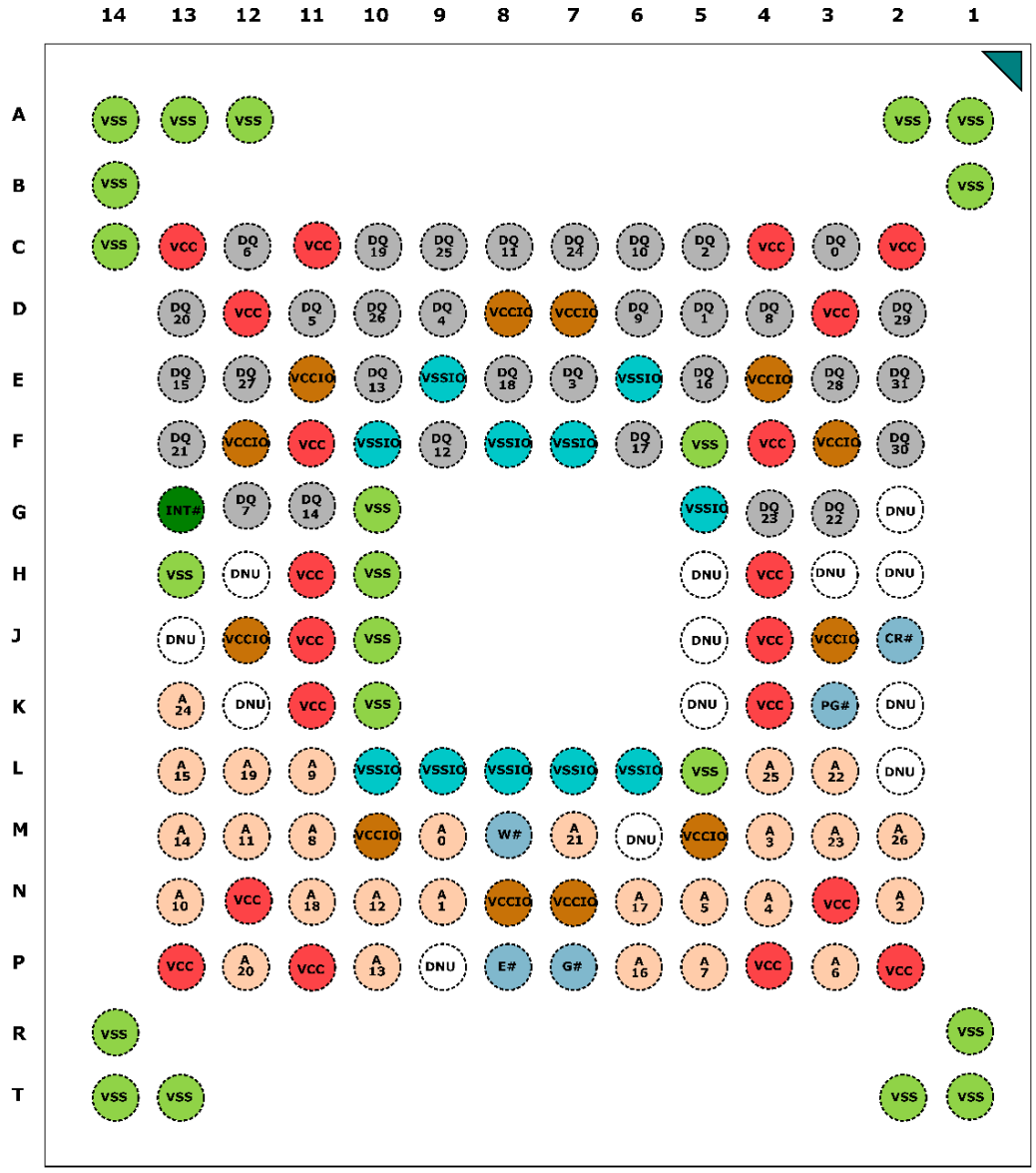


Figure 4: 142-Ball FBGA – 1,2,4Gbit

Package Pinout continued

142-Ball FBGA – 8Gb

UT8MRQ8G32 (Balls Up, Bottom View)

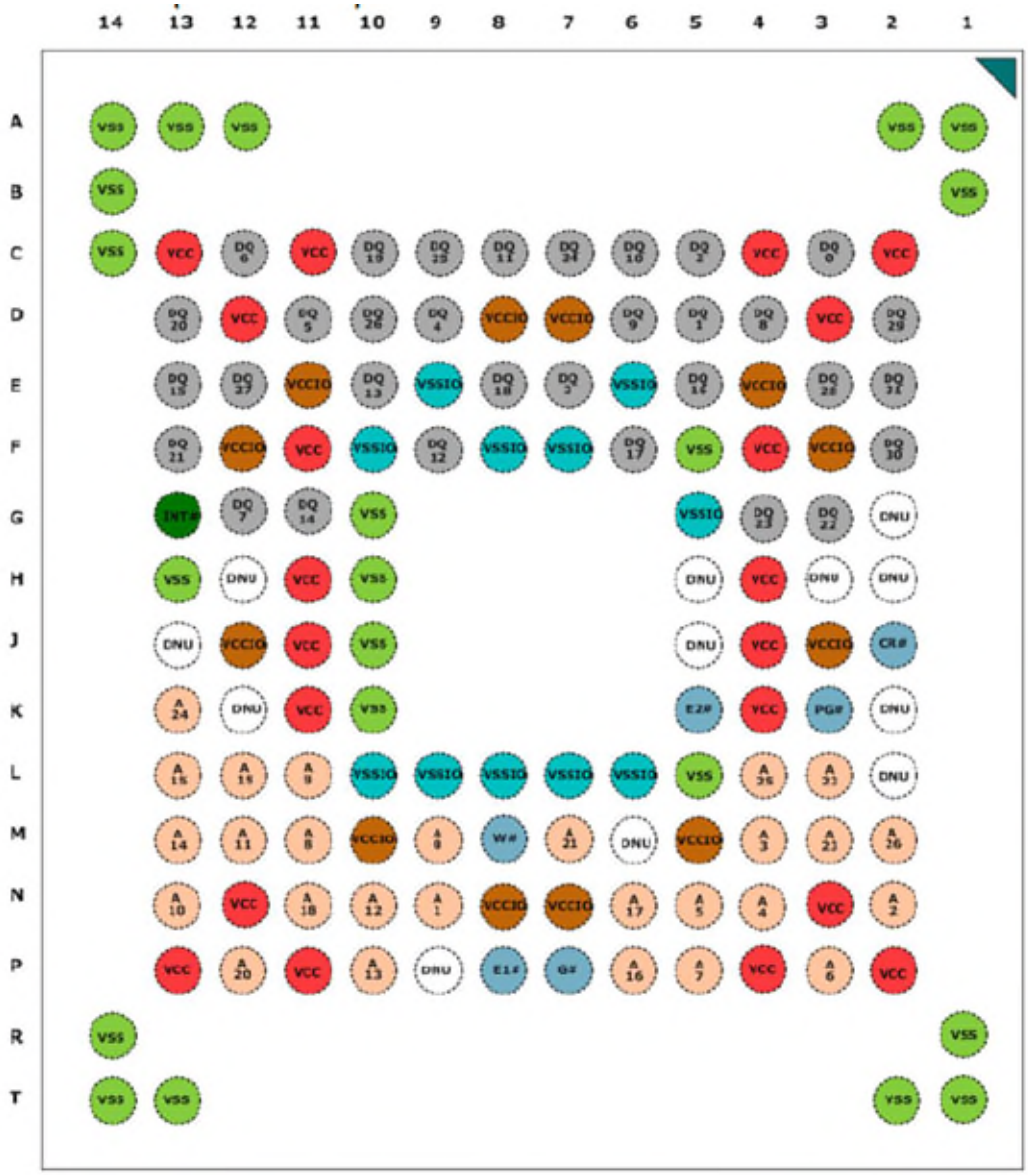


Figure 5: 142-ball FBGA – 8Gb

Normal Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- VCC and VCCIO can ramp up together (RVR), if not possible then VCC first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V before reaching the final value of VCCIO.
- The device must not be selected at power-up (a 10KΩ pull-up Resistor to VCCIO on E# is recommended). Then a further delay of tPU (Figure 5) until VCC reaches VCC(minimum) .
- During Power-up, recovering from power loss or brownout, a delay of tPU is required before normal operation commences (Figure 6).

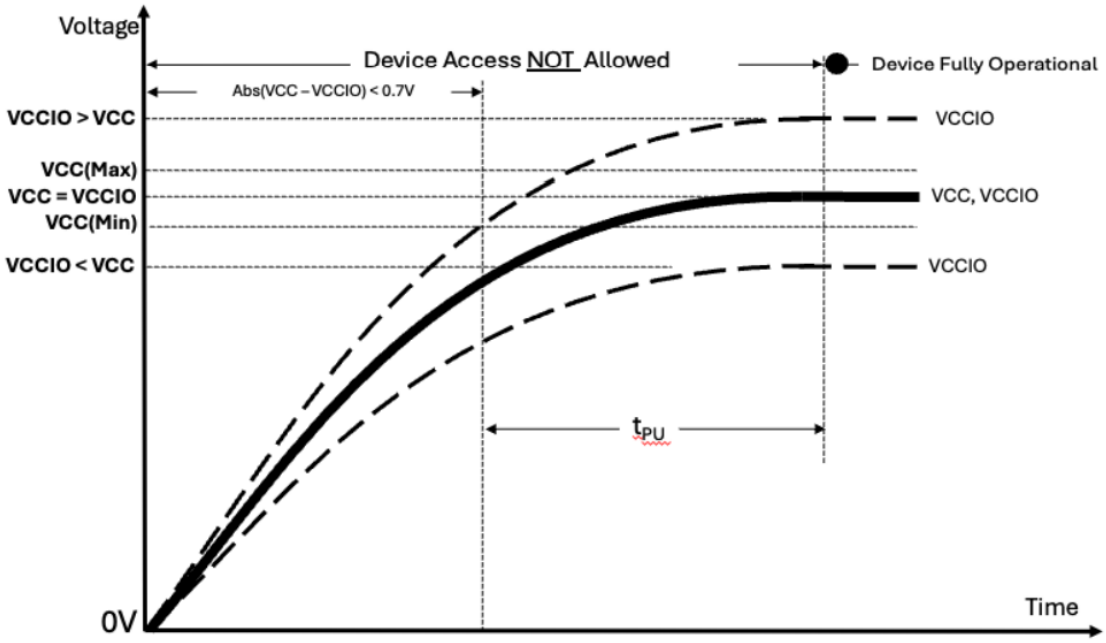


Figure 6: Power-Up Behavior

When powering down, the following procedure is required to turn off the device correctly:

- VCC and VCCIO can ramp down together (RVF), if not possible then VCC first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down (a 10KΩ pull-up Resistor to VCCIO on E# is recommended).
- It is recommended that no instructions are sent to the device when VCC is below VCC (minimum).
- During power loss or brownout, when VCC goes below VCC-CUTOFF. The voltage must drop below VCC(Reset) for a period of tPD. The power-up timing needs to be observed after VCC goes above VCC(minimum)

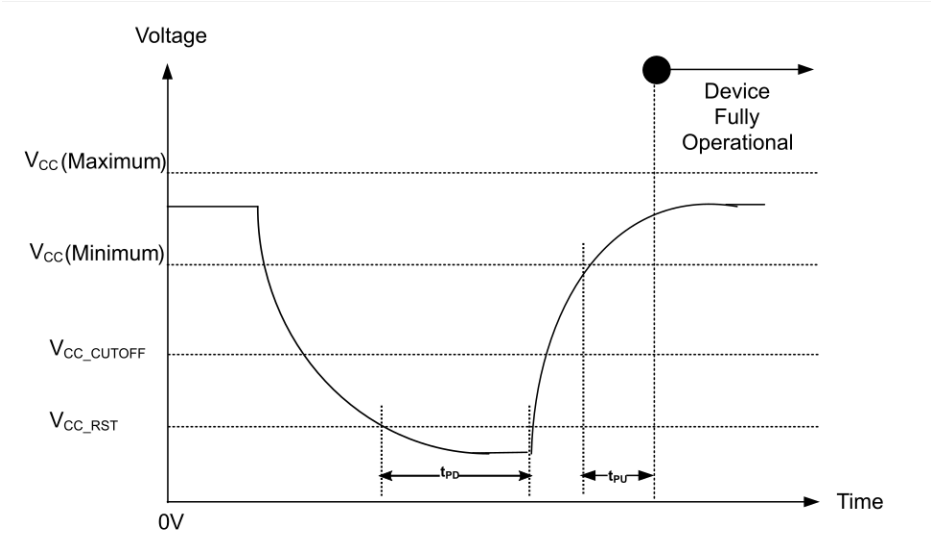


Figure 7: Power-Down Behavior

Table 8: Power Up/Down & Device Initialization Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
VCC Range		All operating voltages and temperatures	2.5	-	3.6	V
VCC Ramp Up Time	RVR		30	-	-	µs/V
VCC Ramp Down Time	RVF		20	-	-	µs/V
VCC Power Up to First Instruction	tPU		1	-	-	ms
VCC (low) time	tPD		1			ms
VCC Cutoff – Must Initialize Device	VCC_CUTOFF		1.6	-	-	V
VCC (Reset)	VCC_RST		0		0.3	V

Electrical Specifications

Table 9: Recommended Operating Conditions

	Parameter / Condition	Minimum	Typical	Maximum	Units
Normal Operation	Operating Temperature:	-40.0	-	125.0	°C
	VCC Supply Voltage	2.5	3.0	3.6	V
	VCCIO Supply Voltage	1.71	1.8 – 3.3	3.6	V
VSS Supply Voltage		0.0	0.0	0.0	V
VSSIO Supply Voltage		0.0	0.0	0.0	V
Vwi Write Inhibit Voltage		2.0	2.2	2.4	V

Table 10: Pin Capacitance

Parameter	Symbol	Test Conditions	Density	Maximum	Units
Input Pin Capacitance	CIN	TEMP = 25°C; f = 1 MHz; VIN = 0V	1Gb	10.0	pF
			2/4Gb	20.0	
			8Gb	40.0	
Input / Output Pin Capacitance	CINOUT	TEMP = 25°C; f = 1 MHz; VIN = 0V	1Gb	10.0	pF
			2/4Gb	20.0	
			8Gb	40.0	

Table 11: Endurance and Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	125°C	10	years
		105°C	10	
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Table 12: Operational Environment

Parameter	Conditions	Limit	Units
Total Dose	VCC & VCCIO = Max; Temperature = Room (~25°C)	100	krads(Si)
SEL Onset LET	VCC = VCCIO = 3.6V; Temperature = 105°C	>40	MeV-cm^2/mg
	VCC = VCCIO = 3.0V; Temperature = 105°C	>60	MeV-cm^2/mg
	VCC = VCCIO = 2.7V; Temperature = 105°C	>75	MeV-cm^2/mg
SEU Onset LET	VCC = VCCIO = 2.5V; Temperature = Room (~25°C)	>83	MeV-cm^2/mg
SEFI Onset LET [1]	VCC = VCCIO = 2.5V; Temperature = Room (~25°C)	>83	MeV-cm2/mg

Note

1. No SEFI's were observed during dynamic testing under test conditions VCC = VCCIO = 2.5V; Temperature = Room (~25°C) which is generally considered the worst case SEFI/SET/SEU corner. However some SEFI like anomalies at high temperature were observed during SEL testing and are described in the radiation report.

Table 13: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	Hmax_write	24000	A/m
Magnetic Field During Read	Hmax_read	24000	A/m

Table 14: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Temperature Under Bias (Junction Temperature)	---	150	°C
Storage Temperature	-55 to 150		°C
Supply Voltage VCC	-0.5	4.0	V
I/O Voltage VCCIO	-0.5	3.8	V
Voltage on any pin except VDD	-0.5	VCCIO + 0.2	V
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test)	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Notes:

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 15: DC Characteristics

Parameter	Symbol	Test Conditions	Density	3.0V Device (2.5V-3.6V)				
				Min	Typical [1]	85°C [2]	Max [3]	Units
Read Current	IREAD	VCC (max), IOUT=0mA	1Gb[4]		25	50	112	mA
			2Gb[4]		50	100	210	
			4Gb		70	200	420	
			8Gb[4]		140	400	840	
Write Current	IWRITE	VCC (max)	1Gb[4]		20	50	112	
			2Gb[4]		50	100	210	
			4Gb		65	200	420	
			8Gb[4]		130	400	840	
Standby Current (-40°C to +125°C)	I_{SB}	E# = V_{IH} VCC (max)	1Gb[4]		25	50	106	
			2Gb[4]		45	100	200	
			4Gb		60	180	400	
			8Gb[4]		120	360	800	
Input Leakage Current	ILI	VIN=0 to VCC (max)					±1.0	µA
Output Leakage Current	ILO	VOUT=0 to VCC (max)					±1.0	µA
Input High Voltage (VCCIO=1.71-2.2)	VIH			0.65* VCCIO			VCCIO +0.2	V
Input High Voltage (VCCIO=2.2-2.7)				1.8				
Input High Voltage (VCCIO=2.7-3.6)				2.2				
Input Low Voltage (VCCIO=1.71-2.2)	VIL			-0.2			0.35* VCCIO	V
Input Low Voltage (VCCIO=2.2-2.7)							0.7	
Input Low Voltage (VCCIO=2.7-3.6)							0.8	
Output Low Voltage (VCCIO=1.71-2.2)	VOL	IOL = 0.1mA					0.2	V
Output Low Voltage (VCCIO=2.2-2.7)		IOL = 0.1mA					0.4	
Output Low Voltage (VCCIO=2.7-3.6)		IOL = 2.0mA					0.4	
Output High Voltage (VCCIO=1.71-2.2)	VOH	IOH = -0.1mA		1.4				V
Output High Voltage (VCCIO=2.2-2.7)		IOH = -0.1mA		2.0				
Output High Voltage (VCCIO=2.7-3.6)		IOH = -1.0mA		2.4				

Notes:

1. Typical values are measured at 25°C
2. 85°C (junction temperature) values are guaranteed by characterization; not tested in production
3. Max values are measured at 125°C (case temperature)
4. **1/2/8 Gb densities are in qualification. Electrical limits subject to change.**

Table 16: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to VCC
Input rise and fall times	5ns
Input and output measurement timing levels	VCC/2
Output Load	CL = 30pF

Write Operation

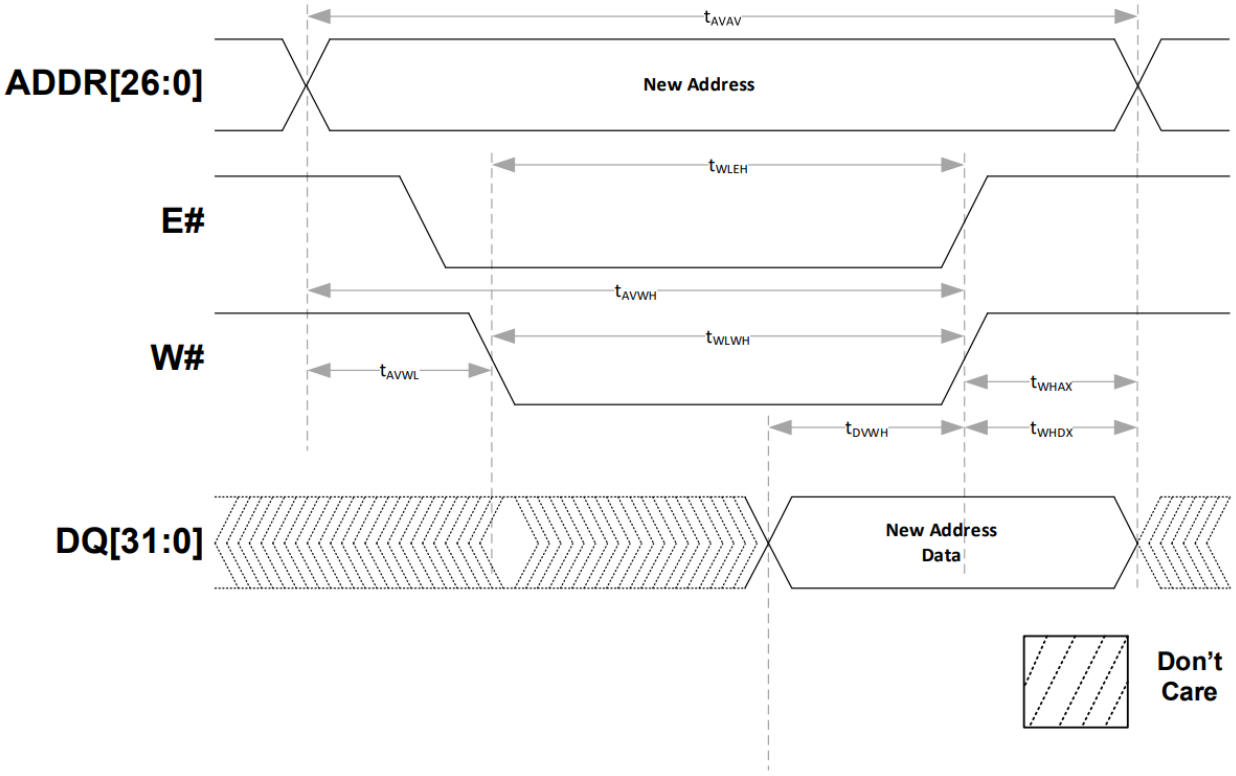


Figure 8: Write Operation (#WE Controlled)

Table 17: Write Operation (#WE Controlled)

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	tAVAV	45	-	ns
Address Set-Up Time	tAVWL	0	-	ns
Address Valid to end of Write (G# High)	tAVWH	28	-	ns
Address Valid to end of Write (G# Low)	tAVWH	30	-	ns
Write Pulse Width (G# High)	tWLWH, tWLEH	25	-	ns
Write Pulse Width (G# Low)	tWLWH, tWLEH	25	-	ns
Data Valid to end of Write	tDVWH	15	-	ns
Data Hold Time	tWHDX	0	-	ns
Write recovery Time	tWHAX	12	-	ns

Notes:

1. G# is High (Logic '1') for Write operation
2. Power supplies must be stable
3. Addresses valid either before or at the same time as E# goes low
4. In case of the 8G device: E# is represented by E1# or E2#

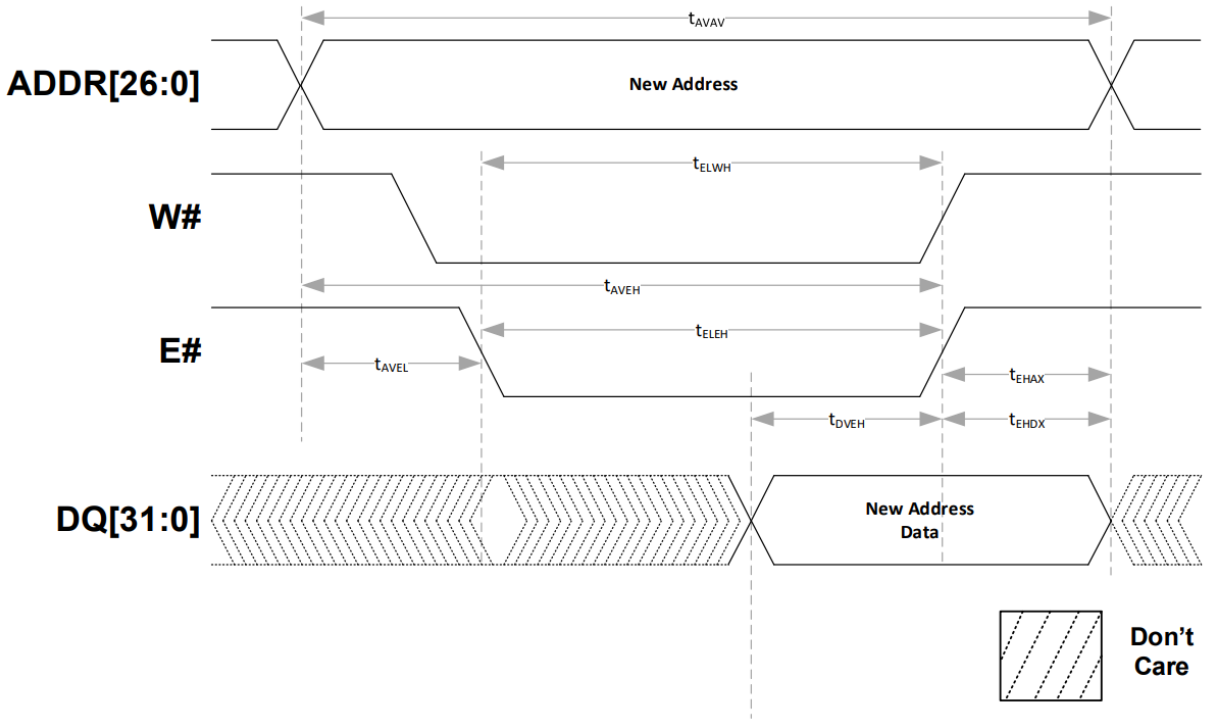


Figure 9: Write Operation (#E Controlled)

Table 18: Write Operation (#E Controlled)

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	tAVAV	45	-	ns
Address Set-Up Time	tAVEL	0	-	ns
Address Valid to end of Write (G# High)	tAVEH	28	-	ns
Address Valid to end of Write (G# Low)	tAVEH	30	-	ns
Write Pulse Width (G# High)	tELWH, tELEH	25	-	ns
Write Pulse Width (G# Low)	tELWH, tELEH	25	-	ns
Data Valid to end of Write	tDVEH	15	-	ns
Data Hold Time	tEHDX	0	-	ns
Write recovery Time	tEHAX	12	-	ns

Notes:

1. G# is High (Logic ‘1’) for Write operation
2. Power supplies must be stable
3. Addresses valid either before or at the same time as W# goes low
4. In case of the 8G device: E# is represented by E1# or E2#

Bus Turnaround Operation – Read To Write

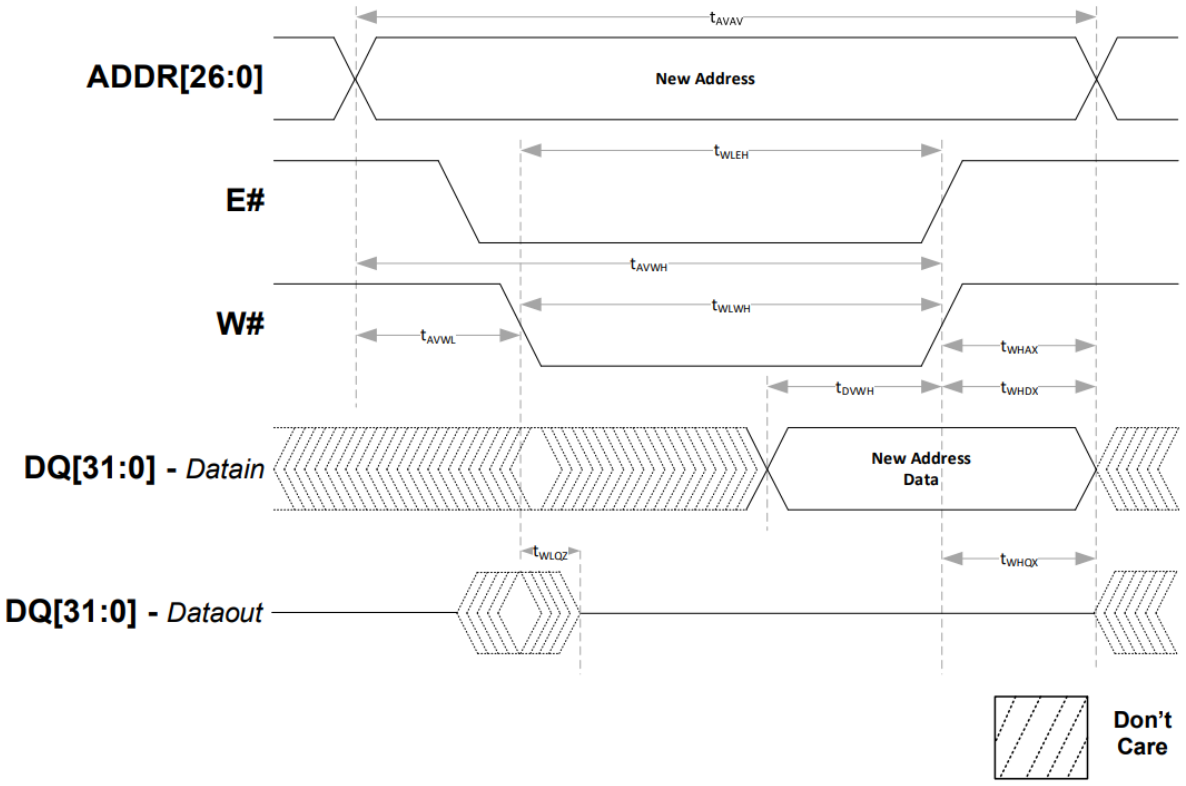


Figure 10: Bus Turnaround Operation

Table 19: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
W# Low to Data Hi-Z	tWLQZ	0	15	ns
W# High to Output Active	tWHQX	3	-	ns

Notes:

1. Power supplies must be stable
2. Addresses valid either before or at the same time as E# goes low
3. In case of the 8G device: E# is represented by E1# or E2#

Read Operation

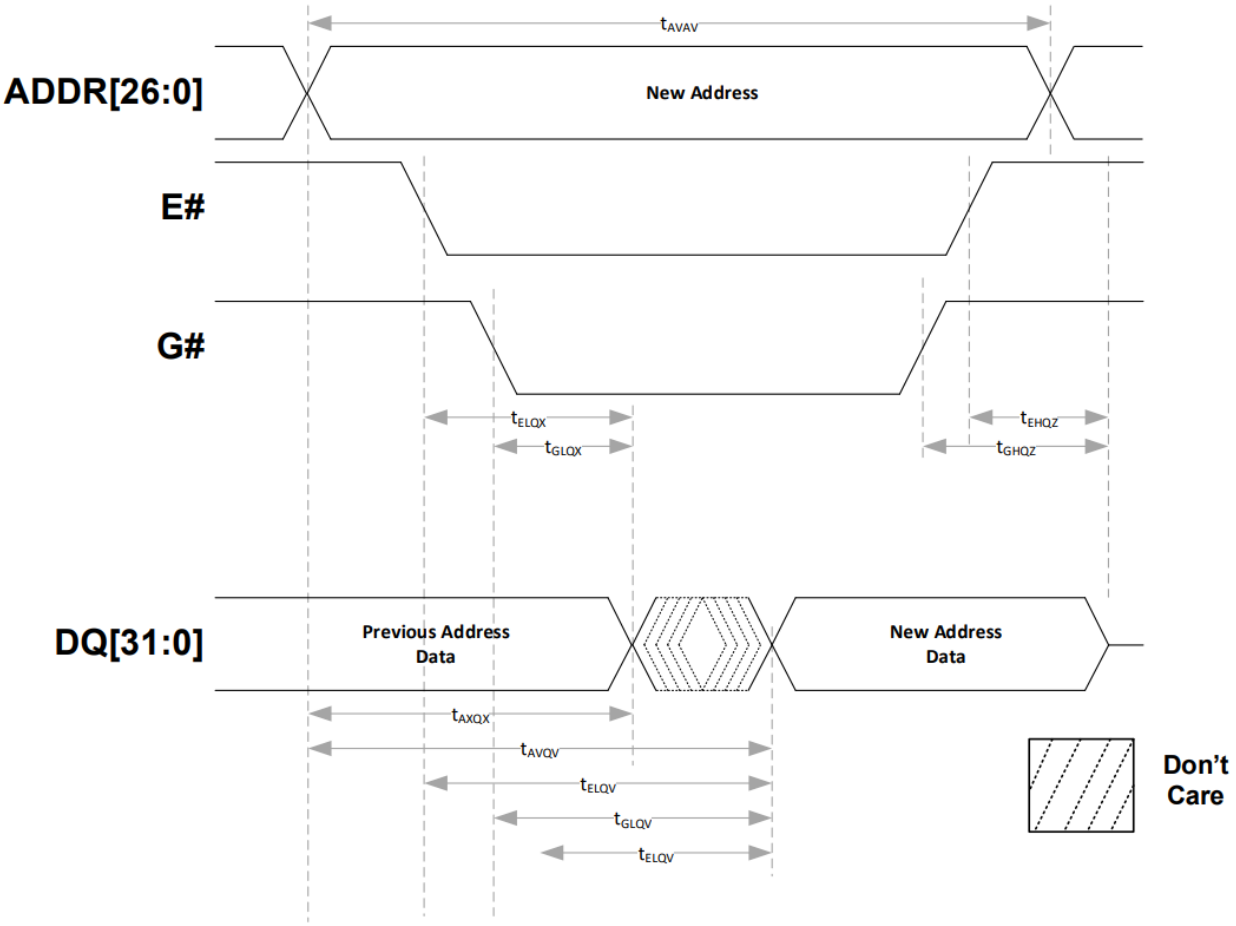


Figure 11: Read Operation

Table 20: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	tAVAV	45	-	ns
Address Cycle Time	tAVQV	-	45	ns
Chip Enable Access Time	tELQV	-	45	ns
Output Enable Access Time	tGLQV	-	25	ns
Output Hold from Address Change	tAXQX	3	-	ns
Chip Enable Low to Output Active	tELQX	3	-	ns
Output Enable Low to Output Active	tGLQX	0	-	ns
Chip Enable High to Output Hi-Z	tEHQZ	0	15	ns
Output Enable High to Output Hi-Z	tGHQZ	0	15	ns

Notes:

1. W# is High (Logic ‘1’) for Read operation
2. Power supplies must be stable
3. Addresses valid either before or at the same time as E# goes low
4. In case of the 8G device: E# is represented by E1# or E2#

Asynchronous Page Mode

Asynchronous page mode is an extension of the legacy asynchronous read and write operations that improves the performance of the MRAM memory, as shown in Figure 8. On power up or reset, the MRAM memory defaults to legacy asynchronous mode to enable controllers to immediately access the memory. Page mode is also immediately available after asserting PG# low and E# high. No special commands or setup are necessary.

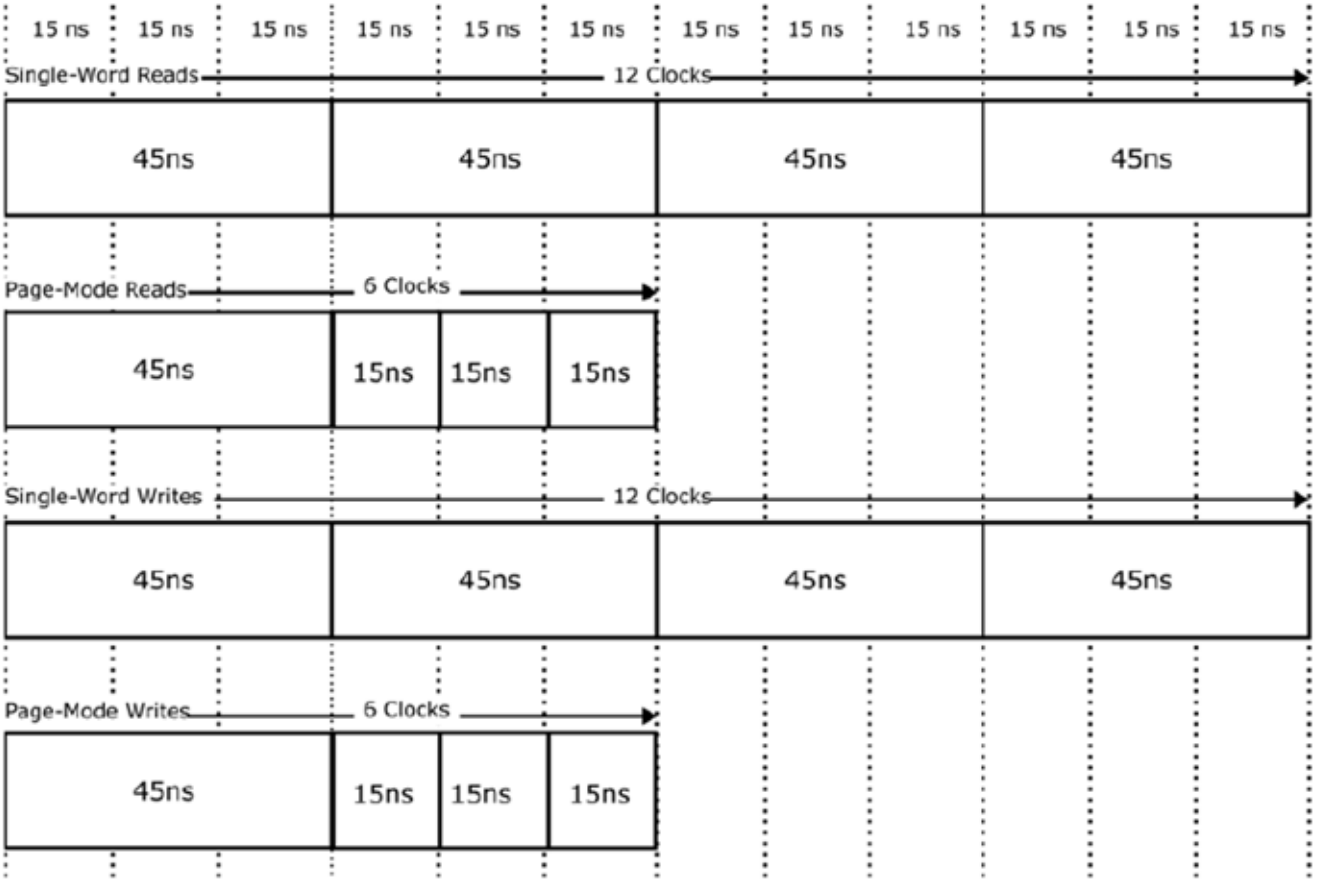


Figure 12: 4-Word Asynchronous Page Mode Comparison with Legacy Asynchronous Mode

Figure 12 shows the page mode functional block diagram. During a page write, a new page is accessed by changing any of the upper addresses A[max:2]. A subsequent write commands (W# toggle) can load the data buffers with new data to be written to any of the adjacent addresses A[1:0]. During page read, an initial asynchronous read access if executed during which 4 data words are read from the memory array simultaneously, and loaded into an internal page buffer, while the first data word is output onto the memory bus. Subsequent reads are output from the data buffer, providing up to two times the read and write access speed of conventional asynchronous reads.

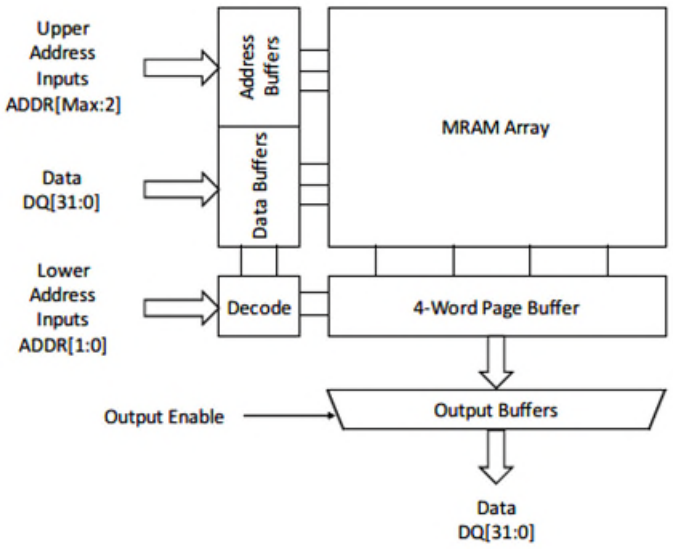
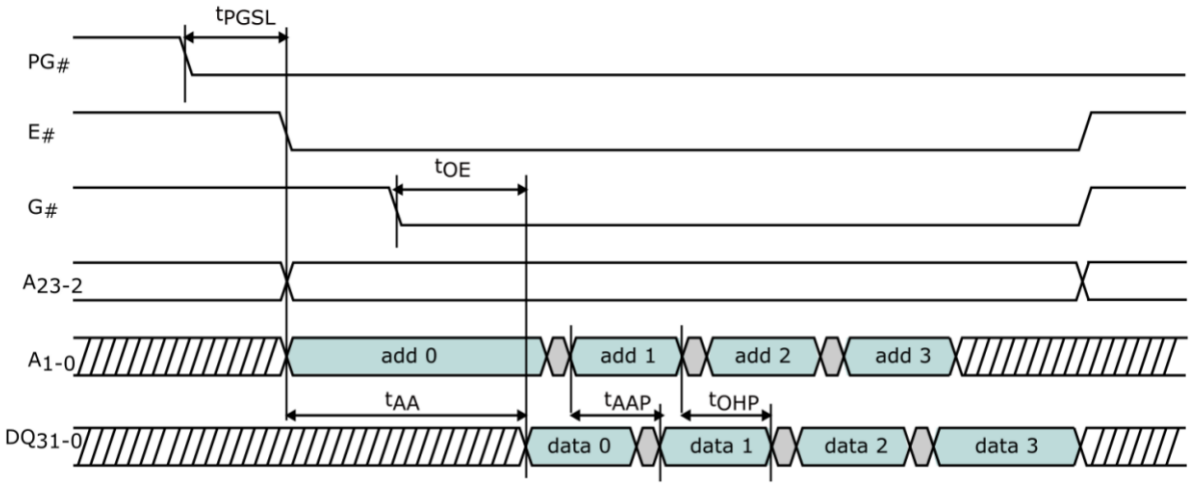


Figure 13: Page Mode Functional Block Diagram

Asynchronous Page Mode Read Operation

Asynchronous page mode reads are initiated by the memory controller in the same way as asynchronous single-word reads by asserting E# or changing any of the upper addresses A[max:2]. In Figure 13; an address is placed on the address bus, and E# and G# are asserted. Multiple data words are “sensed” simultaneously, and loaded into an internal page buffer while the first data word is being output onto the data bus. After the initial-access delay (tAA), read data is driven onto the data bus and then sampled by the memory controller. When the next read address is within the page-buffer range A[1:0], subsequent data is output from the page buffer, not from the MRAM array. A shorter access delay (tAAP) occurs when data is read from the page buffer. The low-order address bits are used to access the page buffer, and determine which word is output. Four-word page access uses A[1:0];



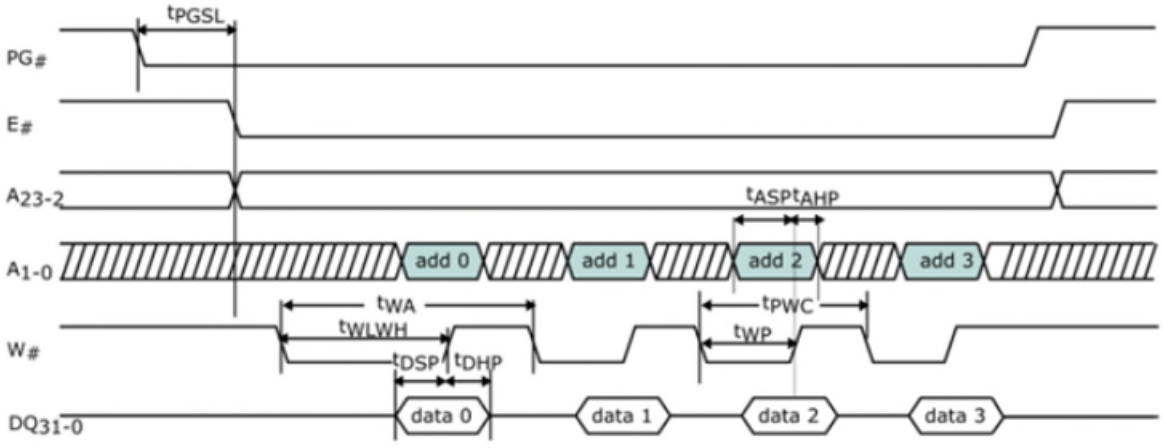
Notes:

In case of 8Gb device: E# is represented by E1# or E2#

Figure 14: Asynchronous Page Read Operation

Asynchronous Page Mode Write Operation

For Asynchronous page mode write, shown in Figure 14, the first write pulse defines the first write access (tPWC). While E# is maintained LOW, a subsequent write pulse along with a new adjacent address A[1:0] executes a page mode write access. E# must be LOW upon completion of a page write access. Asserting E# HIGH at the beginning or the middle of a page access will abort it.



Notes:

In case of 8Gb device: E# is represented by E1# or E2#

Figure 15: Asynchronous Page Write Operation

Asynchronous Page Mode Write To Single Write

On power up or reset, the MRAM memory defaults to the legacy asynchronous mode. The page mode is immediately available after asserting PG# low while maintaining E# HIGH for tPGSL. Returning to legacy mode can be achieved by asserting PG# HIGH and E# for tPGSH.

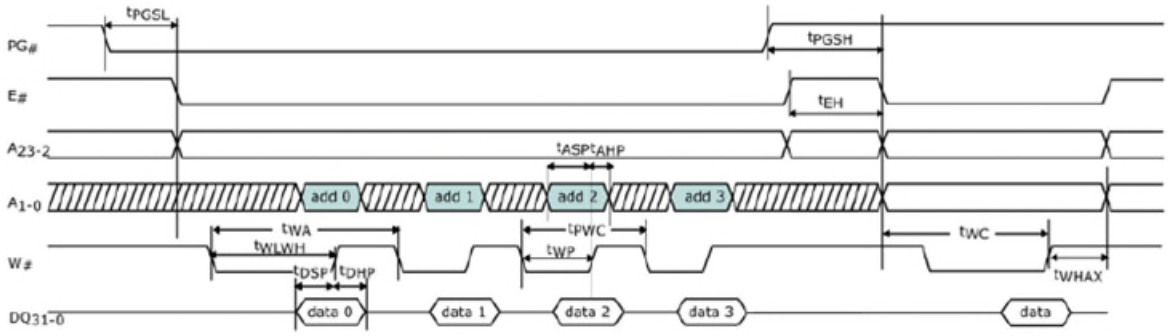


Figure 16: Page Write to Single Write Timing Diagram

Notes:

1. In case of the 8G device: E# is represented by E1# or E2#

Asynchronous Page Mode Ac Timing

Table 21: Page Mode AC Timing

Parameters	Description	Min	Max	Unit
tWA	Write access time	45	-	ns
tWC	Chip enable LOW to write enable HIGH	30	-	ns
tWHAX	Write recovery time	15	-	ns
tWLWH	Write enable low time	25	-	ns
tAS	Address setup time (to E# Low)	0	-	ns
tE	Chip enable access time	-	45	ns
tAA	Address access time	-	45	ns
tOE	Output enable access time	-	15	ns
tPWC	Page mode write access	15		ns
tWP	Page mode write enable low time	7.5		ns
tWPH	Page mode write enable high time	7.5		ns
tAHP	Page mode address hold time (to W# High)	6		ns
tASP	Page mode address setup time (to W# High)	7.5		ns

Parameters	Description	Min	Max	Unit
tAAP	Page mode address access time	-	15	ns
tOHP	Page mode output hold time	5	-	ns
tPGSL	Page mode select to E# Low	10	-	ns
tPGSH	Page mode unselect to E# Low	10	-	ns
tPGH	Page mode high time	45	-	ns
tEH	E# High time	10	-	ns
tOH	Output hold time	5	-	ns
tEP	Page mode E# low time	45	-	ns
tDSP	Page mode data setup time (to W# High)	7.5	-	ns
tDHP	Page mode data hold time (to W# High)	6	-	ns

Thermal Resistance

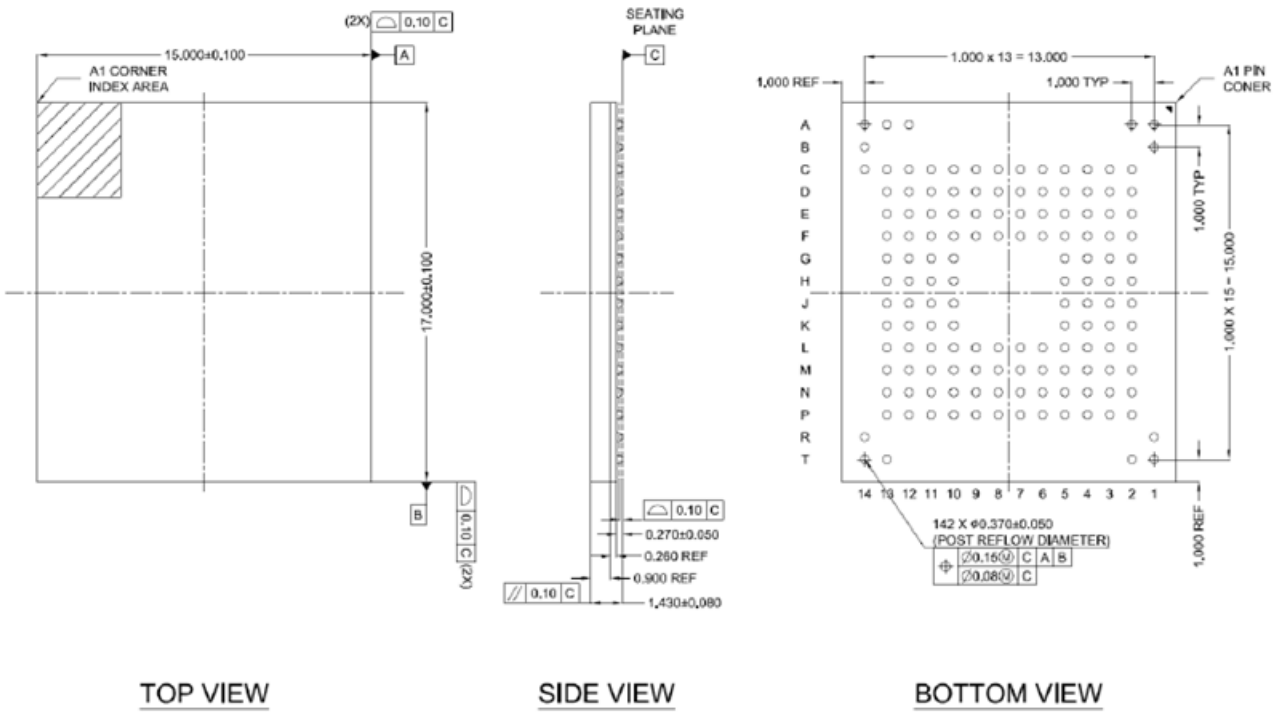
Table 22: Thermal Resistance Specifications 142 Ball BGA

Parameter	Description	Test Condition	1Gb	2Gb	4Gb	8Gb	Units
θJA	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	TBD	17.90	TBD	°C/W
θJC	Thermal resistance (junction to case)		2.10	TBD	2.19	TBD	°C/W

Notes:

1. These parameters are guaranteed by characterization, not tested in production
2. Ambient temperature , TA+ 25°C
3. Worst case junction temperature specified for top die (θJA) and bottom die (θJC)

Package Drawing 1, 2, 4Gb



TOP VIEW SIDE VIEW BOTTOM VIEW

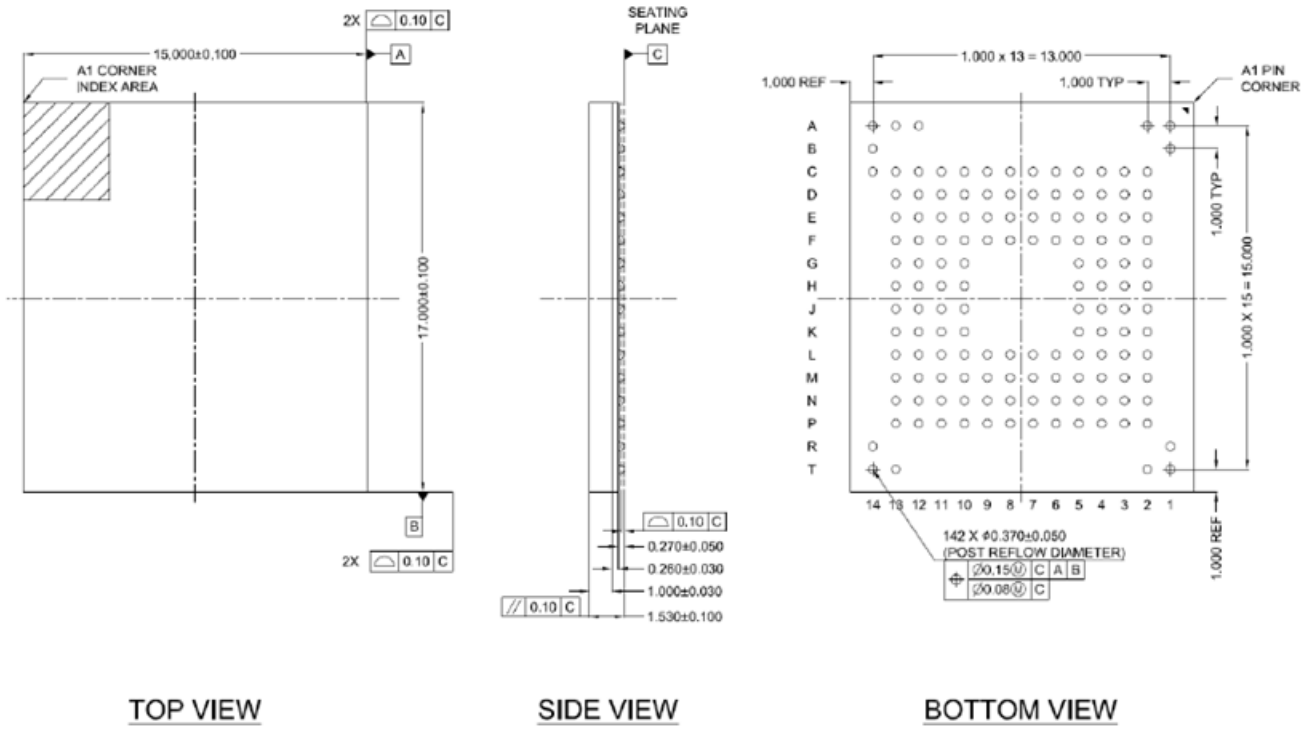
Notes

1. Dimensions given in mm
2. Solder Ball Size Is
   0.35 mm before reflow
   0.37 (±0.05) mm post reflow

3. Solder Resist Opening Is
   0.300 mm

Figure 17: 142-ball FBGA Package Dimensions 1, 2, 4Gb

Package Drawing 8Gb



Notes

1. Dimensions given in mm
2. Solder Ball Size Is
   0.35 mm before reflow
   0.37 (±0.05) mm post reflow
3. Solder Resist Opening Is
   0.300 mm

Figure 18: 142-ball FBGA Package Dimensions 8Gb

Ordering Information

Frontgrade Part Numbering Ordering Information

UTxxxx **** * * ** *

Lead Finish: Solder Ball Composition (Notes: 1)
(H) = Leaded (63Sn 37Pb)
(G) = Unleaded (SAC305)

Screening Level: (Notes: 2, 3)
(X1) = Space PEM L1 (Temperature Range: -40°C to +125°C) (Qualification at this screening level is in progress. Please contact the factory for further information)
(X2) = Space PEM L2 (Temperature Range: -40°C to +125°C)

Radiation Assurance:
(-) = No Radiation Assurance
(L) = 5E4 (50 krad (Si))
(R) = 1E5 (100 krad (Si))

Case Outline:
(B) = 142-Plastic Ball Grid Array (1mm Pitch)

Device Type:
(1G32) = 1Gbit MRAM 32bit parallel bus width (Qualification of this density is in progress. Please contact the factory for further information)
(2G32) = 2Gbit MRAM 32bit parallel bus width (Qualification of this density is in progress. Please contact the factory for further information)
(4G32) = 4Gbit MRAM 32bit parallel bus width
(8G32) = 8Gbit MRAM 32bit parallel bus width (Qualification of this density is in progress. Please contact the factory for further information)

8MRQ = MRAM

Notes:

1. Lead finish (G or H) must be specified.
2. Space PEM L1 and L2 per Frontgrade Manufacturing Flows Document. Based on NASA PEM-INST-001 Level 1 and 2 criteria.
3. Radiation assurance levels may be selected for Space PEM L1 and L2 orders.

Revision History

Date	Revision #	Author	Change Description	Page #
2/26/2024	1.0.0	PBN	Initial released of final datasheet version	
5/16/2025	1.0.1	MJL	Updated INT# operation guidelines. Added Unleaded solder option to ordering page. Added units to package dwg. DS reflects changes to manufacturer rev Z3 (4/8/2025). Added MSL3 to features.	2,10,11,34,35,36

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change. Specifications can be TBD and the part package and pinout are not final.
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.