FRONTGRADE

PROGRAMMING

MRAM

CertusPro-NX FPGA Configuration

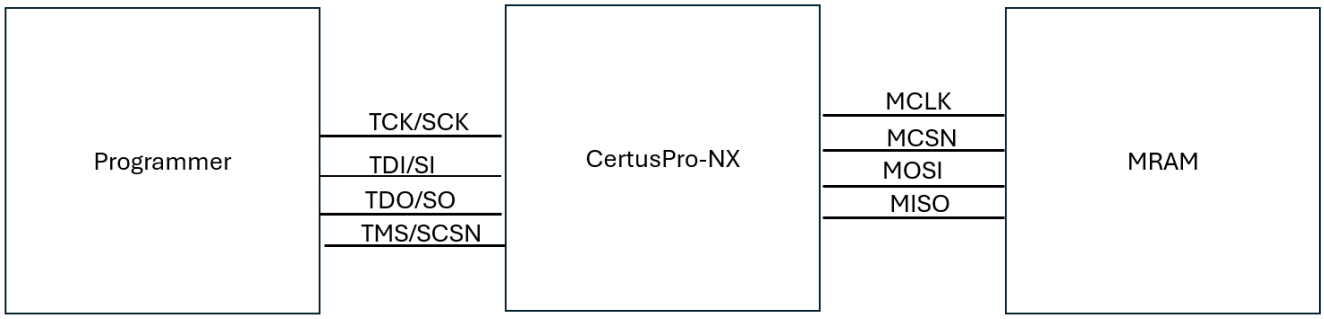
2/23/2026

Version #:

Overview

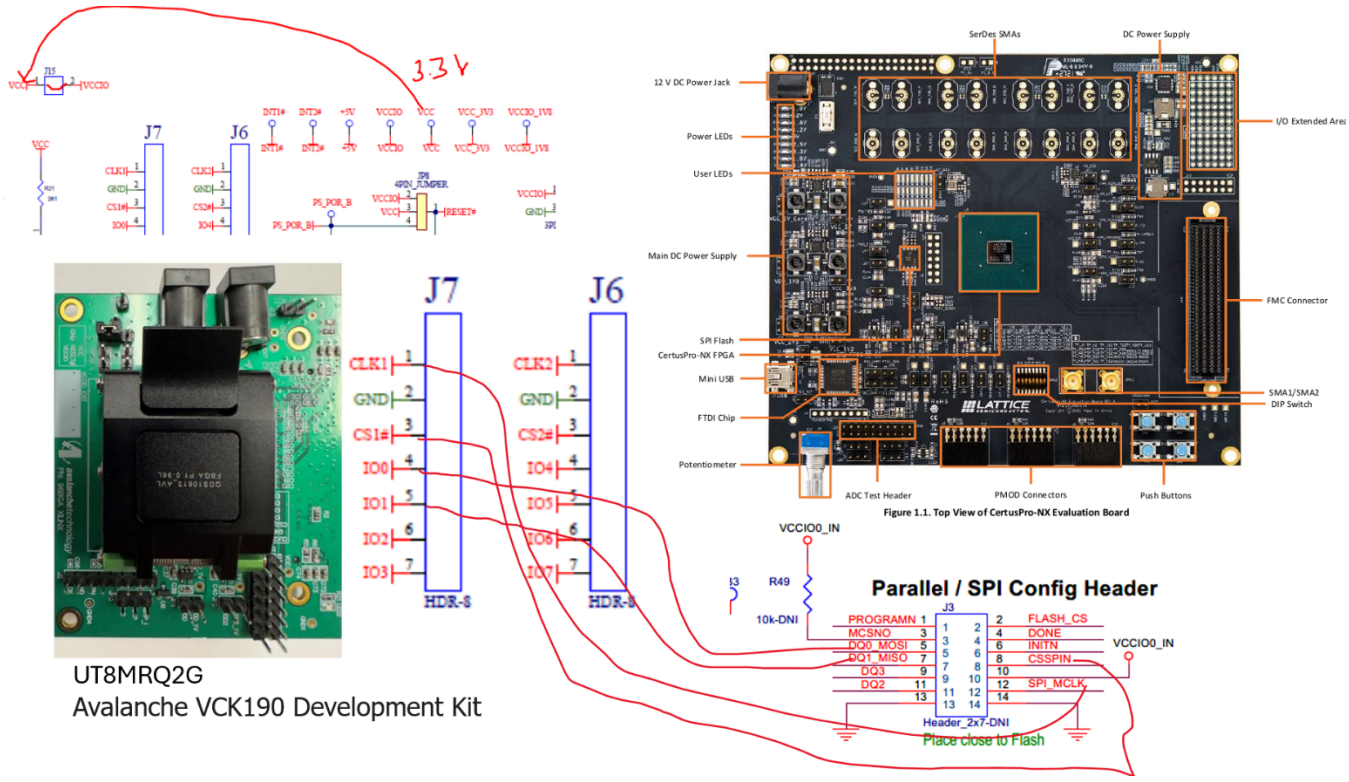
Non-volatile MRAM provides lower power, higher endurance, and faster read and write speeds. Programming the MRAM device using Lattice Radiant tools requires the JTAG connection. For more detailed instructions, see FPGA-EB-02032-1-2-Certus-NX-Versa-Evaluation-Board or similar CertusPro-NX evaluation board.

Note: For Avalanche MRAM devices having 128 Mb, and/or 1,2,4,8 Gb, Lattice Radiant Software version 2025.2 or higher must be used.



Certus-NX Device

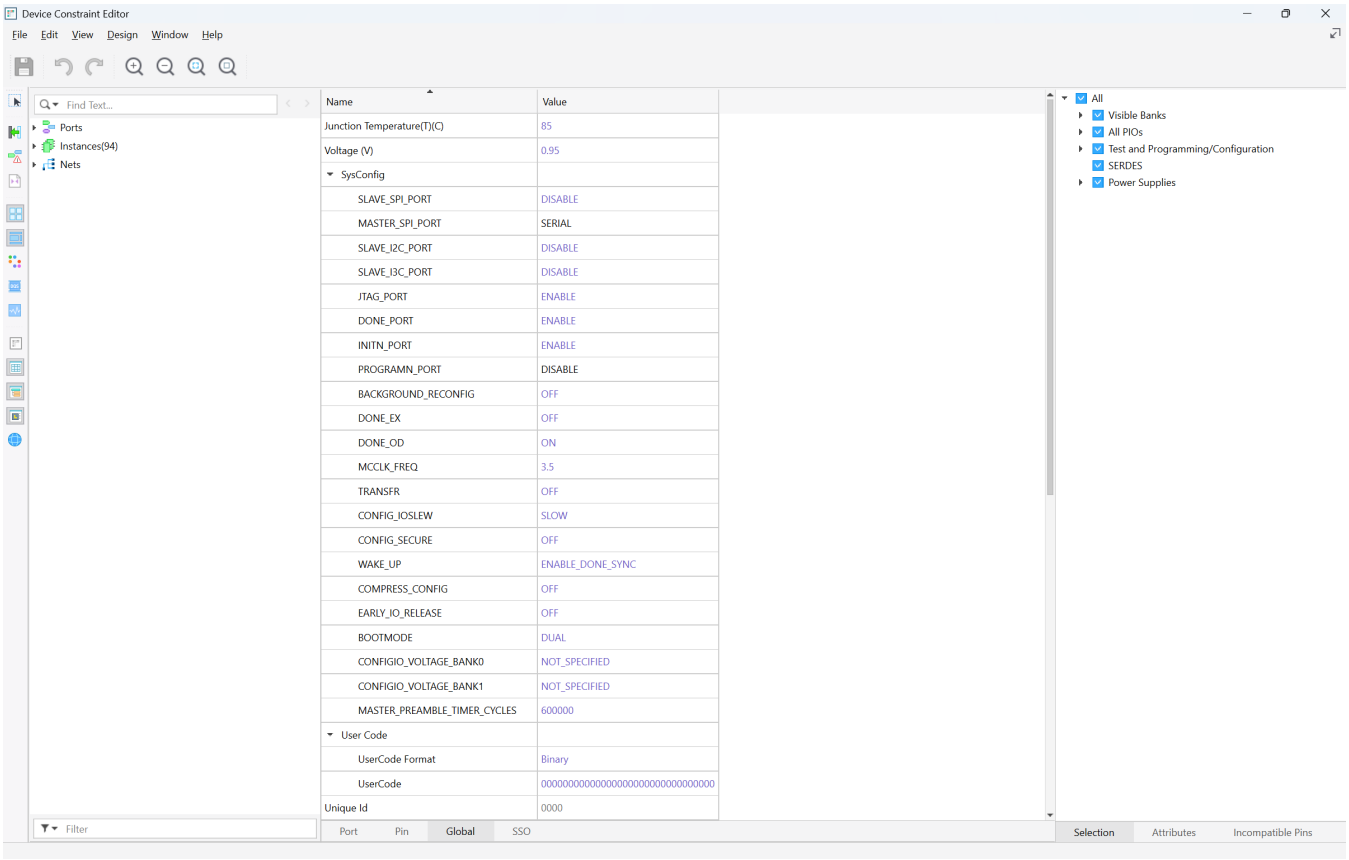
The CertusPro-NX Evaluation Board is the LFCPNX-100-9LFG672C. The Eval Board can be used in a wide range of applications. For more information on the capabilities of CertusPro-NX device, see CertusPro-NX Family Data Sheet (FPGA-DS-02086).



UT8MRQ2G
Avalanche VCK190 Development Kit

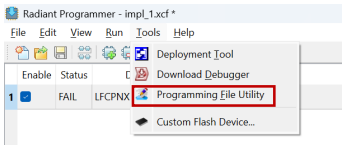
Device Constraint Editor Global Settings

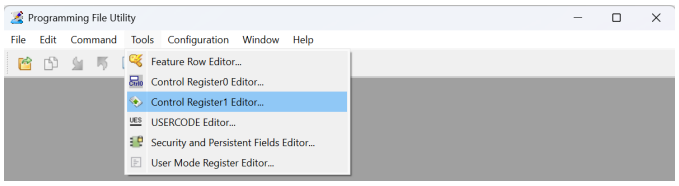
After the particular design has been compiled, select the following Global settings and recompile the design, see picture below.

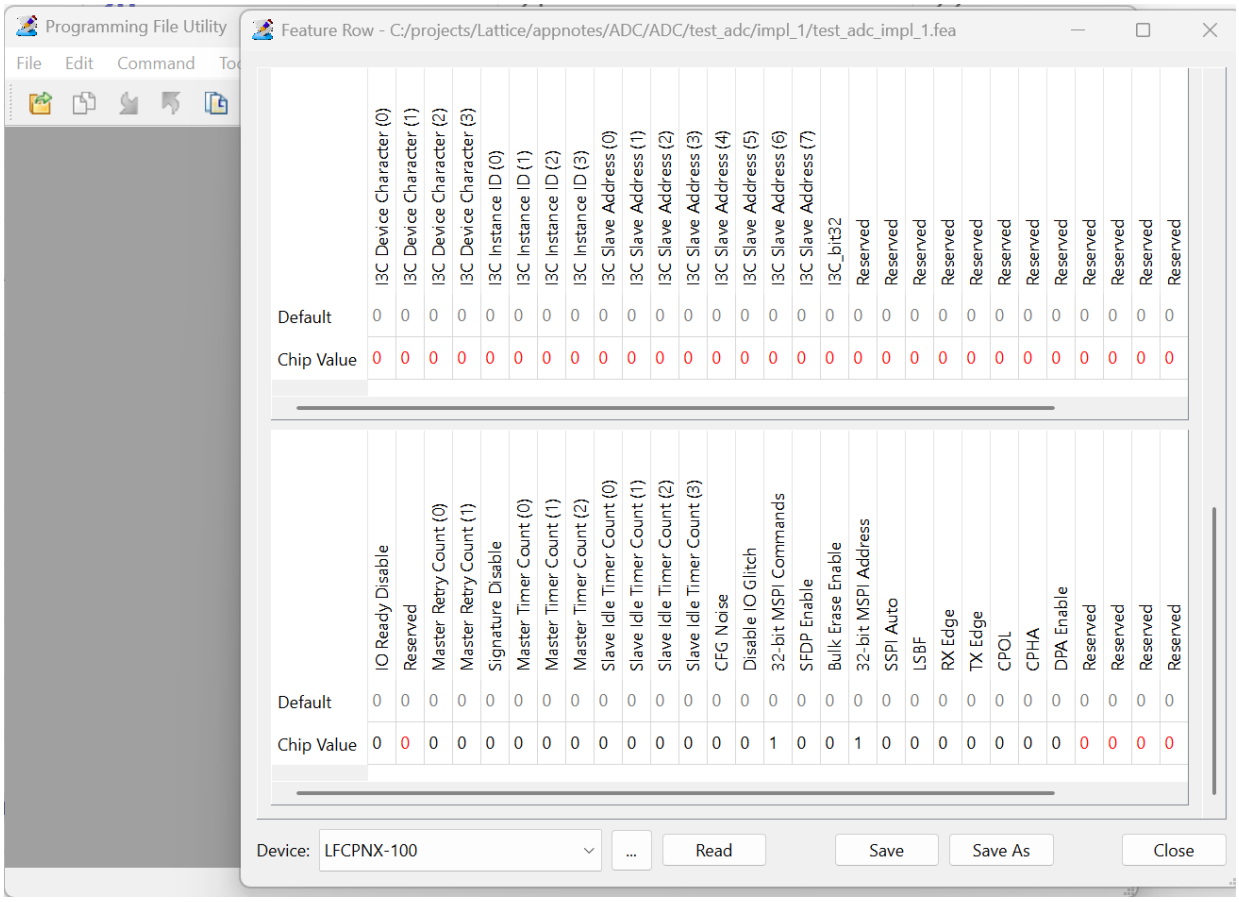


MRAM 32-bit Address Configuration

From the Tools menu, select Programming File Utility and a new window opens, see picture below. On the new window, from the Tools menu, select Feature Row Editor, and set 32-bit MSPI Address and 32-bit MSPI Commands; click Save, see pictures below.



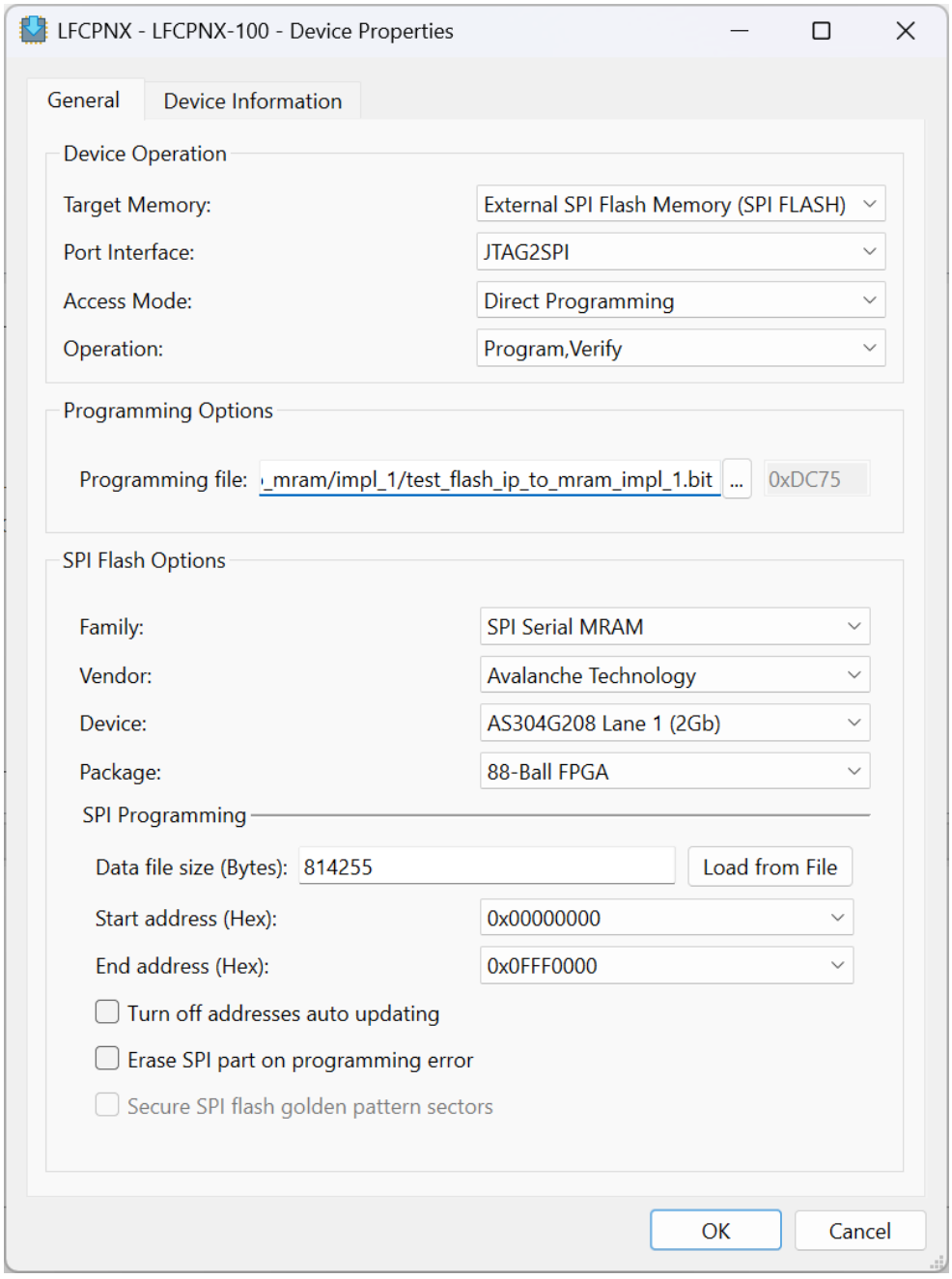




Programmer MRAM Configuration

From the **Edit** menu, select **Device Properties…** and a new window opens, choose the appropriate setting for the particular design, see picture below.

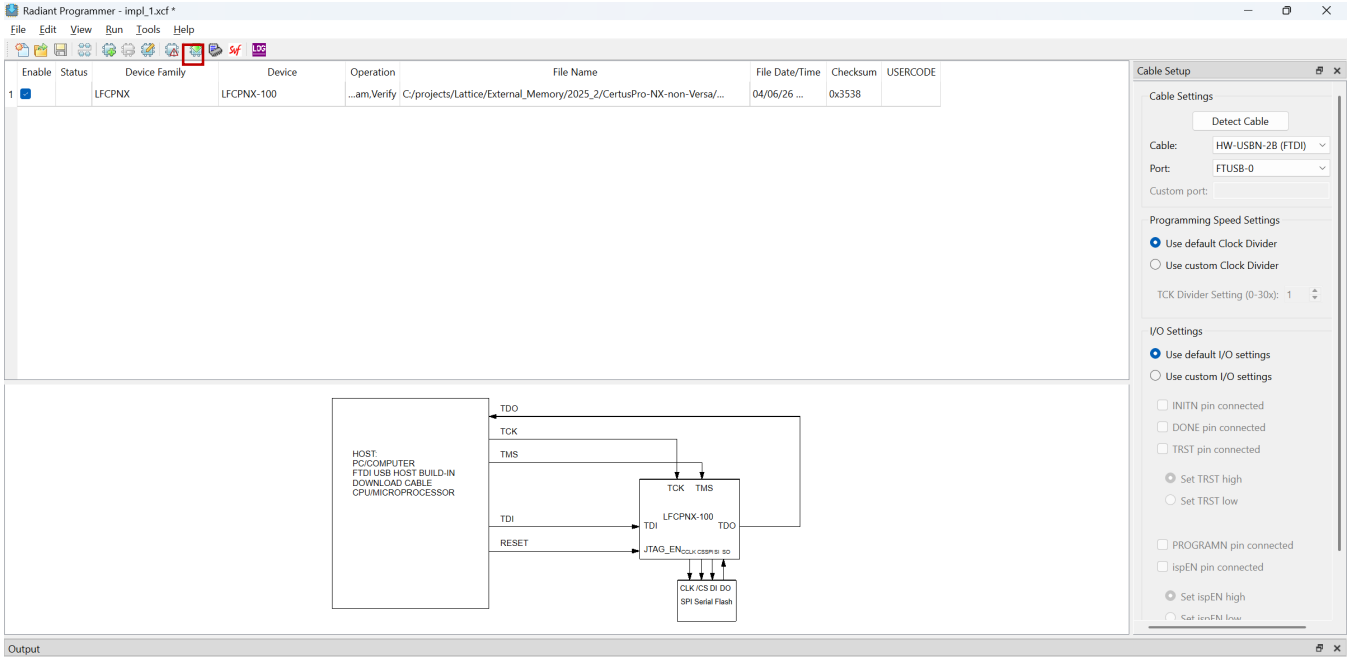
Note: Tested on 96 ball FBGA package, and it works the same as 88-Ball FPGA as long as the interface is SPI and device has plenty of memory.



Program the Device with Radiant Programmer

From the **Tools** menu, select **Programmer** and a new window opens, see picture below. Once the cable is detected and settings are set, program the device by clicking the Program Device icon  , see picture below.

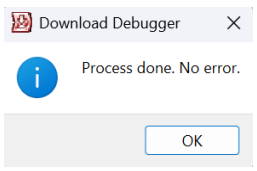
Note: In case the device ID code hasn't been set up and regular programmer fails, you can use the Download Debugger (Tools > Download Debugger) to get around it. See below for "Check the IDCODE" lines commented out.




```
! Check the IDCODE

!ISPEN  LOW;
!SDR    8   TDI   (07);
!SDR    24  TDI   (000000);
!SDR    32  TDI   (00000000)
!       TDO   (C208F08C);

// IDCode Checking...
!SDR 32 TDI(000000F9)
!       TDO(54FFFFFF)
!       MASK(FF000000) ;
// Enabling...
SDR 8 TDI(60) ;
// Programming...
SDR 8 TDI(60) ;
// Address 00000000h
```



Verify the Hardware Interface

Verify that the design uses switches SW[3:0] for controlling the duty cycle to the pwm output, which controls the brightness to LED[0]; LED[7:1] are used as heartbeat of the system.

References

For more information, refer to the following documents:

- 8N1 UART Tranceiver (FPGA-RD-02196-1.0)
- sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095)
- sysDSP Usage Guide for Nexus Platform (FPGA-TN-02096)
- sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099)
- CertusPro-NX SerDes/PCS Usage Guide (FPGA-TN-02245)
- sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067)
- Soft Error Detection (SED)/Correction (SEC) Usage Guide for Nexus Platform (FPGA-TN-02076)
- Memory Usage Guide for Nexus Platform (FPGA-TN-02094)
- ADC Usage Guides for Nexus Platform (FPGA-TN-02129)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Power Management and Calculation for CertusPro-NX Devices (FPGA-TN-02257)
- CertusPro-NX 50k Pinout File (FPGA-SC-02023)
- CertusPro-NX 100k Pinout File (FPGA-SC-02022)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Multi-Boot Usage Guide for Nexus Platform (FPGA-TN-02145)
- I^2C Hardened IP Usage Guide for Nexus Platform (FPGA-TN-02142)

Version #:

Revision History

Date	Revision #	Author	Change Description	Page #
10/23/2006	1.0.0	JA	Initial Release.	