



# FRONTGRADE

## DATASHEET

### UT8Q512K32E

16Megabit RadTolerant SRAM MCM

6/1/2020  
Version #: 2.0.0

## Features

- 25ns maximum (3.3 Volt supply) address access time
- MCM contains four (4) 512K×8 industry-standard asynchronous SRAMs; the control architecture allows operation as 8, 16, 24 or 32-bit data width
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Typical radiation performance:
  - Total dose: 100 krad(Si)
  - SEL Immune: 110 MeV-cm<sup>2</sup>/mg
  - SEU Onset LETth : =>2.8 MeV- cm<sup>2</sup>/mg
  - Saturated Cross Section 2.8E-8 cm<sup>2</sup>/bit
    - 1.1E-9 errors/bit-day, Adams 90% worst case environment geosynchronous orbit
- Packaging:
  - 68-lead dual cavity ceramic quad flatpack (CQFP)(11.0 grams)
- Standard Microcircuit Drawing 5962-01533
  - QML Q & V compliant part

## Introduction

The UT8Q512K32E RadTolerant product is a high-performance 2M byte (16Mbit) CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 × 8 bit SRAMs with a common output enable. Memory expansion is provided by an active LOW Chip Enable ( $\overline{E_n}$ ), an active LOW Output Enable ( $\overline{G}$ ), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory is accomplished by taking Chip Enable ( $\overline{E_n}$ ) input LOW and Write Enable ( $\overline{W_n}$ ) inputs LOW. Data on the eight I/O pins (DQ0 through DQ7) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking Chip Enable ( $\overline{E_n}$ ) and Output Enable ( $\overline{G}$ ) LOW while forcing Write Enable ( $\overline{W_n}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ( $\overline{E_n}$  HIGH), the outputs are disabled ( $\overline{G}$  HIGH), or during a write operation ( $\overline{E_n}$  LOW and  $\overline{W_n}$  LOW). Perform 8, 16, 24 or 32 bit accesses by making  $\overline{W_n}$  along with  $\overline{E_n}$  a common input to any combination of the discrete memory die.

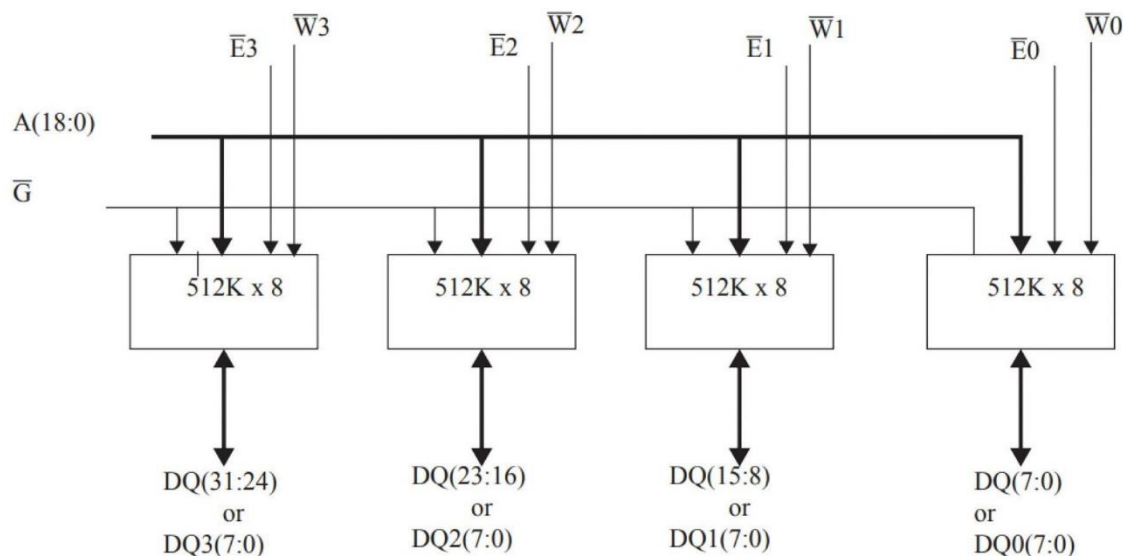


Figure 1: UT8Q512K32E SRAM Block Diagram

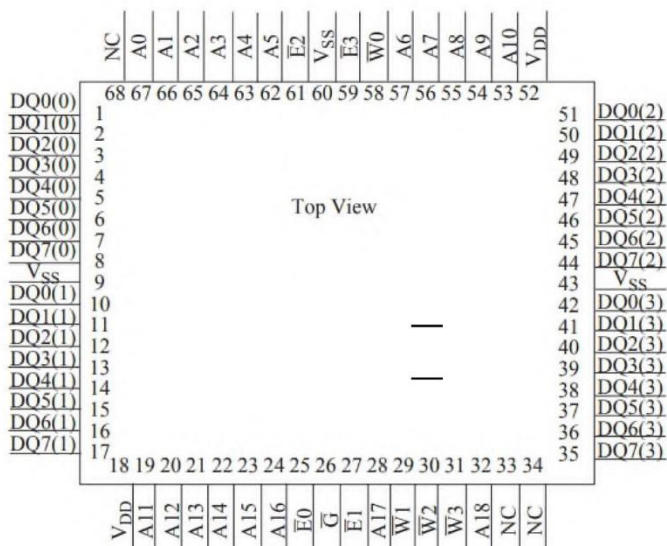


Figure 2: 25ns SRAM Pinout (68)

## Pin Names

A(18:0)	Address	$\overline{Wn}$	Write Enable
DQ(7:0)	Data Input/Output	$\overline{G}$	Output Enable
En	Enable	$V_{DD}$	Power (1.8V)
		$V_{SS}$	Ground

## Device Operation

The UT8R512K32E has three control inputs called Chip Enable ( $\overline{En}$ ), Write Enable ( $\overline{Wn}$ ), and Output Enable ( $\overline{G}$ ); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0).  $\overline{En}$  Device Enable controls device selection, active, and standby modes. Asserting  $\overline{En}$  enables the device, causes  $I_{DD}$  to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory.  $\overline{Wn}$  controls read and write operations. During a read cycle,  $\overline{G}$  must be asserted to enable the outputs.

**Table 1. Device Operation Truth Table**

$\overline{G}$	$\overline{Wn}$	$\overline{En}$	I/O Mode	Mode
X <sup>1</sup>	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read <sup>2</sup>
0	1	0	Data out	Read

### Notes:

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

## Read Cycle

A combination of  $\overline{Wn}$  greater than  $V_{IH}$  (min) and  $\overline{En}$  less than  $V_{IL}$  (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of any chip enable or any address change while any chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs while the chip is enabled with  $\overline{G}$  asserted and  $\overline{Wn}$  deasserted. Valid data appears on data outputs DQ(7:0) after the specified  $t_{AVQV}$  is satisfied. Outputs remain active throughout the entire cycle. As long as Chip Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time ( $t_{AVAV}$ ). Changing addresses prior to satisfying  $t_{AVAV}$  minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-Controlled Access in Figure 4b, is initiated by  $\overline{E_n}$  going active while  $\overline{G}$  remains asserted,  $\overline{W_n}$  remains deasserted, and the addresses remain stable for the entire cycle. After the specified  $t_{ETQV}$  is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM Read Cycle 3, the Output Enable-Controlled Access in Figure 4c, is initiated by  $\overline{G}$  going active while  $\overline{E_n}$  is asserted,  $\overline{W_n}$  is deasserted, and the addresses are stable. Read access time is  $t_{GLQV}$  unless  $t_{AVQV}$  or  $t_{ETQV}$  have not been satisfied.

## Write Cycle

A combination of  $\overline{W_n}$  less than  $V_{IL}(\text{max})$  and  $\overline{E_n}$  less than  $V_{IL}(\text{max})$  defines a write cycle. The state of  $\overline{G}$  is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either  $\overline{G}$  is greater than  $V_{IH}(\text{min})$ , or when  $\overline{W_n}$  is less than  $V_{IL}(\text{max})$ .

Write Cycle 1, the Write Enable-Controlled Access in Figure 5a, is defined by a write terminated by  $\overline{W_n}$  going high, with  $\overline{E_n}$  still active. The write pulse width is defined by  $t_{WLWH}$  when the write is initiated by  $\overline{W_n}$ , and by  $t_{ETWH}$  when the write is initiated by  $\overline{E_n}$ . Unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-Controlled Access in Figure 5b is defined by a write terminated by  $\overline{E_n}$  going inactive. The write pulse width is defined by  $t_{WLEF}$  when the write is initiated by  $\overline{W_n}$ , and by  $t_{ETEF}$  when the write is initiated by the  $\overline{E_n}$  going active. For the  $\overline{W_n}$  initiated write, unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

## Operational Environment

The UT8Q512K32E SRAM incorporates features which allow operation in a limited radiation environment.

**Table 2. Operational Environment Design Specifications<sup>1</sup>**

Total Dose	100	krad(Si)
Heavy Ion Error Rate <sup>2</sup>	$\leq 1.1\text{E-}9$	Errors/Bit-Day
SEU LET <sub>TH</sub>	2.8	MeV- cm <sup>2</sup> /mg
SEL	Immune to 110	MeV- cm <sup>2</sup> /mg

### Notes:

1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 90% worst case particle environment, geosynchronous orbit, 100 mils of Aluminum.

## Absolute Maximum Ratings<sup>1</sup>

(Referenced to  $V_{SS}$ )

Symbol	Parameter	Limits
$V_{DD}$	DC supply voltage	-0.5 to 4.6V
$V_{I/O}$	Voltage on any pin	-0.5 to 4.6V
$T_{STG}$	Storage temperature	-65 to +150°C
$P_D$	Maximum power dissipation	1.0W (per byte)
$T_J$	Maximum junction temperature <sup>2</sup>	+150°C
$\theta_{JC}$	Thermal resistance, junction-to-case	10°C/W
$I_I$	DC input current	±10 mA

### Notes:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
- Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

## Recommended Operating Conditions

Symbol	Parameter	Limits
$V_{DD2}$	Positive supply voltage	3.0 to 3.6V
$T_C$	Case temperature range	( $\bar{W}$ ) Screening: -40 to +105°C
$V_{IN}$	DC input voltage	0V to $V_{DD}$



## DC Electrical Characteristics (Pre- and Post-Radiation)\*

**-40°C to +105°C ( $V_{DD} = 3.3V \pm 0.3V$ )**

Symbol	Parameter	Condition	MIN	MAX	Unit
$V_{IH}$	High-level input voltage		2.0		V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OL1}$	Low-level output voltage	$I_{OL} = 6mA$ , $V_{DD} = 3.0V$ (TTL)		0.4	V
$V_{OL2}$	Low-level output voltage	$I_{OL} = 200\mu A$ , $V_{DD} = 3.0V$ (CMOS)		0.08	V
$V_{OH1}$	High-level output voltage	$I_{OH} = -3mA$ , $V_{DD} = 3.0V$ (TTL)	2.2		V
$V_{OH2}$	High-level output voltage	$I_{OH} = -200\mu A$ , $V_{DD} = 3.0V$ (CMOS)	$0.8 \cdot V_{DD}$		V
$C_{IN1}^1$	Input capacitance: All Address and Output Enable Pins	$f = 1MHz$ @ 0V		45	pF
$C_{IN2}^1$	Input capacitance: All Enable and Write Enable Pins	$f = 1MHz$ @ 0V		18	pF
$C_{IO}^1$	Bidirectional I/O capacitance	$f = 1MHz$ @ 0V		25	pF
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ and $V_{SS}$ , $V_{DD} = V_{DD} (max)$	-2	2	$\mu A$
$I_{OZ}$	Three-state output leakage current	$V_O = V_{DD}$ and $V_{SS}$ $V_{DD} = V_{DD} (max)$ $\bar{G} = V_{DD} (max)$	-2	2	$\mu A$
$I_{OS}^{2,3}$	Short-circuit output current	$V_{DD} = V_{DD} (max)$ , $V_O = V_{DD}$ $V_{DD} = V_{DD} (max)$ , $V_O = 0V$	-90	90	mA
$I_{DD} (OP)$	Supply current operating @ 1MHz (per byte)	Inputs: $V_{IL} = 0.8V$ , $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		40	mA
$I_{DD1} (OP)$	Supply current operating @40MHz (per byte)	Inputs: $V_{IL} = 0.8V$ , $V_{IH} = 2.0V$ $I_{OUT} = 0mA$ $V_{DD} = V_{DD} (max)$		70	mA
$I_{DD2} (SB)$	Supply current operating @ 0MHz (per byte)	Inputs: $V_{IL} = V_{SS}$ $I_{OUT} = 0mA$ $\bar{E}_n = V_{DD} - 0.5$ $V_{DD} = V_{DD} (max)$	-40°C, 25°C	16	mA
			105°C	24	mA

### Notes:

\*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Post-radiation limit based off of high temperature limit.

## AC Characteristics Read Cycle (Pre- and Post-Radiation) \*

**-40°C to +105°C ( $V_{DD} = 3.3V \pm 0.3V$ )**

Symbol	Parameter	MIN	MAX	Unit
$t_{AVAV}^{1,6}$	Read cycle time	25		ns
$t_{AVSK}^5$	Address valid to address valid skew time		4	ns
$t_{AVQV}$	Read access time		25	ns
$t_{AXQX}^2$	Output hold time	3		ns
$t_{GLQX}^2$	$\overline{G}$ -controlled Output Enable time	0		ns
$t_{GLQV}$	$\overline{G}$ -controlled Output Enable time (Read Cycle 3)		10	ns
$t_{GHQZ}^2$	$\overline{G}$ -controlled output three-state time		10	ns
$t_{ETQX}^{2,3}$	$\overline{E}n$ -controlled Output Enable time	3		ns
$t_{AVET}^5$	Address setup time for read ( $\overline{E}n$ -controlled)	-4		ns
$t_{ETQV}^3$	$\overline{E}n$ -controlled access time		25	ns
$t_{EFQZ}^{1,2,4}$	$\overline{E}n$ -controlled output three-state time		10	ns

### Notes:

\*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

- Functional test.
- Three-state is defined as a 300mV change from steady-state output voltage.
- The ET (chip enable true) notation refers to the latter falling edge of  $\overline{E}n$ . SEU immunity does not affect the read parameters.
- The EF (chip enable false) notation refers to the latter rising edge of  $\overline{E}n$ . SEU immunity does not affect the read parameters.
- Guaranteed by design
- Address changes prior to satisfying  $t_{AVAV}$  minimum is an invalid operation

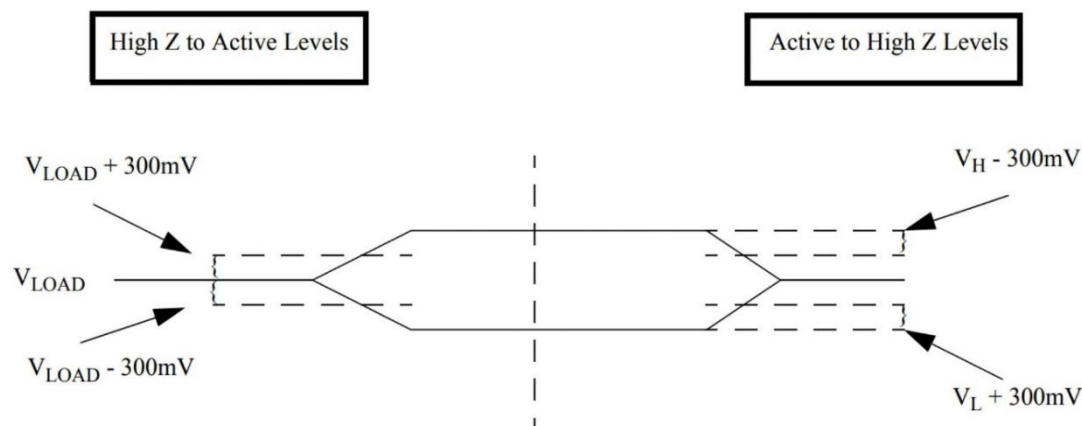


Figure 3. 3.3-Volt SRAM Loading



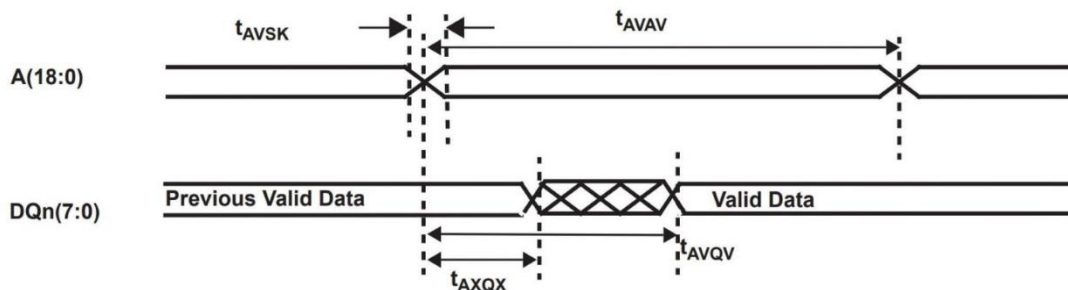


Figure 4a. SRAM Read Cycle 1: Address Access

**Assumption:**

1.  $\overline{E_n}$  and  $\overline{G} \leq V_{IL}(\text{max})$  and  $\overline{W_n} \geq V_{IH}(\text{min})$

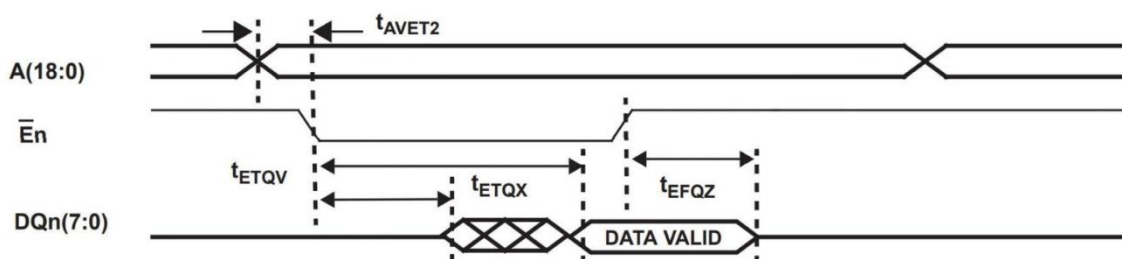


Figure 4b. SRAM Read Cycle 2: Chip Enable Access

**Assumption:**

1.  $\overline{G} \leq V_{IL}(\text{max})$  and  $\overline{W_n} \geq V_{IH}(\text{min})$

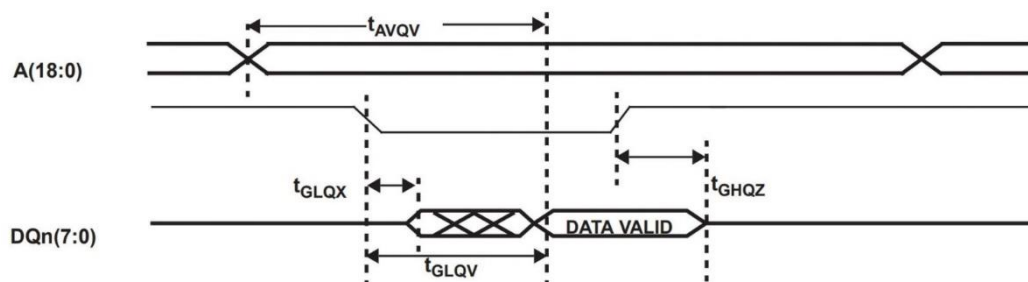


Figure 4c. SRAM Read Cycle 3: Output Enable Access

**Assumption:**

1.  $\overline{E_n} \leq V_{IL}(\text{max})$  and  $\overline{W_n} \geq V_{IH}(\text{min})$ .

## AC Characteristics Write Cycle (Pre- and Post-Radiation)\*

**-40°C to +105°C ( $V_{DD} = 3.3V \pm 0.3V$ )**

Symbol	Parameter	MIN	MAX	Unit
$t_{AVAV}^1$	Write cycle time	25		ns
$t_{ETWH}$	Chip Enable to end of write	20		ns
$t_{AVET}$	Address setup time for write ( $\bar{E}n$ - controlled)	1		ns
$t_{AVWL}$	Address setup time for write ( $\bar{W}n$ - controlled)	0		ns
$t_{WLWH}$	Write pulse width	20		ns
$t_{WHAX}$	Address hold time for write ( $\bar{W}n$ - controlled)	0		ns
$t_{EFAX}$	Address hold time for Device Enable ( $\bar{E}n$ - controlled)	0		ns
$t_{WLQZ}^2$	$\bar{W}n$ - controlled three-state time		10	ns
$t_{WHQX}^2$	$\bar{W}n$ - controlled Output Enable time	4		ns
$t_{ETEF}$	Chip Enable pulse width ( $\bar{E}n$ - controlled)	20		ns
$t_{DVWH}$	Data setup time	15		ns
$t_{WHDX}$	Data hold time	2		ns
$t_{WLEF}$	Chip Enable controlled write pulse width	20		ns
$t_{DVEF}$	Data setup time	15		ns
$t_{EFDX}$	Data hold time	2		ns
$t_{AVWH}$	Address valid to end of write	20		ns
$t_{WHWL}^1$	Write disable time	5		ns

### Notes:

\*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Functional test performed with outputs disabled ( $\bar{G}$  high).
2. Three-state is defined as 300mV change from steady-state output voltage.

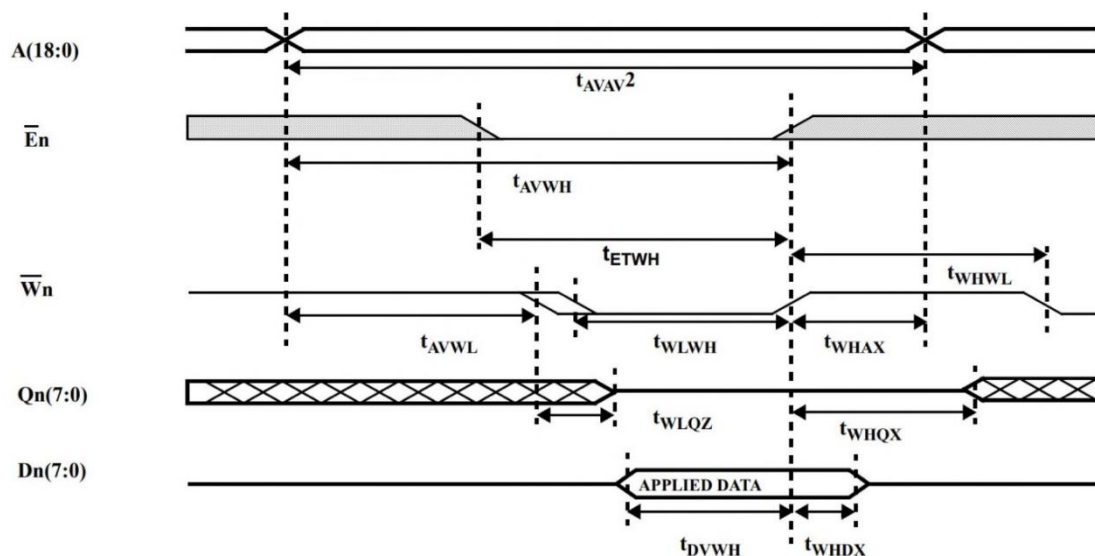


Figure 5a. SRAM Write Cycle 1: W - Controlled Access

### Assumptions:

1.  $\bar{G} \leq V_{IL}(\text{max})$ . If  $\bar{G} \geq V_{IH}(\text{min})$  then Qn(7:0) will be in three-state for the entire cycle.
2.  $\bar{G}$  high for  $t_{AVAV}$  cycle.

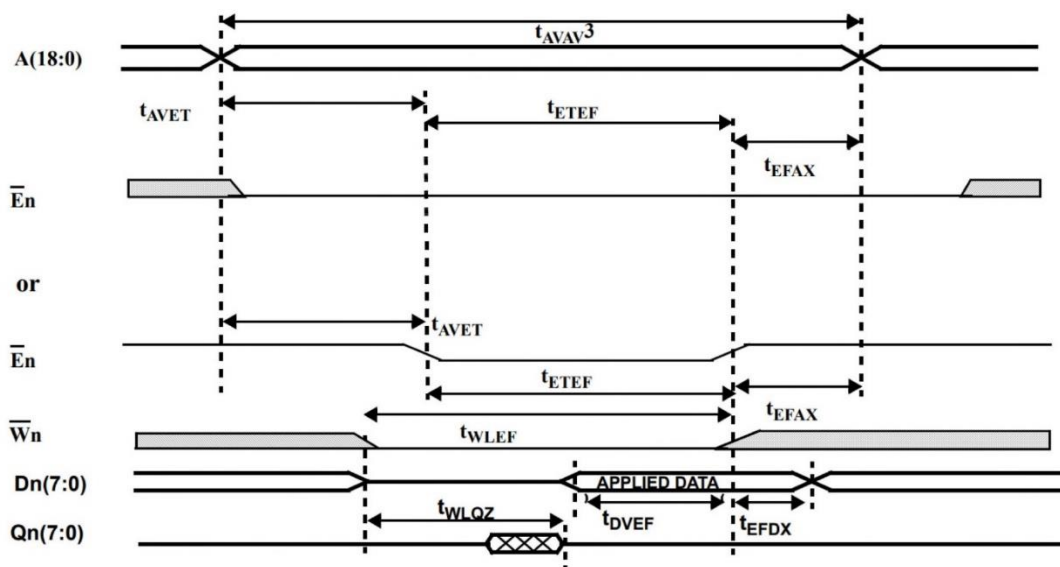


Figure 5b.

### Assumptions & Notes:

1.  $\bar{G} \leq V_{IL}(\text{max})$ . If  $\bar{G} \geq V_{IH}(\text{min})$  then Qn(7:0) will be in three-state for the entire cycle.
2. Either  $\bar{E}_n$  scenario above can occur.
3.  $\bar{G}$  high for  $t_{AVAV}$  cycle.

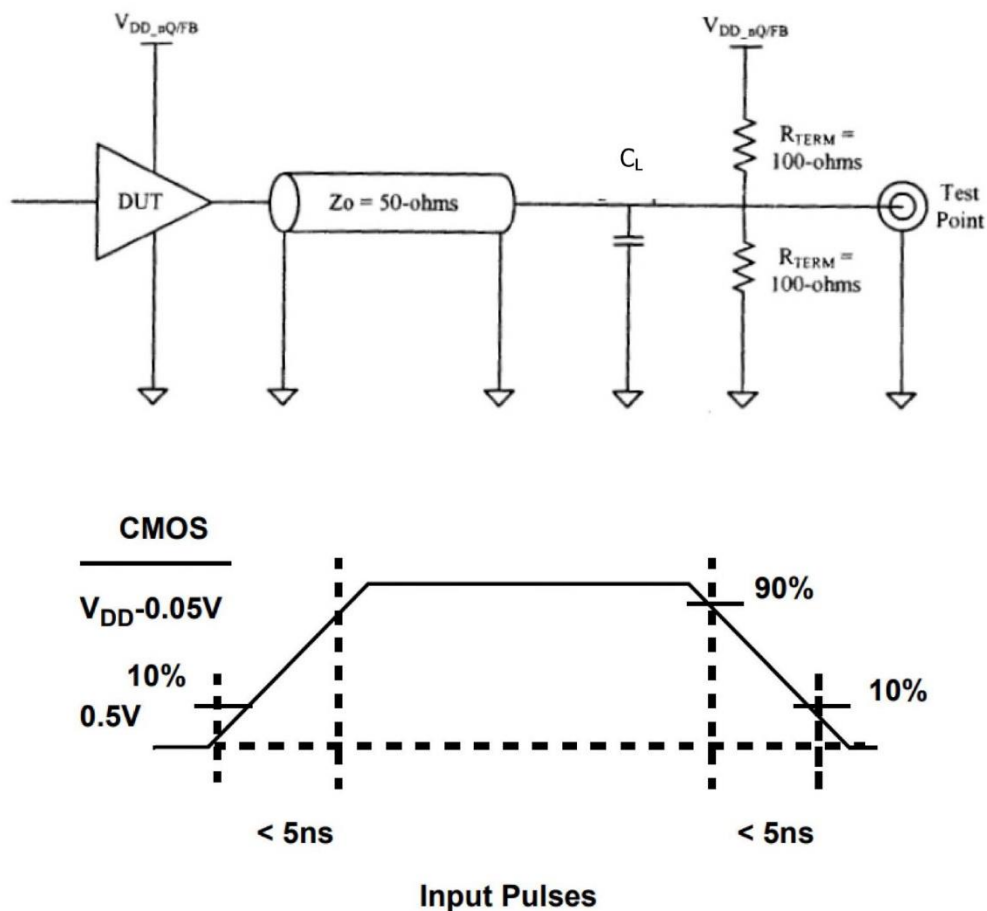


Figure 6. AC Test Loads and Input Waveforms

**Notes:**

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input =  $V_{DD2}/2$ ).

### Data Retention Characteristics (Pre-Radiation)\*

( $V_{DD} = V_{DD}(\min)$ , 1 Sec DR Pulse)

Symbol	Parameter	TEMP	Minimum	Maximum	Unit
$V_{DR}$	$V_{DD}$ for data retention	--	2.0	--	V
$I_{DDR}^{1,2}$	Data retention current (per byte)	-40°C	--	16	mA
		25°C	--	16	mA
		105°C	--	24	mA
$t_{EFR}^{1,2}$	Chip deselect to data retention time	--	0	--	ns
$t_R^{1,2}$	Operation recovery time	--	$t_{AVAV}$	--	ns

#### Notes:

\*Post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019.

- $\overline{EN} = V_{DR}$  all other inputs =  $V_{DR}$  or  $V_{SS}$
- Not guaranteed or tested

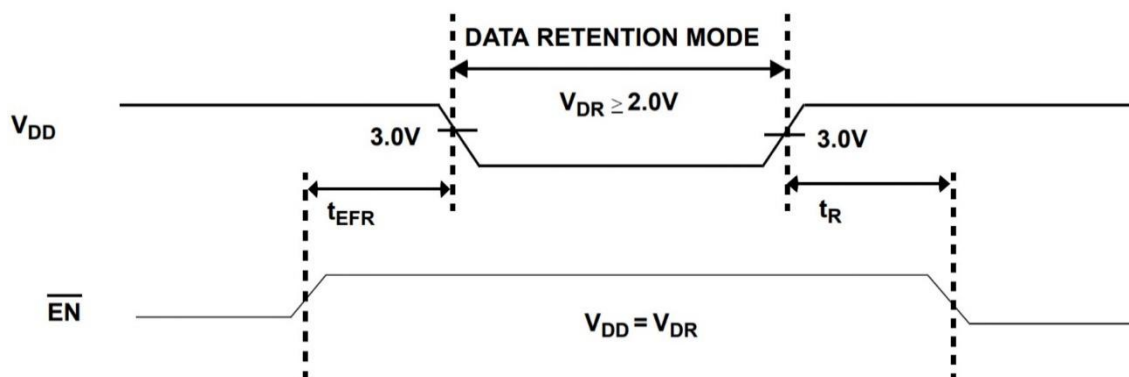


Figure 7. Low  $V_{DD}$  Data Retention Waveform

## Packaging

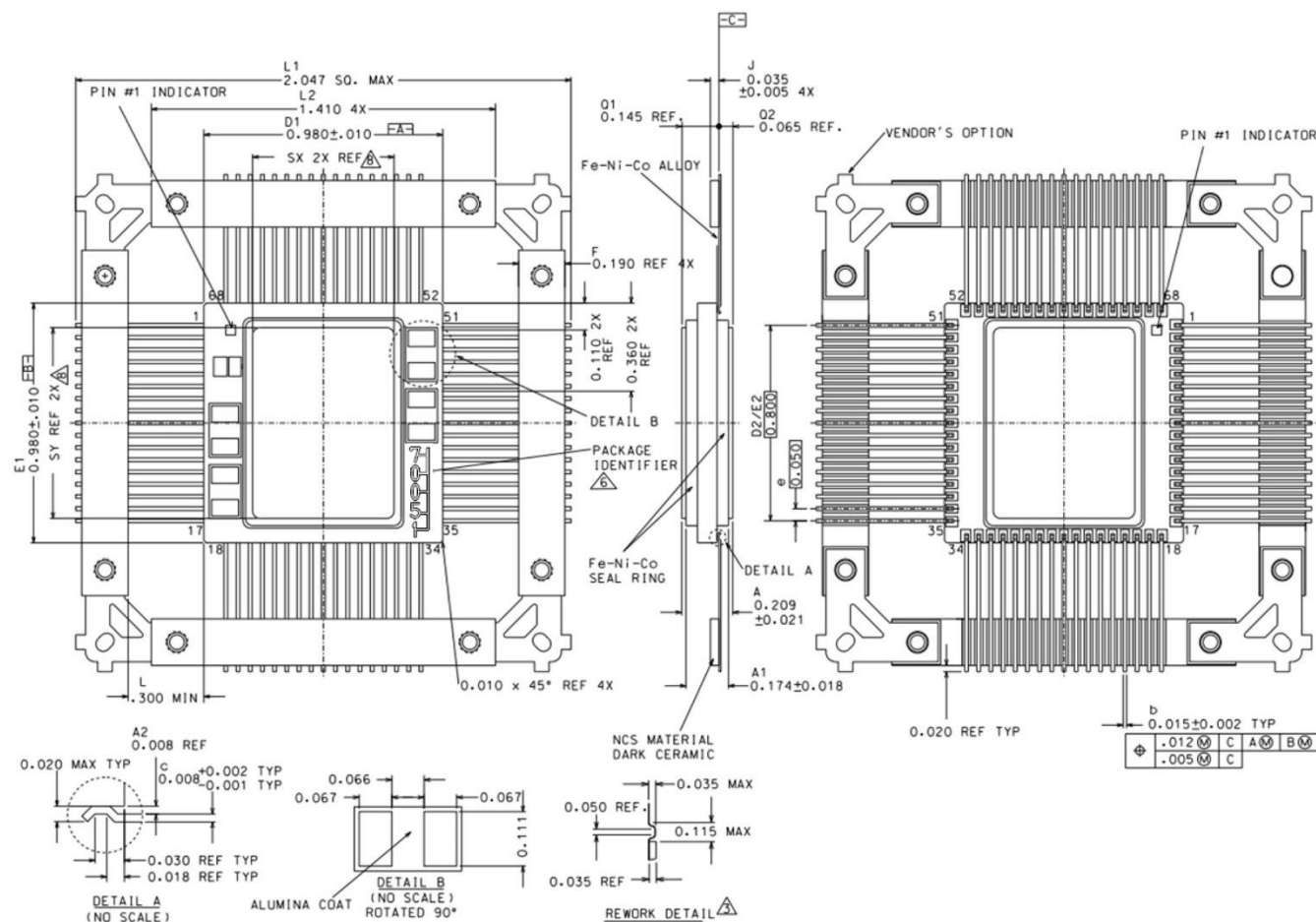


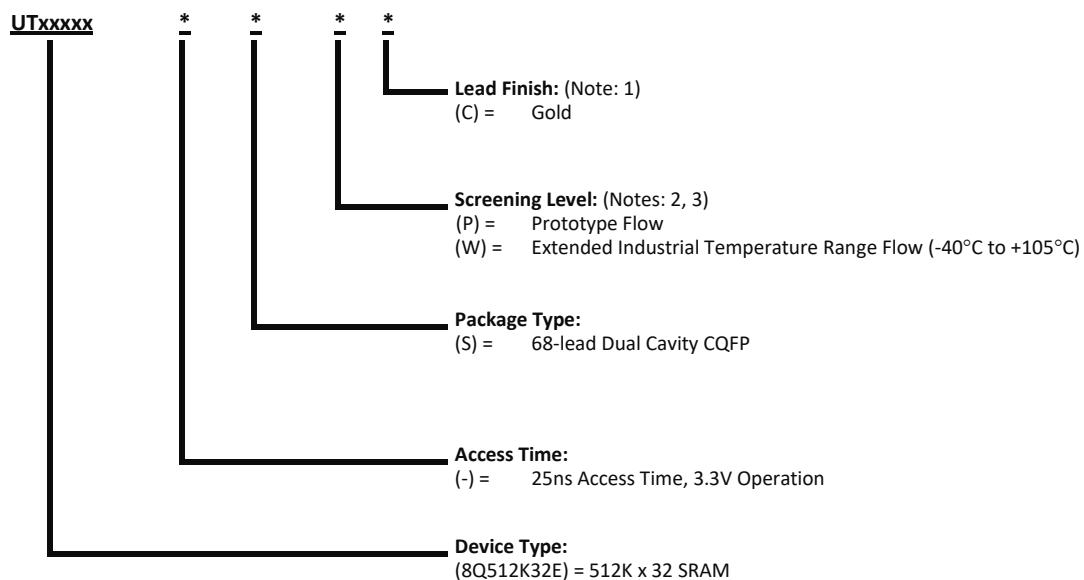
Figure 8. 68-pin Ceramic Quad Flatpack

### Notes:

1. All exposed metallized areas are gold plated over nickel per MIL-PRF-38535.
2. The lids are electrically connected to  $V_{SS}$ .
3. Packages may be shipped with repaired leads as shown.
4. Coplanarity requirements do not apply in repaired area.
5. Letter designations are to cross reference to MIL-STD-1835.
6. Lead true position tolerances and coplanarity are not measured.
7. Capacitor pads are sized to fit CDR32 (1206) capacitors.

## Ordering Information

### Frontgrade Part Numbering Ordering Information

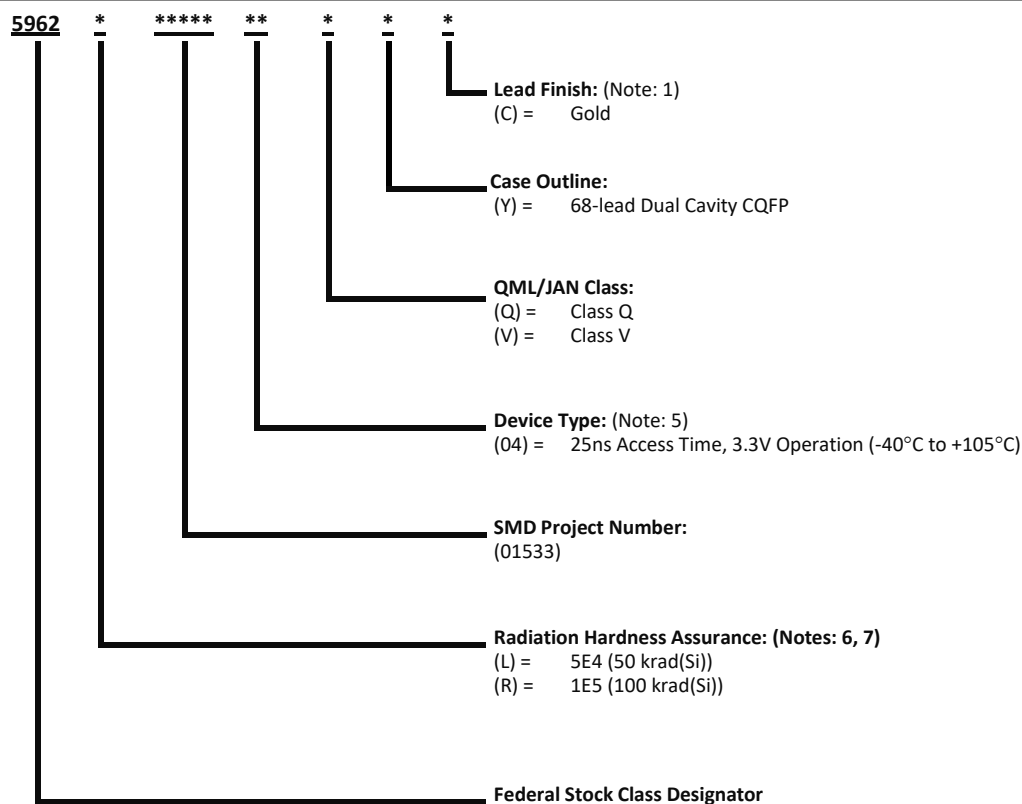


#### Notes:

1. Gold lead finish only.
2. Prototype flow per Frontgrade Colorado Springs Manufacturing Flows Document. Devices are tested at 25°C. Radiation neither tested nor guaranteed.
3. Extended Industrial Range flow per Frontgrade Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C to 105°C. Radiation neither tested nor guaranteed.



### SMD Part Number Ordering Information



#### Notes:

- Lead finish is "C" (Gold) only.
- Total dose radiation must be specified when ordering.

## Revision History

Date	Revision #	Author	Change Description	Page #
7/15/19	1.0.0		Added wording addressing read app note AN-MEM-002 and added timing parameters to AC Characteristics Read Cycle table, figure 4a and 4b; Corrected notes at the bottom of both AC electrical tables	
6/20	2.0.0		Raised max TID to 100krads (Si); changed abs max ratings for $V_{DD}$ and VI/O to match SMD; Typo fixes; Split input capacitance to clarify capacitance differences between bussed inputs and single inputs; Increased standby current to 16mA; changed timing parameters $t_{GLQX}$ and $t_{AVET}$ ; added note to data retention table (page 11); change package identification marking on package outline; revised SMD PN buildup page to reflect new device type and TID offering.	11

## Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the <b>datasheet is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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