

# FRONTGRADE

## DATASHEET

### UT54LVDS218

Deserializer

9/21/2022

Version #: 1.0.3

## Features

- 15 to 75MHz shift clock support
- 50% duty cycle on receiver output clock
- Low power consumption
- Cold sparing all pins
- $\pm 1V$  common mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Megabytes/sec bandwidth
- 325 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge strobe
- Operational Environment; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total dose: 300 krad(Si) and 1 Mrad(Si)
  - Latchup immune ( $LET \leq 100 \text{ MeV-cm}^2/\text{mg}$ )
- Packaging options:
  - 48-lead flatpack (1.4 grams)
- Standard Microcircuit Drawing 5962-01535
  - QML Q and V compliant part
- Compatible with TIA/EIA-644 LVDS Standard

## Introduction

The UT54LVDS218 Deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/sec).

The UT54LVDS218 Deserializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have Cold Spare buffers. These buffers will be high impedance when  $V_{DD}$  is tied to  $V_{SS}$ .

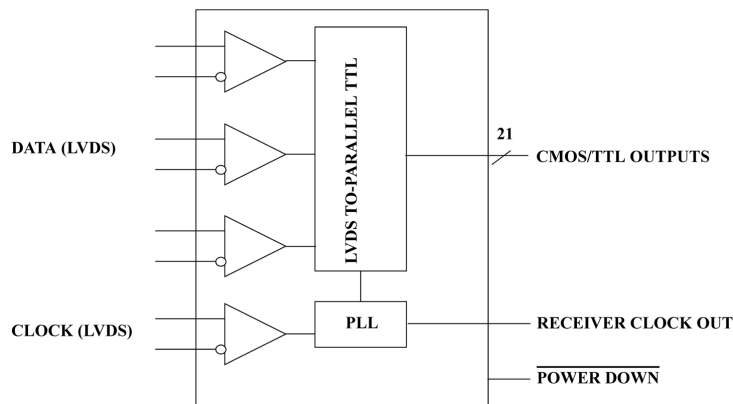


Figure 1. UT54LVDS218 Deserializer Block Diagram

RxOUT 17	1	UT54LVDS218	48	V <sub>DD</sub>
RxOUT 18	2		47	RxOUT 16
GND	3		46	RxOUT 15
RxOUT 19	4		45	RxOUT 14
RxOUT 20	5		44	GND
N/C	6		43	RxOUT 13
LVDS GND	7		42	V <sub>DD</sub>
RxIN0-	8		41	RxOUT 12
RxIN0+	9		40	RxOUT 11
RxIN1-	10		39	RxOUT 10
RxIN1+	11		38	GND
LVDS V <sub>DD</sub>	12		37	RxOUT 9
LVDS GND	13		36	V <sub>DD</sub>
RxIN2-	14		35	RxOUT 8
RxIN2+	15		34	RxOUT 7
RxCLK IN-	16		33	RxOUT 6
RxCLK IN+	17		32	GND
LVDS GND	18		31	RxOUT 5
PLL GND	19		30	RxOUT 4
PLL V <sub>DD</sub>	20		29	RxOUT 3
PLL GND	21		28	V <sub>DD</sub>
PWR DWN	22		27	RxOUT 2
RxCLK OUT	23		26	RxOUT 1
RxOUT0	24		25	GND

Figure 2. UT54LVDS218 Pinout

## Pin Description

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs <sup>1</sup>
RxIN-	I	3	Negative LVDS differential data output <sup>1</sup>
RxOUT	O	21	TTL level data outputs
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN-	I	1	Negative LVDS differential clock input
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low
V <sub>DD</sub>	I	4	Power supply pins for TTL outputs and logic
GND	I	5	Ground pins for TTL outputs and logic
PLL V <sub>DD</sub>	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V <sub>DD</sub>	I	1	Power supply pin for LVDS pins
LVDS GND	I	3	Ground pins for LVDS inputs

### Notes:

- These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, data outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

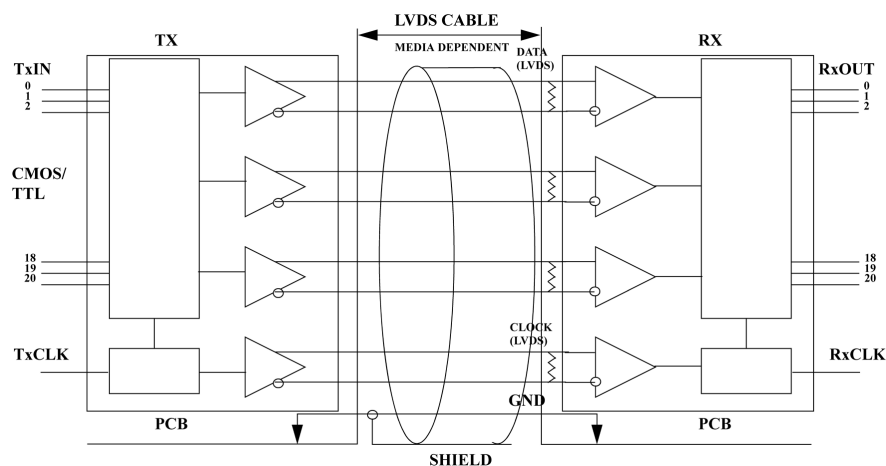


Figure 3. UT54LVDS218 Typical Application

## Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	1.0E6	rad(Si)
Single Event Latchup (SEL)	≤100	MeV-cm <sup>2</sup> /mg
Neutron Fluence <sup>1</sup>	1.0E13	n/cm <sup>2</sup>

### Notes:

1. Guaranteed but not tested.

## Absolute Maximum Ratings<sup>1</sup>

(Referenced to  $V_{SS}$ )

Symbol	Parameter	Limits
$V_{DD}$	DC supply voltage	-0.3 to 4.0V
VI/O	Voltage on any pin	-0.3 to ( $V_{DD} + 0.3V$ )
$ESD_{HBM}$	HBM ESD Rating	1000V
$T_{STG}$	Storage temperature	-65 to +150°C
$P_D$	Maximum power dissipation	1.25 W
$T_J$	Maximum junction temperature <sup>2</sup>	+150°C
$\Theta_{JC}$	Thermal resistance, junction-to-case <sup>3</sup>	10°C/W
II	DC input current	±10mA

### Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.
4. For cold spare mode ( $V_{DD} = V_{SS}$ ), VI/O may be -0.3V to the maximum recommended operating  $V_{DD} + 0.3V$ .

## Recommended Operating Conditions

Symbol	Parameter	Limits
$V_{DD}$	Positive Supply voltage	3.0 to 3.6V
$T_C$	Case temperature range	-55 to +125°C
$V_{IN}$	DC input voltage	0V to $V_{DD}$

## DC Electrical Characteristics\*1

( $V_{DD} = 3.3V$  to  $0.3V$ ;  $-55^{\circ}C < T_c < +125^{\circ}C$ ); Unless otherwise noted,  $T_c$  is per the temperature noted.

Symbol	Parameter	Condition	MIN	MAX	Unit
CMOS/TTL DC Specifications (PWR DWN, RXOUT)					
$V_{IH}$	High-level input voltage		2.0	$V_{DD}$	V
$V_{IL}$	Low-level input voltage		GND	0.8	V
$V_{OL}$	Low-level input voltage	$I_{OL} = 2mA$		0.3	V
$V_{OH}$	High-level input voltage	$I_{OL} = -0.4mA$	2.7		V
$I_{IH}$	High-level input current	$V_{IN}=3.6V$ ; $V_{DD} = 3.6V$	-10	+10	$\mu A$
$I_{IL}$	Low-level input current	$V_{IN}=0V$ ; $V_{DD} = 3.6V$	-10	+10	mA
$V_{CL}$	Input clamp voltage	$I_{CL} = -18mA$		-1.5	V
$I_{CS}$	Cold Spare Leakage current	$V_{IN}=3.6V$ ; $V_{DD} = V_{SS}$	-20	+20	mA
$I_{OS}^{2,3}$	Output short circuit current	$V_{OUT} = 0V$	-15	-130	mA
LVDS Receiver DC Specifications (IN+, IN-)					
$V_{TH}^3$	Differential input high threshold	$V_{CM} = +1.2V$		+100	mV
$V_{T3}^4$	Differential input low threshold	$V_{CM} = +1.2V$	-100		mV
$V_{CMR}^4$	Common mode voltage range	$V_{ID}=210mV$	0.2	2.00	V
$I_{IN}$	Input current	$V_{IN} = +2.4V$ , $V_{DD} = 3.6V$	-10	+10	mA
		$V_{ID} = 0V$ , $V_{DD} = 3.6V$	-10	+10	mA
$I_{CSIN}$	Cold Spare Leakage Current	$V_{IN} = 3.6V$ , $V_{DD} = V_{SS}$	-20	+20	mA
Supply Current					
$I_{CC}^3$	Active supply current	CL=8pF (see Figure 5)		105	mA
$I_{CCPD}$	Power down supply current	PWR DWN= Low, LVDS inputs = logic low, $V_{DD} = 3.6V$		2.0	mA

### Notes:

- \*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at  $25^{\circ}C$  per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
- Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
- Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, for a maximum duration of one second.
- Guaranteed by characterization.
- Tested functionally.

## Receiver Switching Characteristics\*<sup>1</sup>

(V<sub>DD</sub> = 3.0V to 3.6V; T<sub>c</sub> = -55°C to +125°C); Unless otherwise noted, T<sub>c</sub> is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit	
CLHT <sup>3</sup>	CMOS/TTL Low-to-High Transition Time (Figure 5)		3.5	ns	
CHLT <sup>3</sup>	CMOS/TTL High-to-Low Transition Time (Figure 5)		3.5	ns	
RSPos0 <sup>3</sup>	Receiver Input Strobe Position for Bit 0 (Figure 10)	0.50	1.24	ns	
RSPos1 <sup>3</sup>	Receiver Input Strobe Position for Bit 1 (Figure 10)	2.41	3.15	ns	
RSPos2 <sup>3</sup>	Receiver Input Strobe Position for Bit 2 (Figure 10)	f =75MHz	4.31	5.05	ns
RSPos3 <sup>3</sup>	Receiver Input Strobe Position for Bit 3 (Figure 10)	f =75MHz	6.22	6.96	ns
RSPos4 <sup>3</sup>	Receiver Input Strobe Position for Bit 4 (Figure 10)	f =75MHz	8.12	8.86	ns
RSPos5 <sup>3</sup>	Receiver Input Strobe Position for Bit 5 (Figure 10)	f =75MHz	10.03	10.77	ns
RSPos6 <sup>3</sup>	Receiver Input Strobe Position for Bit 6(Figure 10)	f =75MHz	11.93	12.67	ns
RCOP <sup>3</sup>	RxCLK OUT Period (Figure 6)	f =75MHz	13.3	66.7	ns
RCOH <sup>3</sup>	RxCLK OUT High Time (Figure 6)	f =75MHz	3.6		ns
RCOL <sup>3</sup>	RxCLK OUT Low Time (Figure 6)	f =75MHz	3.6		ns
RSRC <sup>4</sup>	RxOUT Setup to RxCLK OUT (Figure 6)	f =75MHz	3.5		ns
RHRC <sup>4</sup>	RxOUT Hold to RxCLK OUT (Figure 6)	f =75MHz	3.5		ns
RCCD <sup>2</sup>	RxCLK IN to RxCLK OUT Delay (Figure 7)	f =75MHz	3.4	8.3	ns
RPLLS <sup>5</sup>	Receiver Phase Lock Loop Set (Figure 8)	f =75MHz		10	ms
RPDD	Receiver Powerdown Delay (Figure 9)	f =75MHz		2	μs

### Notes:

- \*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
- Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock jitter less than 250 ps (calculated from TPOS - RPOS) - see Figure 11.
- Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for LVDS217 Serializer and the LVDS218 Deserializer is (T + TCCD) + 2\*T + RCCD, where T = Clock period.
- Guaranteed by characterization.
- Guaranteed by design.
- Tested functionally.



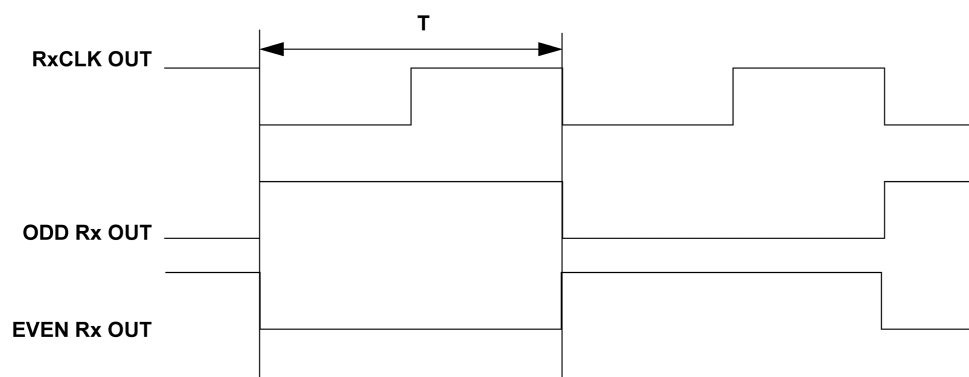


Figure 4. Test Pattern

## AC Timing Diagrams

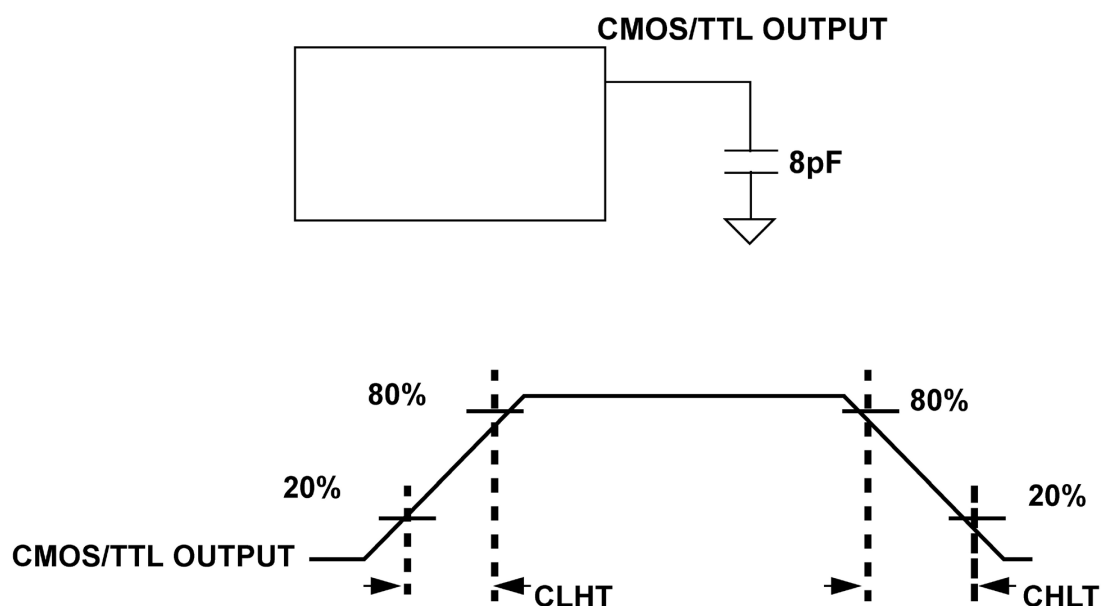


Figure 5. UT54LVDS218 Output Load and Transition Times

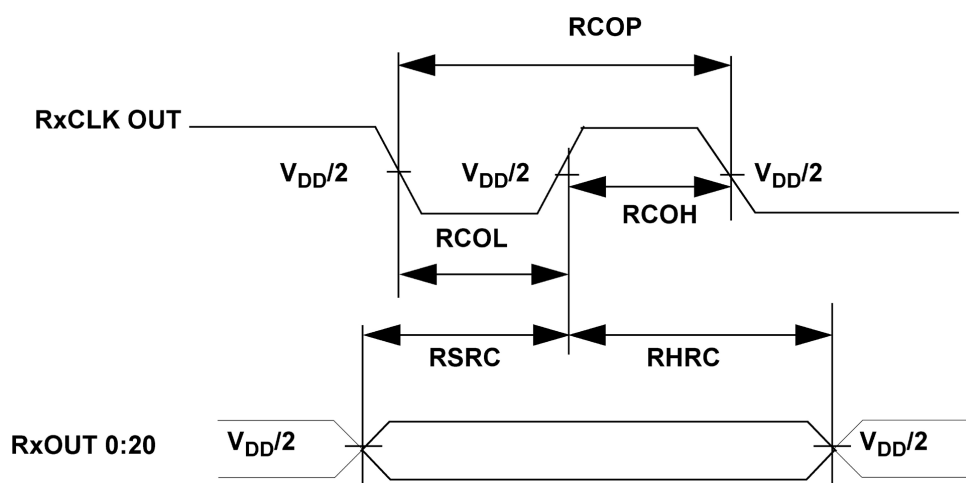


Figure 6. UT54LVDS218 Setup/Hold and High/Low Times

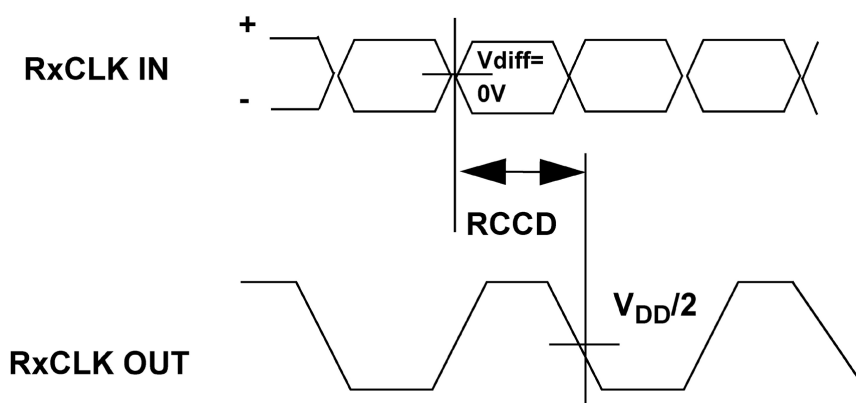


Figure 7. UT54LVDS218 Clock-to-Clock Out Delay

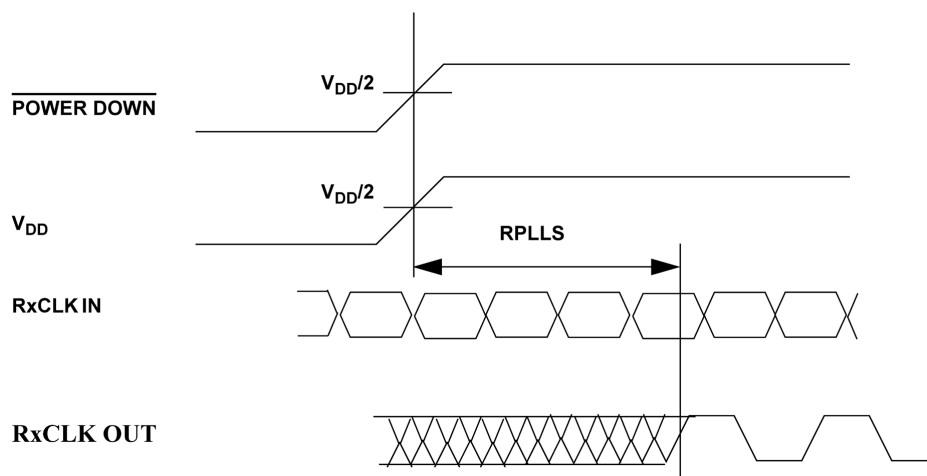


Figure 8. UT54LVDS218 Phase Lock Loop Set Time

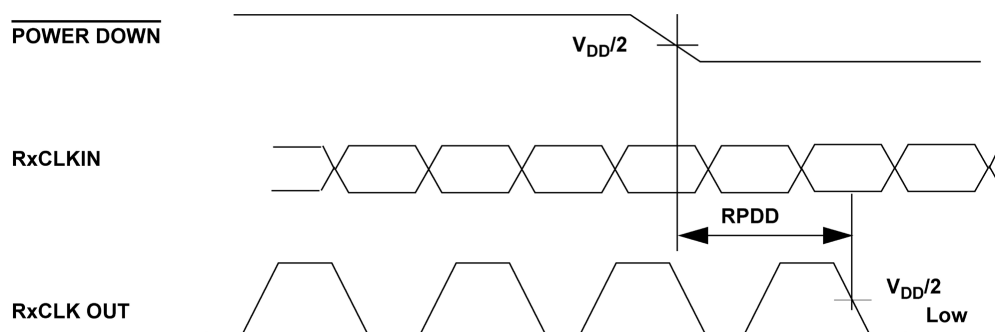


Figure 9. Receiver Powerdown Delay

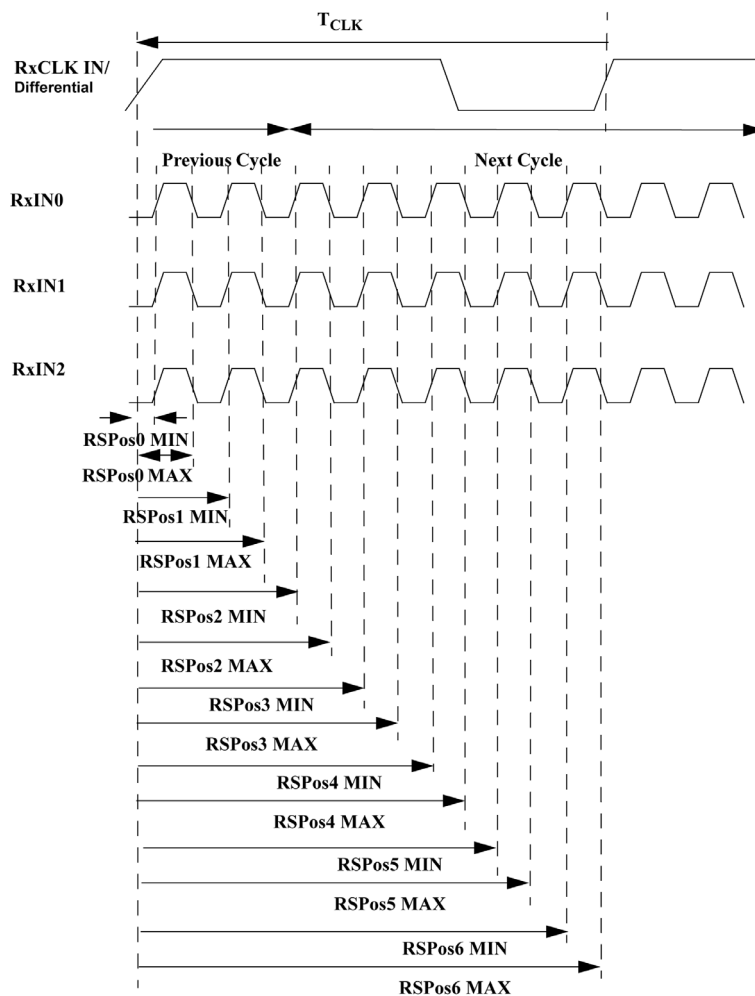
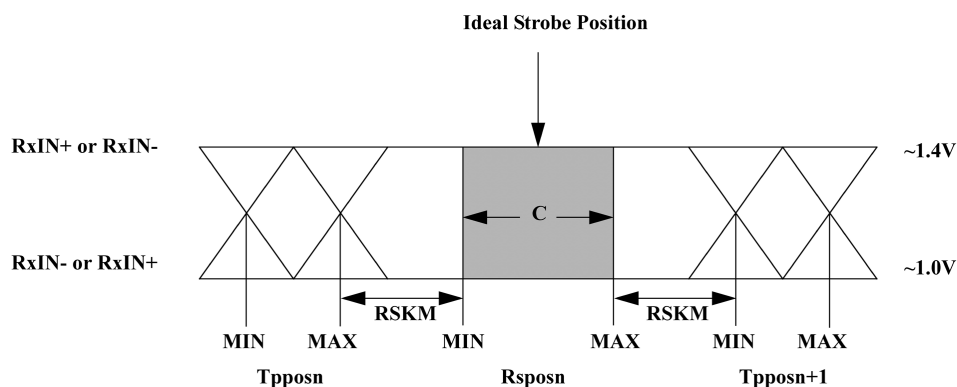


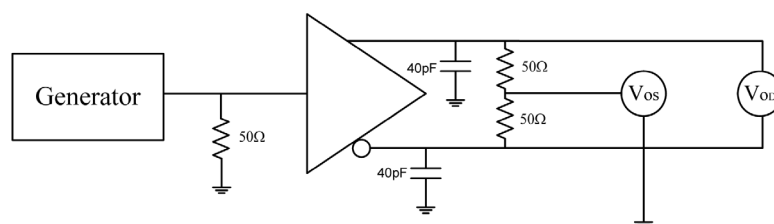
Figure 10. Receiver LVDS Input Strobe Position



- $C$  - Setup and Hold Time (Internal data sampling window) defined by  $RSPOSN$  (receiver input strobe position min and max)
- $TPPOSN$  - Transmitter output pulse position (min and max)
- Cable Skew – based on type and length, typically 10 ps-40 ps per foot, media dependent Source Clock Jitter - Cycle-to-cycle jitter is less than 250 ps at 75MHz.
- ISI - Inter-symbol interference, dependent on interconnect length, may be zero.

$$RSKM(Side) > \frac{\text{Cable Skew}}{2} + \frac{\text{Source Clock Jitter}}{2} + \frac{ISI}{2}$$

Figure 11. Receiver LVDS Skew Margin


Figure 12. Driver  $V_{OD}$  and  $V_{OS}$  Test Circuit or Equivalent Circuit

## Packaging

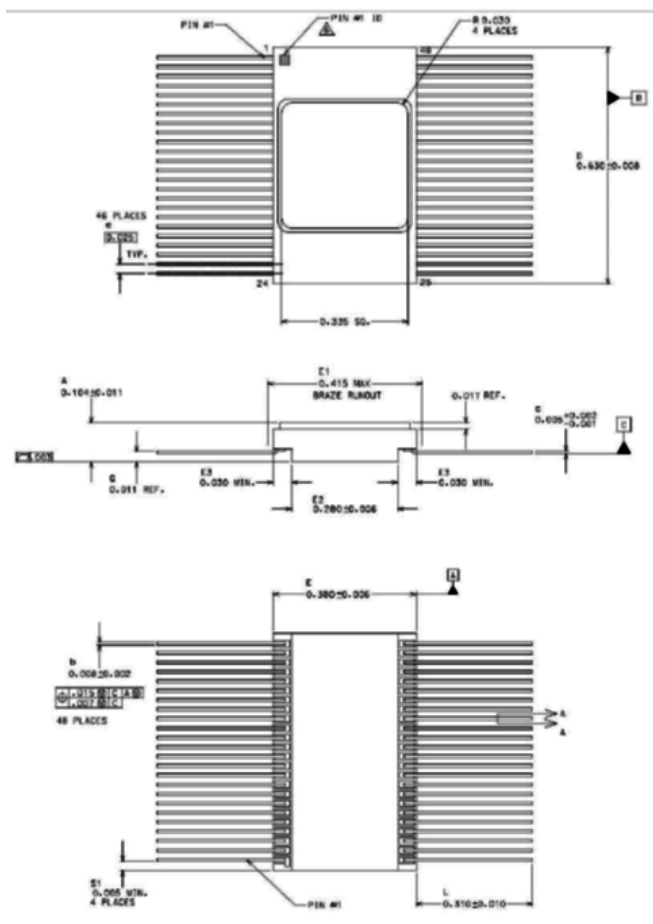


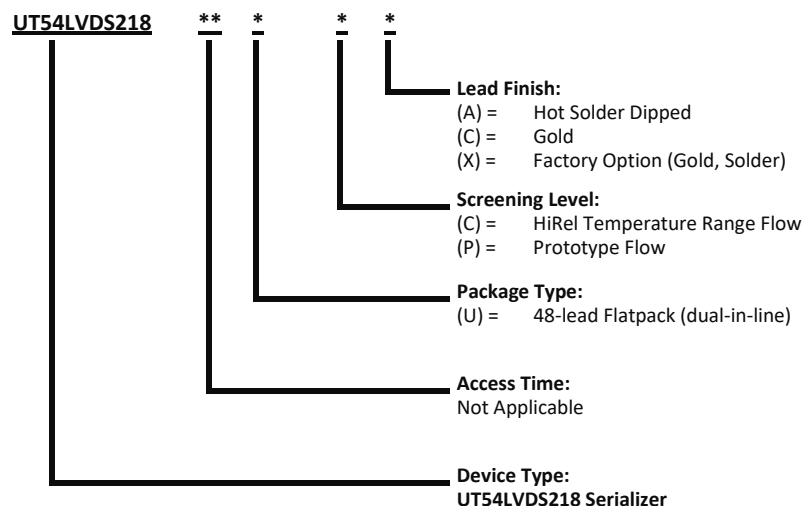
Figure 13. 48-Lead Flatpack

### Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to  $V_{SS}$ .
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

## Ordering Information

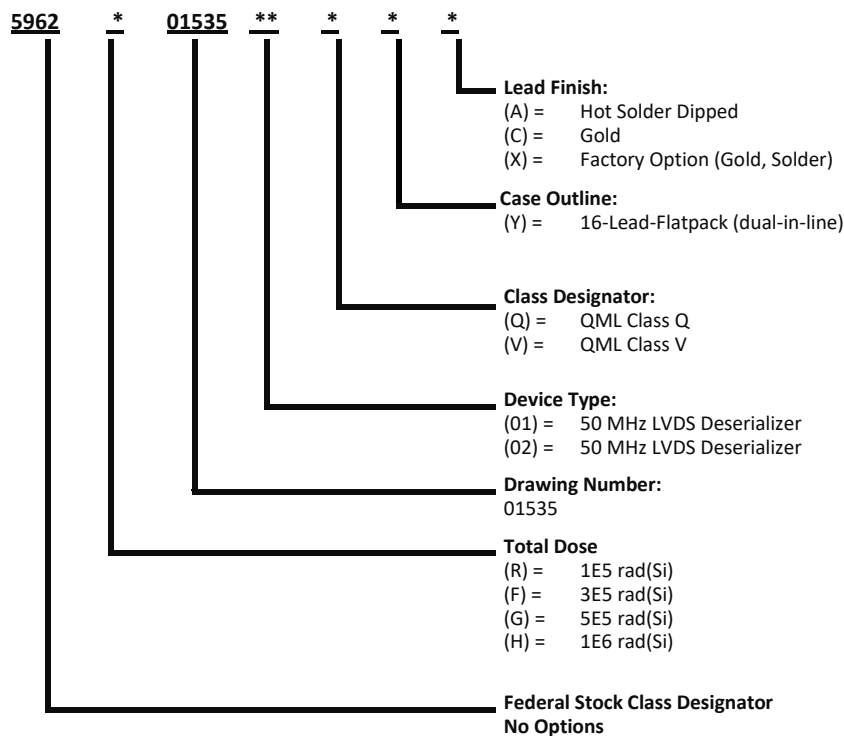
### Frontgrade Part Numbering Ordering Information



#### Notes:

- Lead finish (A, C, or X) must be specified.
- If and "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- Prototype Flow per Frontgrade Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY Radiation neither tested nor guaranteed.
- HiRel Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -55°C room temp, and 125°C. Radiation neither tested nor guaranteed.

### SMD Part Number Ordering Information



#### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.



## Revision History

Date	Revision #	Author	Change Description	Page #
10-08	1.0.0	MM	Last official release	
9-17-15	1.0.1	MM	Page 1, added package weight. Applied new Frontgrade Data Sheet template to the document.	p. 1
8-16-21	1.0.2	BM	Added HBM ESD Rating: AMR Table, p.4	p. 4
9-22-21	1.0.3	BM	SEL Limit sign, p.1, 4	p. 1, 4

## Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the <b>datasheet is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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