FRONTGRADE

DATASHEET

UT54ALVC2525

Clock Driver 1 to 8 Minimum Skew

2/1/2016

Version #: 1.0.0

Features

- 2.0V to 3.6V Power supply operation
- Guaranteed pin-to-pin and part-to-part skew • Eight LVTTL outputs with high drive strength
- Operational environment:
  - > Total-dose tolerance: 100 to 300 krad(Si), or 1 Mrad(Si)
  - > SEL Immune to a LET of 111 MeV-cm2/mg • HiRel temperature range: -55℃ to +125℃
- Packaging options:
- 14-Lead Ceramic Flatpack
- Standard Microcircuit Drawing: 5962-06233
  - > QML Q and V

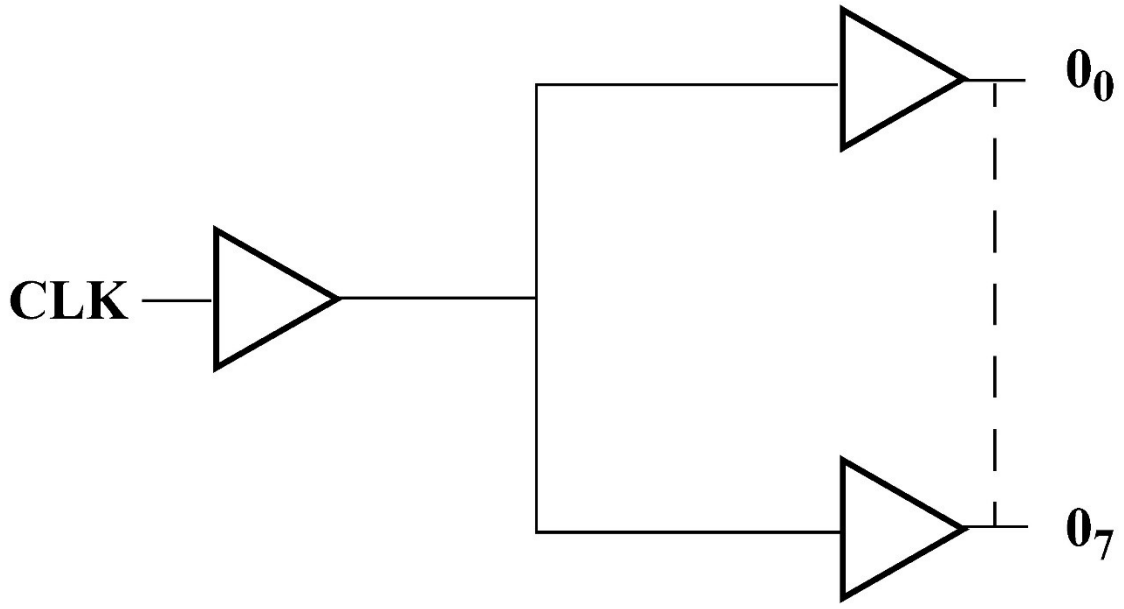


Figure 1: UT54ALVC2525 Block Diagram

Introduction

The UT54ALVC2525 is a low-voltage, minimum skew, one-to-eight clock driver. The UT54ALVC2525 distributes a single clock to eight, high-drive, outputs with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions making it ideal for signal generation and clock distribution. The output pins act as a single entity and will follow the state of the CLK pin.

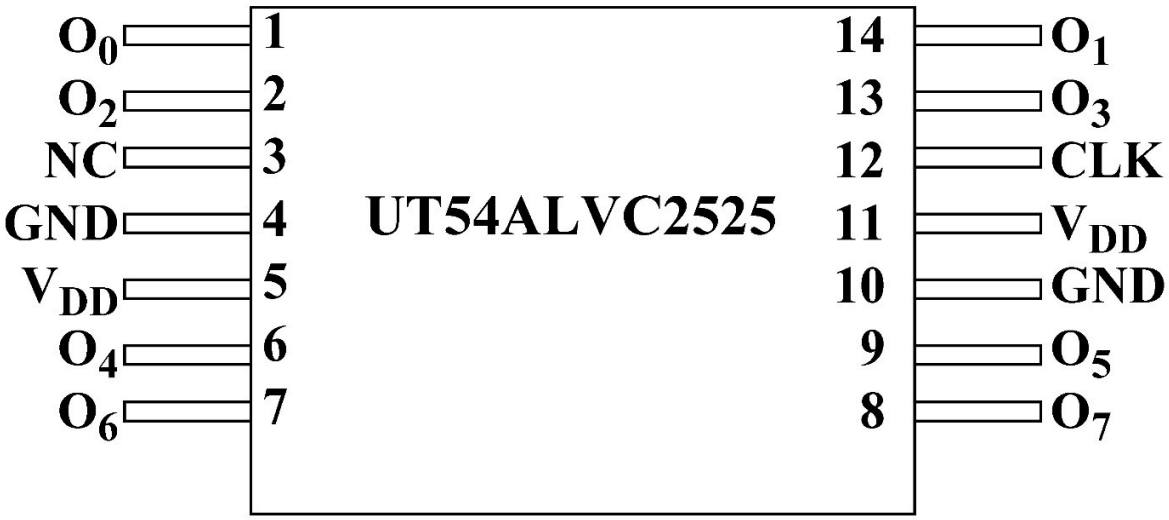


Figure 2. 14-Lead Ceramic Flatpack Pinouts

Pin Description

Flatpack Pin No.	Name	I/O	Type	Description
12	CLK	I	LVTTL	Primary reference clock input. This pin must be driven by an LVTTL or LVCMOS clock source.
3	N/C	--	--	No connect.
1, 2, 6, 7, 8, 9, 13, 14	On	O	LVTTL	Eight output clocks.
5, 11	V_{DD}	PWR	Power	Power supply for internal circuitry and output buffers.
4, 10	VSS	PWR	Power	Ground

Operational Environment

The UT54ALVC2525 incorporates special design, layout, and process features which allows operation in a limited HiRel environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	>1E6	rads(Si)
Single Event Latchup (SEL)[1, 2]	>111	MeV-cm²/mg
Onset Single Event Upset (SEU) LET (@2.0V)[3, 5]	52	MeV-cm²/mg
Onset Single Event Upset (SEU) LET (@3.0V) [4, 5]	66	MeV-cm²/mg
Neutron Fluence	1.0E14	n/cm²
Dose Rate Upset	TBD	rads(Si)/sec
Dose Rate Survivability	TBD	rads(Si)/sec

Notes:

1. The UT54ALVC2525 is latchup immune to particle LETs >111 MeV-cm2/mg.
2. SEL temperature and voltage conditions of TC = +125°C, V_{DD} = 3.6V.
3. SEU temperature and voltage conditions of TC = +25°C, V_{DD} = 2.0V. Tested at 200MHz.
4. SEU temperature and voltage conditions of TC = +25°C, V_{DD} = 3.0V. Tested at 200MHz.
5. For the UT54ALVC2525 SET performance at select operating frequency data ranges, please contact the factory.

Absolute Maximum Ratings:[1]

(Referenced to V_{SS})

Symbol	Description	Limits	Units
V_{DD}	Core Power Supply Voltage	-0.3 to 4.0	V
V_{IN}	Voltage Any Clock Input	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Voltage Any Clock Output	-0.3 to V_{DD} + 0.3	V
I_I	DC Input Current	±10	mA
P_D	Maximum Power Dissipation	1	W
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Maximum Junction Temperature 2	+150	°C
Θ_{JC}	Thermal Resistance, Junction to Case	20	°C/W
ESD_{HBM}	ESD Protection (Human Body Model) - Class II	>3000	V

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.

Recommended Operating Conditions:

Symbol	Description	Limits	Units
V_{DD}	Core Operating Voltage	2.0 to 3.6	V
V_{IN}	Voltage Clock Input	0 to V_{DD}	V
V_{OUT}	Voltage Any Clock Output	0 to V_{DD}	V
T_C	Case Operating Temperature	-55 to +125	°C

Electrical Characteristics (Pre- and Post-Radiation)*
(V_{DD} = 2.0V to 3.6V; TC = -55°C to +125°C)

Symbol	Description	Conditions		V_{DD}	MIN	MAX	Units
V_{IH}[1]	High level input voltage			2.0V 2.75V 3.0V 3.6V	1.25 1.5 1.75 2.0		V
V_{IL}[1]	Low level input voltage			2.0V 2.75V 3.0V 3.6V		0.7 0.8 0.8 0.8	V
V_{OL}	Low level output voltage	I_{OL} = 12mA I_{OL} = 12mA I_{OL} = 12mA I_{OL} = 12mA		2.0V 2.75V 3.0V 3.6V		0.45 0.4 0.4 0.4	V
V_{OH}	High level output voltage	I_{OH} = -12mA I_{OH} = -12mA I_{OH} = -12mA I_{OH} = -12mA		2.0V 2.75V 3.0V 3.6V	1.5 2.2 2.4 3.0		V
I_{OS}[2]	Short-circuit output current	V_{OUT} = V_{DD} and V_{SS}		2.0V 3.6V	-200 -300	200 300	mA
I_{IL}	Input leakage current	V_{IN} = V_{DD} or V_{SS}		3.6V	-1	1	µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}		2.0V 3.6V		1.0 1.0	mA
P_{TOTAL}[3]	Total power dissipation	CL = 20pF		2.0V 2.75V 3.0V 3.6V		1.2 2.7 3.5 5.2	mW/ MHz
C_{IN}[4]	Input capacitance	ƒ = 1MHz		0V		15	pF
C_{OUT}[4]	Output capacitance	ƒ = 1MHz		0V		15	pF

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).

1. Functional tests are conducted in accordance with MIL-STD-883 with the following test conditions: VIH=VIH(min) +20%, -0% VIL=VIL(max)+0%, -50%, as specified herein for the LVTTL and LVCMOS inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to VIH(min), VIL (max).
2. Supplied as a design limit. Neither guaranteed nor tested.
3. When measuring the dynamic supply current, all outputs are loaded in accordance with the equivalent test load defined in figure 3.
4. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and the VSS at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

AC Electrical Characteristics (Pre- and Post-Radiation)* (V_{DD} = 2.0V to 3.6V; TC = -55°C to +125°C)

Symbol	Description	Condition	V_{DD}	MIN	MAX	Unit
t_R, t_F[3]	Input rise/fall time	V_{IH} (min) - V_{IL} (max)	3.6V		20	ns/V
t_{PHL}[1,2]	Propagation delay: CLK to On, high-to-low transition	Measured as transition time between V_{IN} = V_{DD}÷2 to V_{OUT} = V_{DD}÷2	2.0V 2.75V 3.0V 3.6V	3.5 3.0 2.75 2.25	7.5 5.5 5.25 4.75	ns
t_{PLH}[1,2]	Propagation delay: CLK to On, low-to-high transition	Measured as transition time between VIN = V_{DD}÷2 to V_{OUT} = V_{DD}÷2	2.0V 2.75V 3.0V 3.6V	3.25 2.75 2.5 2.0	7.25 5.25 5.0 4.5	ns
t_{OSHL}[2,4,5]	Maximum skew: common edge, output-to-output, high-to-low transition	Measured as V_{On} = V_{DD} ÷2 to V_{Om} = V_{DD}÷2 where *n,m* = 0 to 7; *n* not equal to *m* @ f_{CLK} = 200MHz	2.0V 3.6V		0.15 0.25	ns
tOSLH 2, 4, 5	Maximum skew: common edge, output-to-output, low-to-high transition	Measured as V_{On}= V_{DD} ÷2 to V_{Om}= V_{DD}÷2 where *n,m* = 0 to 7; *n* not equal to *m* @ fCLK = 200MHz	2.0V 3.6V		0.15 0.25	ns
tORISE & 3 tOFALL	Output rise/fall time	Measured as transition time between 20% * V_{OL} and 80% * V_{OH} @ fCLK = 100MHz	2.0V 3.6V		2.4 2.0	ns
tPART 4, 5	Part-part skew	Skew between the same output of any two devices under identical settings and conditions (V_{DD}, temp, air flow, frequency, etc).	2.0V 3.6V		0.1 0.15	ns
tPBAL 1, 4	Propagation delay balance: difference between same output, low-to-high and high-to-low transitions	Measured as transition time between V_{IN} = V_{DD}÷2 to VOUT = V_{DD}÷2	2.0V 2.75V 3.0V 3.6V		0.43 0.3 0.26 0.21	ns

Notes:

*Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).

1. Test load = 40pF, terminated to V_{DD}÷2. All outputs are equally loaded. Reference Figure 3 for clock output loading.
2. Reference Figure 4 for AC timing diagram.
3. Supplied only as a design guideline, neither tested nor guaranteed.
4. Guaranteed by characterization, but not tested.
5. Test load = 40pF, terminated to V_{DD}÷2. All outputs are equally loaded. Reference Figure 5 for clock output loading.

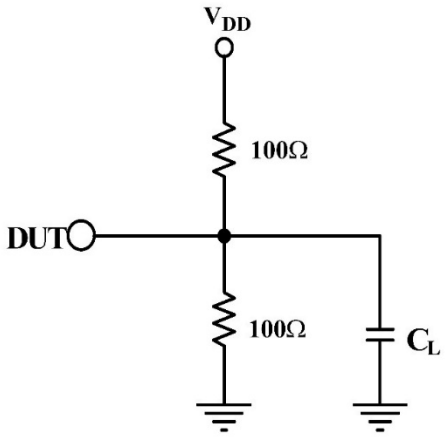


Figure 3. Test Load Circuit for Dynamic Power Supply Current and AC Measurements

Note:

1. This is not the recommended termination for normal user operation.

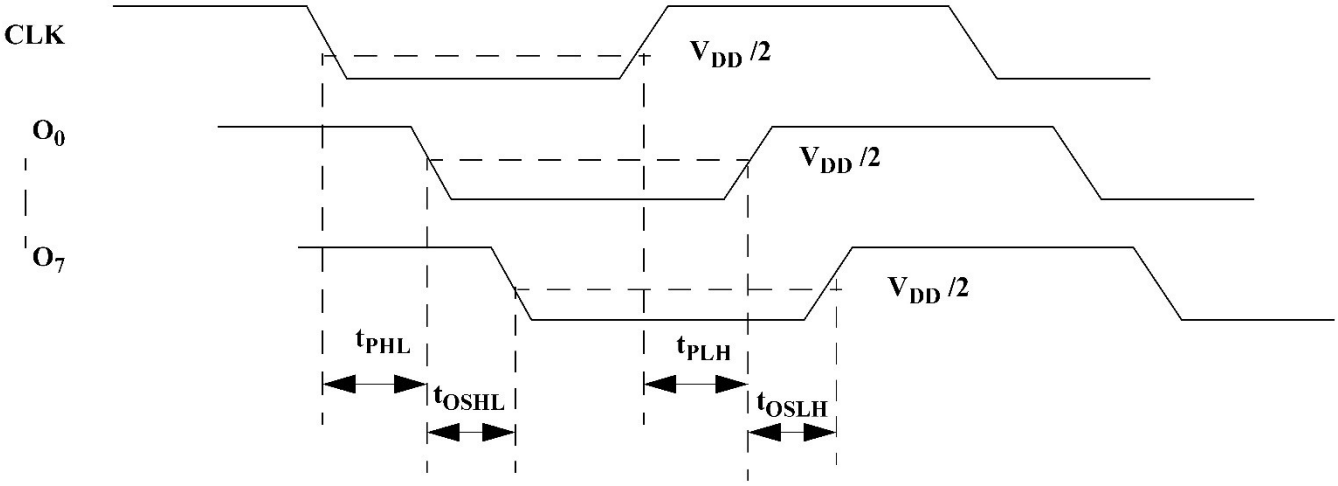


Figure 4. AC Timing Diagram

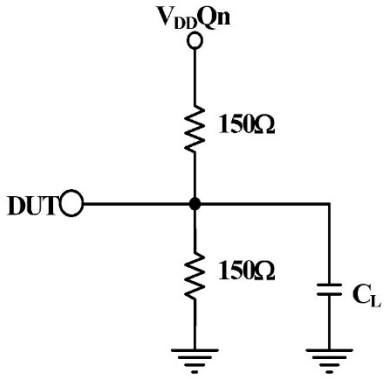


Figure 5. Test Load Circuit for tOSHL and tOSLH Measurements

Packaging

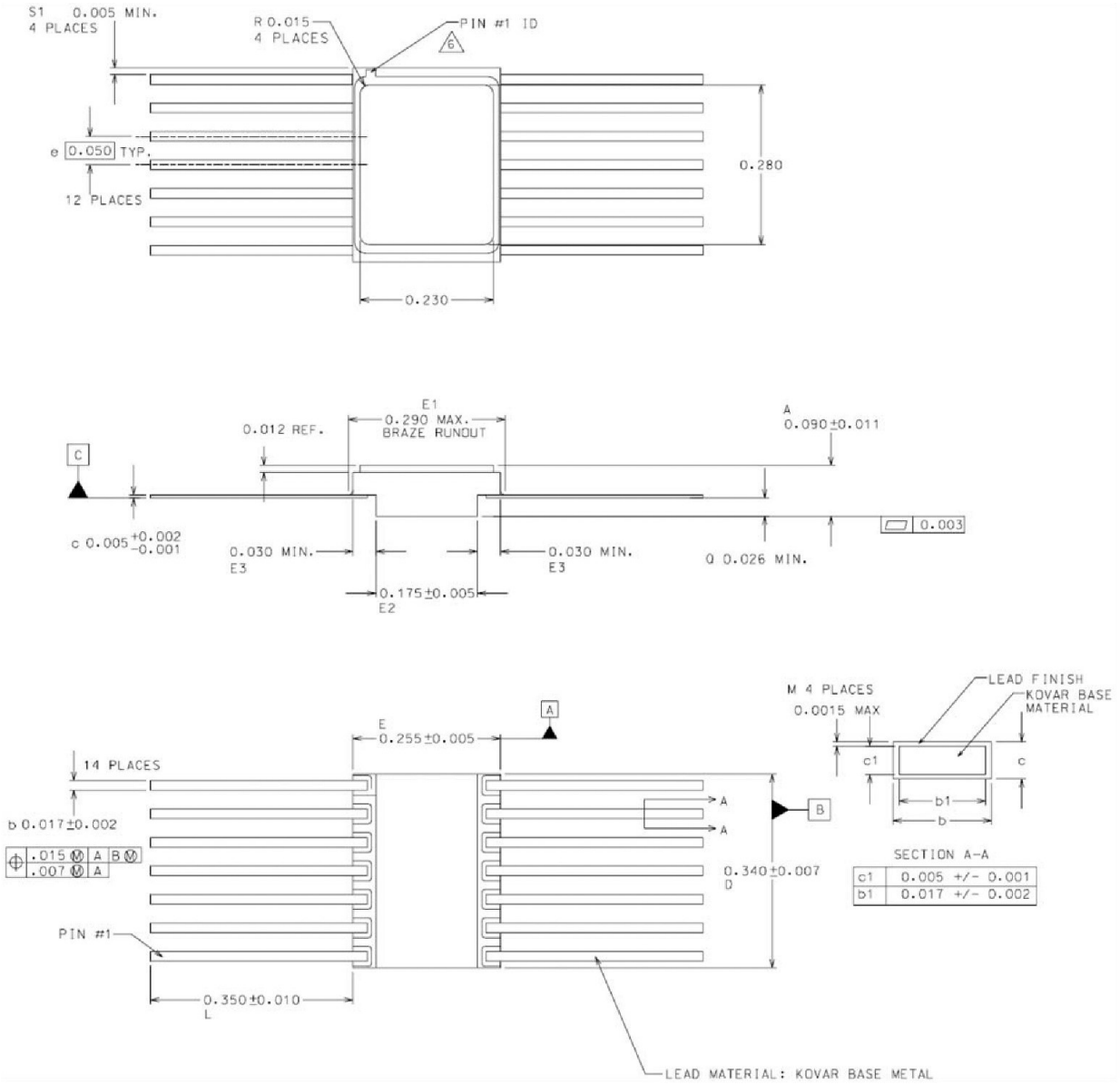


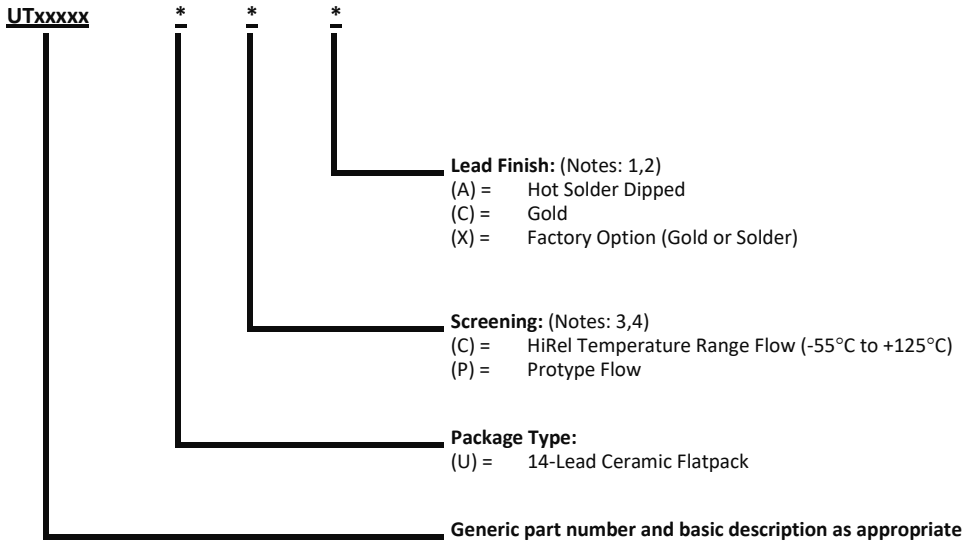
Figure 6. 14-Pin Flatpack Package

Notes:

1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.
6. ID mark symbol is vendor option.

Ordering Information

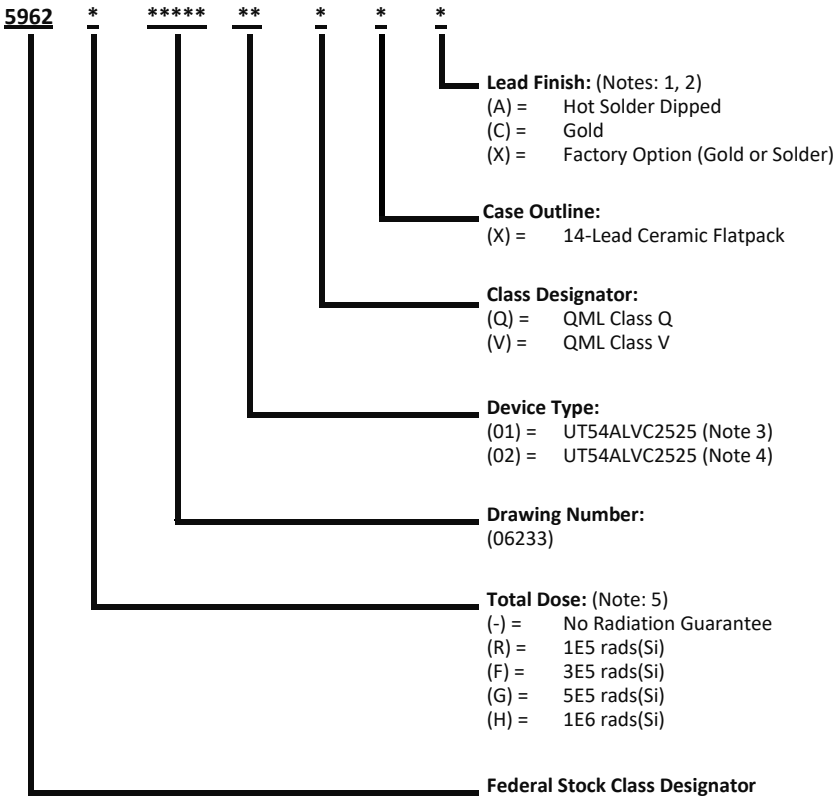
UT54ALVC2525:



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per CAES Manufacturing Flows Document. Tested at 25℃ only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55℃, room temp, and 125℃. Radiation neither tested nor guaranteed.

UT54ALVC2525: SMD



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold)
3. Available to a maximum RHA level of H.
4. Available to a maximum RHA level of R. Device is irradiated at a dose rate = 50-300 rads(Si)/s in accordance with MIL-STD-883, Method 1019, Condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rads(Si)/s per MIL-STD-883, Method 1019, Condition A, section 3.11.2. The total dose specification for these devices only applies to a low dose rate environment.
5. Total dose radiation must be specified when ordering. QML Q and QML V are not available without radiation hardening.

Revision History

Date	Revision #	Author	Change Description	Page #
2-16	1.0.0	BM	Added datasheet template	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.