FRONTGRADE

DATASHEET

UT54ACS164E/UT54ACTS164E

8-Bit Shift Registers

1/15/2018
Version #: 1.0

Features

- AND-gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Direct clear
- 0.6µm CRH CMOS Process
  - > Latchup immune
- High speed
- Low power consumption
- Wide operating power supply from 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack
- UT54ACS164E - SMD - 5962-96556
- UT54ACT164E - SMD - 5962-96557

Description

The UT54ACS164E and the UT54ACTS164E are 8-bit shift registers which feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high-level at both serial inputs sets the first flip-flop to the high level at the next clock pulse. Data at the serial inputs may be changed while the clock is high or low, providing the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

The devices are characterized over the full HiRel temperature range of -55℃ to +125℃.

Pinout

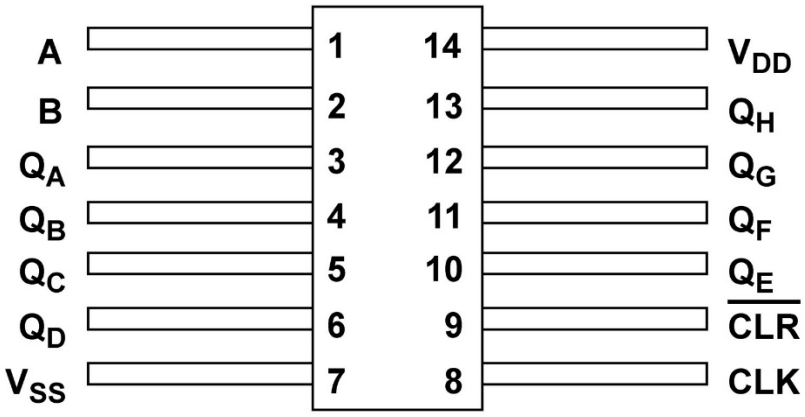


Figure 1: 14-Lead Flatpack
Top View

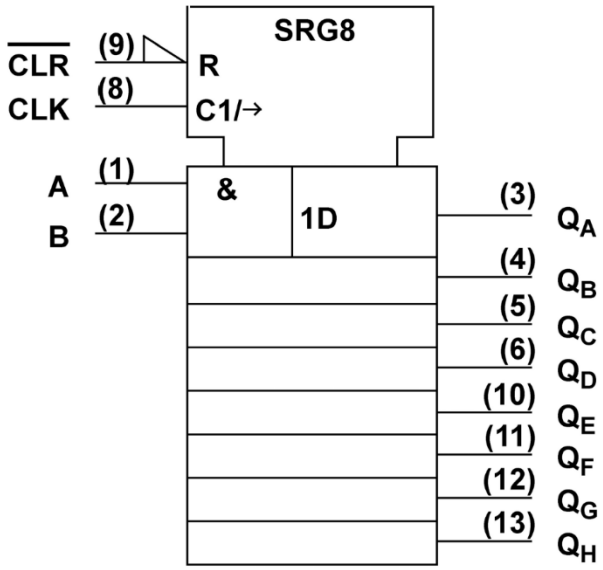
Function Table

Inputs				Outputs			
$\overline{CLR}$	CLK	A	B	QA	QB	...	QH
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{HO}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

Notes:

1. QA0, QB0, QH0 = the level of QA, QB or QH, respectively, before the indicated steady-state input conditions were established.
2. QAn and QGn = the level of QA or QG before the most recent - transition of the clock; indicates a one-bit shift.

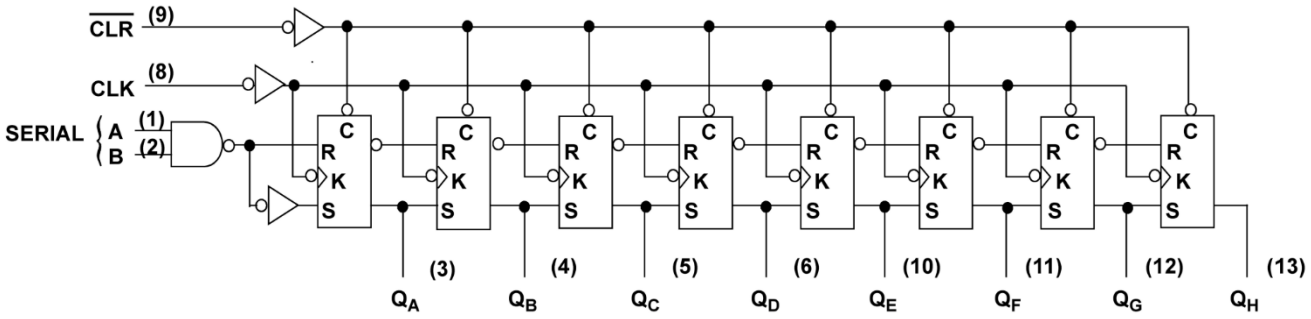
Logic Symbol



Note:

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Diagram



Operational Environment[1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold[2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15.0	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	℃

DC Electrical Characteristics for the UT54ACS164E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55℃ < T_C < +125℃)

Symbol	Parameter		Condition	VDD	MIN	MAX	Unit
V_{IL}	Low-level input voltage[1]			3.0V		0.9	V
				5.5V		1.65	
V_{IH}	High-level input voltage[1]			3.0V	2.1		V
				5.5V	3.85		
I_{IN}	Input leakage current		V_{IN} = V_{DD} or V_{SS}	5.5V	-1	1	µA
V_{OL}	Low-level output voltage[3]		I_{OL} = 100µA	3.0V		0.25	V
				4.5V		0.25	
V_{OH}	High-level output voltage[3]		I_{OH} = -100µA	3.0V	2.75		V
				4.5V	4.25		
I_{OS}	Short-circuit output current[2,4]		V_O = V_{DD} and V_{SS}	3.0V	-100	100	mA
				5.5V	-200	200	
I_{OL}	Low level output current[9]		V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	3.0V	6		mA
				5.5V	8		
I_{OH}	High level output current[9]		V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V	3.0V		-6	mA
				5.5V		-8	
P_{total}	Power dissipation[2,8]		C_L = 50pF	5.5V		1.9	mW/MHz
				3.0V		0.76	
I_{DDQ}	Quiescent Supply Current	Pre-Rad All Device Types	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX	5.5V		10	µA
		Post-rad Device Type - 03		5.5V		50	
		Post-Rad Device Type - 02		5.5V		130	
C_{IN}	Input capacitance[5]		f = 1MHz	0V		15	pF
C_{OUT}	Output capacitance[5]		f = 1MHz	0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, -0\%$; $V_{IL} = V_{IL}(max) + 0\%, -50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si), and 1E6 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
8. Power dissipation specified per switching output.
9. This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics for the UT54ACS164E[2]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[1], -55°C < T_C < +125°C)

Symbol	Parameter	Condition	VDD	Minimum	Maximum	Unit
t_{PHL1}	CLK to Qn	C_L = 30pF	3.0V & 3.6V	4	21	ns
			4.5V & 5.5V	4	17	
		C_L = 50pF	3.0V & 3.6V	4	25	ns
			4.5V & 5.5V	4	21	
t_{PLH1}	CLK to Qn	C_L = 30pF	3.0V & 3.6V	2	18	ns
			4.5V & 5.5V	2	14	
		C_L = 50pF	3.0V & 3.6V	2	22	ns
			4.5V & 5.5V	2	18	
t_{PHL2}	$\overline{CLR}$ to Qn	C_L = 30pF	3.0V & 3.6V	5	21	ns
			4.5V & 5.5V	5	17	
		C_L = 50pF	3.0V & 3.6V	5	25	ns
			4.5V & 5.5V	5	21	
f_{MAX}	Maximum clock frequency	C_L = 50pF	3.0V, 4.5V, and 5.5V		83	MHz
t_{SU1}	Data setup time before CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	4		ns
t_{SU2}	$\overline{CLR}$ inactive Setup time before CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	4		ns
t_H[3]	Data hold time after CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	2		ns
t_W	Minimum pulse width $\overline{CLR}$ low CLK high CLK low	C_L = 50pF	3.0V, 4.5V, and 5.5V	6		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) and 1E6 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
3. Based on characterization, hold time (tH) of 0ns can be assumed if data setup time (tSU1) is ≥10ns. This is guaranteed, but not tested.

DC Electrical Characteristics for he UT54ACTS164E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < T_C < +125°C)

Symbol	Parameter		Condition	VDD	MIN	MAX	Unit
V_{IL}	Low-level input voltage[1]			3.0V		0.8	V
				5.5V		0.8	
V_{IH}	High-level input voltage[1]			3.0V	2.0		V
				5.5V	2.75		
I_{IN}	Input leakage current		V_{IN} = V_{DD} or V_{SS}	5.5V	-1	1	µA
V_{OL}	Low-level output voltage[3]		I_{OL} = 6mA	3.0V		0.4	V
			I_{OL} = 8mA	4.5V		0.4	V
V_{OH}	High-level output voltage[3]		I_{OL} = -6mA	3.0V	2.4		V
			I_{OL} = -8mA	4.5V	3.15		V
I_{OS}	Short-circuit output current[2,4]		V_O = V_{DD} and V_{SS}	3.0V	-100	100	mA
				5.5V	-200	200	
I_{OL}	Low level output current[10]		V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	3.0V	6		mA
				5.5V	8		
I_{OH}	High level output current[10]		V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V	3.0V		-6	mA
				5.5V		-8	
P_{total}	Power dissipation[2,8,9]		C_L = 50pF	5.5V		1.9	mW/MHz
				3.0V		0.76	
I_{DDQ}	Quiescent Supply Current	Pre-Rad All Device Types	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX			10	µA
		Post-rad Device Type - 03		5.5V		50	
		Post-Rad Device Type - 02		5.5V		130	
ΔI_{DDQ}	Quiescent Supply Current Delta		For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS}	5.5V		1.6	mA
C_{IN}	Input capacitance[5]		f = 1MHz	0V		15	pF
C_{OUT}	Output capacitance[5]		f = 1MHz	0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, -0\%$; $V_{IL} = V_{IL}(max) + 0\%, -50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density £5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si), and 1E6 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
8. Power does not include power contribution of any TTL output sink current
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics for the UT54ACTS164E[2]

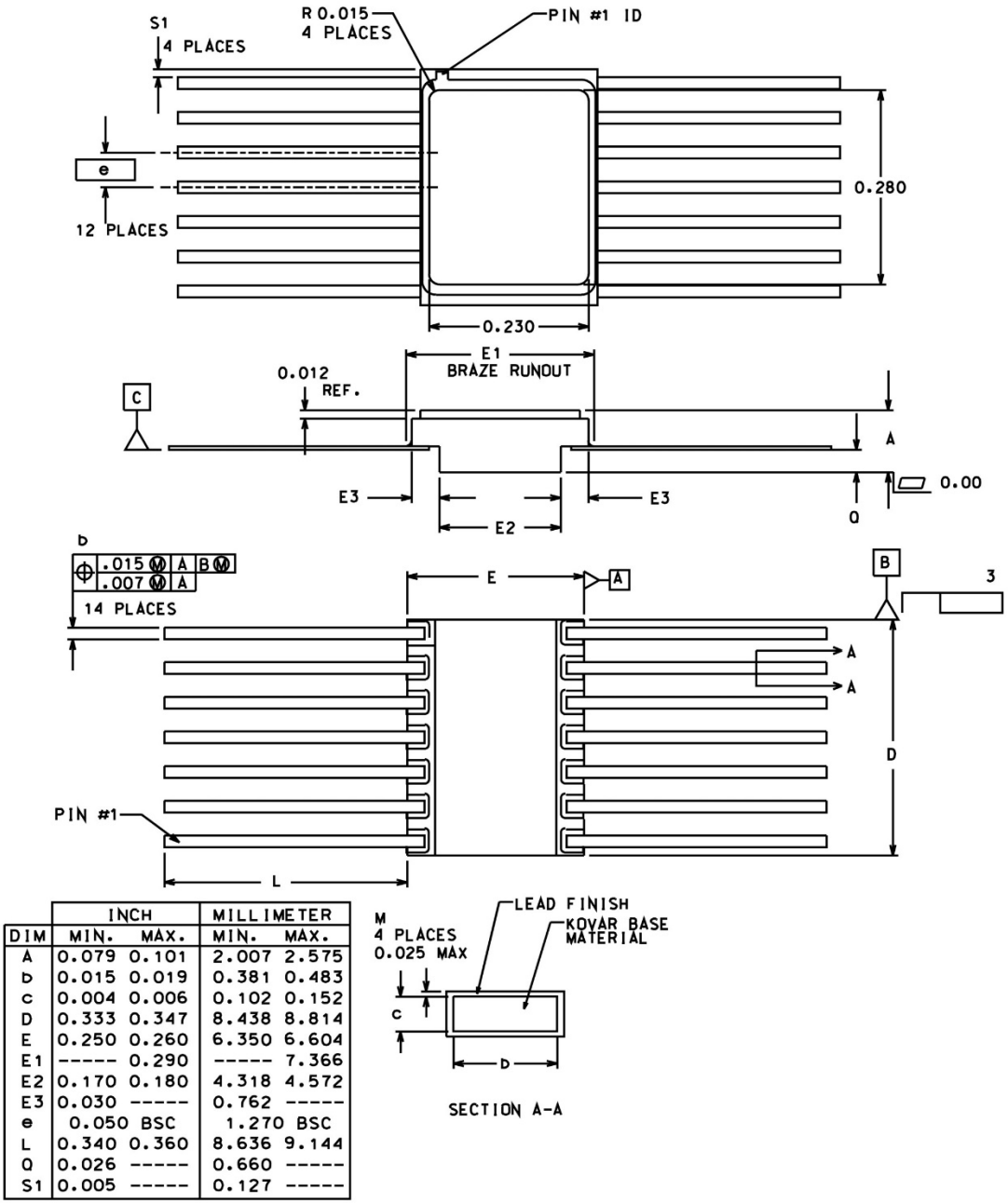
(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[1]; -55°C < T_C < +125°C)

Symbol	Parameter	Condition	V_{DD}	Minimum	Maximum	Unit
t_{PHL1}	CLK to Qn	C_L = 30pF	3.0V & 3.6V	4	21	ns
			4.5V & 5.5V	4	17	
		C_L = 50pF	3.0V & 3.6V	4	25	ns
			4.5V & 5.5V	4	21	
t_{PLH1}	CLK to Qn	C_L = 30pF	3.0V & 3.6V	2	18	ns
			4.5V & 5.5V	2	14	
		C_L = 50pF	3.0V & 3.6V	2	22	ns
			4.5V & 5.5V	2	18	
t_{PHL2}	$\overline{CLR}$ to Qn	C_L = 30pF	3.0V & 3.6V	5	21	ns
			4.5V & 5.5V	5	17	
		C_L = 50pF	3.0V & 3.6V	5	25	ns
			4.5V & 5.5V	5	21	
f_{MAX}	Maximum clock frequency	C_L = 50pF	3.0V, 4.5V, and 5.5V		83	MHz
t_{SU1}	Data setup time before CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	4		ns
t_{SU2}	$\overline{CLR}$ inactive setup time before CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	4		ns
t_H[3]	Data hold time after CLK ↑	C_L = 50pF	3.0V, 4.5V, and 5.5V	2		ns
t_W	Minimum pulse width $\overline{CLR}$ low CLK high CLK low	C_L = 50pF	3.0V, 4.5V, and 5.5V	6		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si), and 1E6 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
3. Based on characterization, hold time (tH) of 0ns can be assumed if data setup time (tSU1) is ≥10ns. This is guaranteed, but not tested.

Packaging



DIM	INCH MIN.	INCH MAX.	MILLIMETER MIN.	MILLIMETER MAX.
A	0.079	0.101	2.007	2.575
b	0.015	0.019	0.381	0.483
c	0.004	0.006	0.102	0.152
D	0.333	0.347	8.438	8.814
E	0.250	0.260	6.350	6.604
E1	-----	0.290	-----	7.366
E2	0.170	0.180	4.318	4.572
E3	0.030	-----	0.762	-----
e	0.050 BSC		1.270 BSC	
L	0.340	0.360	8.636	9.144
Q	0.026	-----	0.660	-----
S1	0.005	-----	0.127	-----

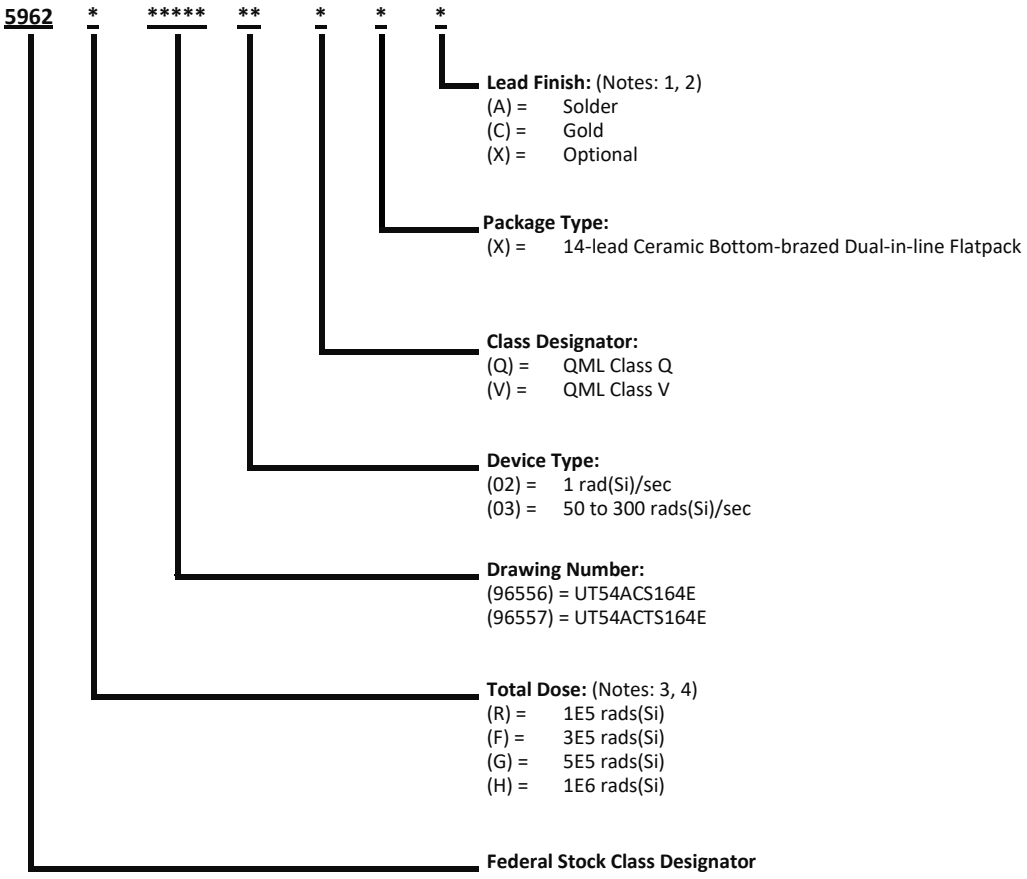
Figure 2: Figure 1. 14-lead Flatpack

Notes:

1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533. 5) Lead position and colanarity are not measured.

Ordering Information

UT54ACS164E/UT54ACTS164E SMD Part Number Ordering Information



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #
10/17		RT	Edited IDDQ Applied new Frontgrade Data Sheet template to the document.	4, 6
1/18		RT	Updates to reflect current SMD	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.