FRONTGRADE

DATASHEET

UT54ACTQ16374

RadHard CMOS 16-bit D Flip-Flop TTL Inputs, and Three-State Outputs

5/16/2012
Version #: 1.0

Features

- 16 non-inverting D flip-flops with three-state outputs
- Guaranteed simultaneously switching noise level and dynamic threshold performance
- Buffered positive edge-triggered clock
- Separate control logic for each byte
- Guaranteed pin-to-pin output skew
- 0.6µm Commercial RadHard™ CMOS
  - > Total dose: 100K rad(Si)
  - > Single Event Latchup immune
  - > SEU Onset LET >95 MeV -cm^2/mg
- High speed, low power consumption
- Output source/sink 24mA
- Standard Microcircuit Drawing 5962-06245
  - > QML compliant part
- Package:
  - > 48-lead flatpack, 25 mil pitch (.390 x .640)

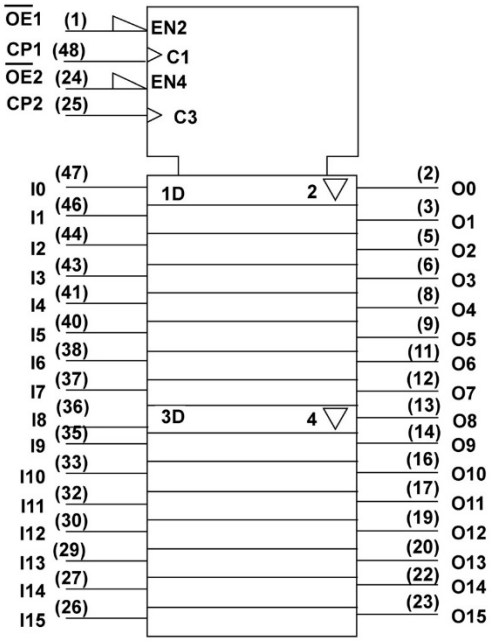
Description

The 16-bit wide UT54ACTQ16374 D flip-flop is built using Frontgrade Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high-speed, low power UT54ACTQ16374 D flip-flop is designed for bus-oriented applications. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 16-bit operation. The UT54ACTQ16374 are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers and working registers. Each flip-flop will store the state of their individual D inputs (In) that meet the setup and hold requirements on the low-to-high clock (CPn) transition. With the Output Enable ($\overline{OE}$n) low, the contents of the flip-flops are available at the output. When $\overline{OE}$n is high, the outputs go to high impedance state. Operation of $\overline{OE}$n input does not affect the state of the D flip-flops.

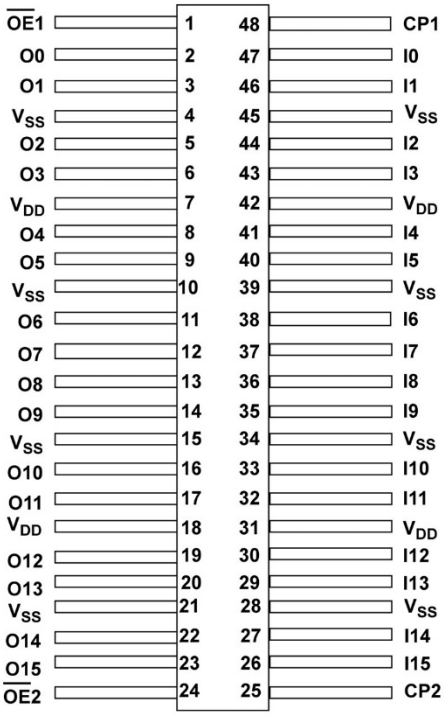
Pin Description

Pin Names	Description
$\overline{OE}$n	Output Enable Input (Active Low)
CPn	Clock Pulse Input
I0-I15	Inputs
O0-O15	Outputs

Logic Symbol



Pinouts



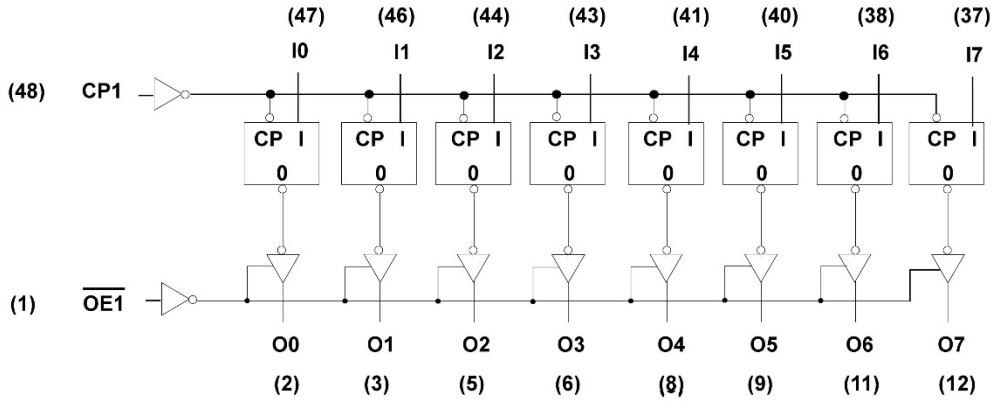
48-Lead Flatpack
Top View

Function Table

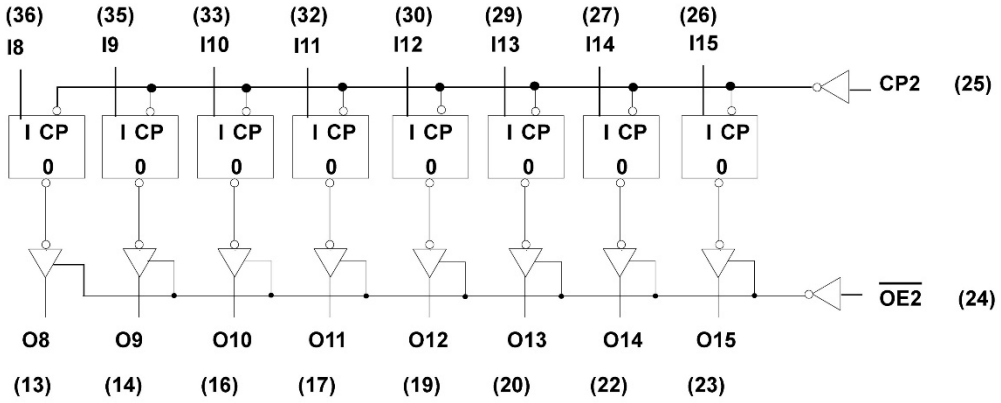
Inputs			Output	Operation
$\overline{OE}$n	CPn	In	On	
H	H	L	Z	Hold
H	H	H	Z	Hold
H	↑	L	Z	Load
H	↑	H	Z	Load
L	↑	L	L	Data Available
L	↑	H	H	Data Available
L	H	L	Qo	No change in data
L	H	H	Qo	No change in data

Logic Diagram

BYTE 1 (0:7)



BYTE 2 (8:15)



Radiation Hardness Specifications[1]

Parameter	Limit	Units
Total Dose	1.0E5	rad(Si)
SEL Immune	>108	MeV-cm^2/mg
SEU Onset Let	>95	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limit (Mil only)	Units
$V_{I/O}$	Voltage any pin during operation	-.3 to V_{DD} +.3	V
V_{DD}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	310	mW

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C
t_{INRISE} t_{INFALL}	Maximum input rise or fall time (V_{IN} transitioning between V_{IL} (max) and V_{IH} (min))	20	ns

Electrical Characteristics[1]

(-55°C < T_C < +125°C)

Symbol	Parameter	Condition		MIN	MAX	Unit
V_{IL}	Low level input voltage[2]	V_{DD} from 4.5V to 5.5V			0.8	V
V_{IH}	High level input voltage[2]	V_{DD} from 4.5V to 5.5V		2.0		V
I_{IN}	Input leakage current[3]	V_{DD} from 4.5V to 5.5V V_{IN} = V_{DD} or V_{SS}		-1	1	µA
I_{OZ}	Three-state output leakage current	V_{DD} from 4.5V to 5.5V; V_{IN} = V_{DD} or V_{SS}		-10	10	µA
I_{OS}	Short-circuit output current[4,5]	V_O = V_{DD} or VSS; V_{DD} from 4.5V to 5.5V		-600	600	mA
V_{OL1}	Low-level output voltage[5]	I_{OL}=24mA I_{OL}=24mA I_{OL}= 100µA V_{IN} = 2V or 0.8V V_{DD} = 4.5V to 5.5V	-55C, 25C		0.36	V
			+125C		0.5	
			-55C, 25C +125C		0.2	
V_{OL2}	Low-level output voltage[5,6]	I_{OL}= 50mA V_{IN} = 2.0V or 0.8V V_{DD} = 5.5V	-55C, 25C		0.8	V
			+125C		1.0	
V_{OH1}	High-level output voltage[5]	I_{OH}=-24mA I_{OH}=-24mA I_{OH}= -100µA V_{IN} = 2V or 0.8V V_{DD} = 4.5V to 5.5V	-55C, 25C	V_{DD} - 0.64		V
			+125C	V_{DD} - 0.8		
			-55C, 25C +125C	V_{DD} - 0.2		
V_{OH2}	High-level output voltage[5,6]	I_{OH}= -50mA V_{IN} = 2.0V or 0.8V V_{DD} = 5.5V	-55C, 25C	V_{DD} - 1.1		V
			+125C	V_{DD} - 1.3		
V_{IC+}	Positive input clamp voltage	For input under test, I_{IN} = 18mA V_{DD} = 0.0V		0.4	1.5	V
V_{IC-}	Negative input clamp voltage	For input under test, I_{IN} = -18mA V_{DD} = open		-1.5	-0.4	V
P_{total}	Power dissipation[7,6,9]	C_L = 20pF; V_{DD} from 4.5V to 5.5V			0.5	mW/MHz
I_{DDQ}	Standby Supply Current V_{DD} Pre-Rad 25°C -55°C to +125°C Post-Rad 25°C	V_{IN}= V_{DD} or V_{SS} V_{DD} = 5.5V $\overline{OE}$n = V_{DD} $\overline{OE}$n = V_{DD} $\overline{OE}$n = V_{DD}			10 160 160	µA
ΔI_{DDQ}	Quiescent Supply Current Delta, TTL input level	For input under test: V_{IN} = V_{DD} - 2.1V For other inputs: V_{IN} = V_{DD} or V_{SS}; V_{DD} = 5.5V			1.6	mA
C_{IN}	Input capacitance[10]	*f* = 1MHz @ 0V V_{DD} from 4.5V to 5.5V			15	pF
C_{OUT}	Output capacitance[10]	*f* = 1MHz @ 0V V_{DD} from 4.5V to 5.5V			15	pF
V_{OLP} V_{OLV}	Low level V_{SS} bounce noise[11]	V_{IH} = 3.0V, V_{IL} = 0.0V, T_A=+25°C, V_{DD} = 5.0V See figure "Quiet Output Under Test			1100 -1300	mV mV
V_{OHP} V_{OHV}	High level V_{DD} bounce noise[11]				V_{OH}+1200 V_{OH} -1400	mV mV

Notes:

1. All specifications valid for radiation dose ≤1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$ (min) + 20%, - 0%; $V_{IL} = V_{IL}$ (max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Supplied as a design limit, but not guaranteed or tested.
5. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
6. Transmission driving tests are performed at V_{DD} = 5.5V, only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for $V_{IN}=V_{IH}$ minimum or V_{IL} maximum.
7. Guaranteed by characterization.
8. Power does not include power contribution of any CMOS output sink current.
9. Power dissipation specified per switching output.
10. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
11. This test is for qualification only. VSS and V_{DD} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture.

AC Electrical Characteristics[1]

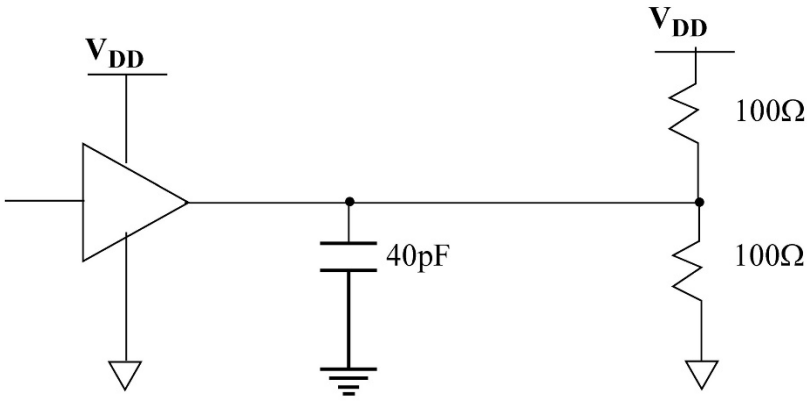
(V_{DD} = 5V ±10%; -55°C < T_C < +125°C)

Symbol	Parameter	MIN	MAX	Unit
t_{PLH}	Propagation delay CPn to On	2	10	ns
t_{PHL}	Propagation delay CPn to On	2	10	ns
t_{PZL}	Output enable time $\overline{OE}$n to On	2	9.0	ns
t_{PZH}	Output enable time $\overline{OE}$n to On	2	9.0	ns
t_{PLZ}	Output disable time $\overline{OE}$n to On high impedance	2	9.0	ns
t_{PHZ}	Output disable time $\overline{OE}$n to On high impedance	2	9.0	ns
t_{FMAX}[2]	Maximum clock frequency		100	MHz
t_S	Setup time high or low In to CPn	1.5		ns
t_H	Hold time high or low In from CPn	0.5		ns
t_W	Clock pulse, high or low CPn	5.0		ns
t_{SKEW}[3]	Output-to-output skew		1.25	ns
t_{DSKEW}[3]	Differential skew between outputs		1.5	ns
$t_{DSKEWPP}$[3,5]	Part-to-part output skew between outputs on multiple devices under identical system conditions.		500	ps

Notes:

1. All specifications valid for radiation dose ≤1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Verified by functional testing.
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs low-to-high.
4. Differential skew is defined as a comparison of any two output transitions high-to-low vs. low-to-high and low-to-high vs high-to low.
5. Guaranteed by characterization, but not tested.

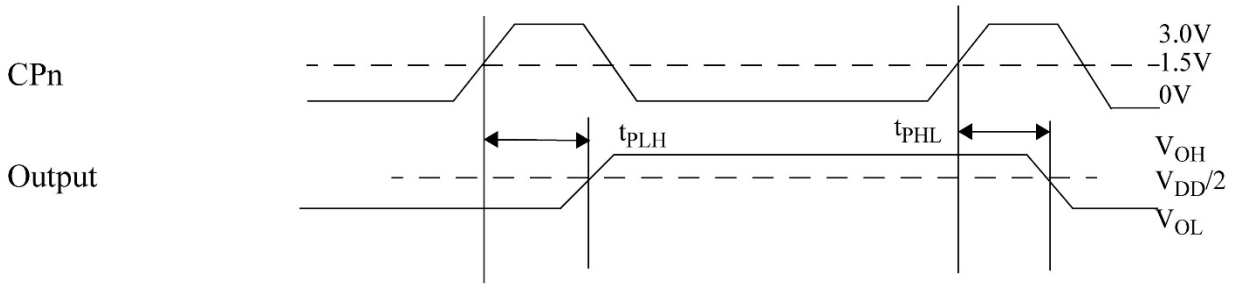
Test Load or Equivalent[1]



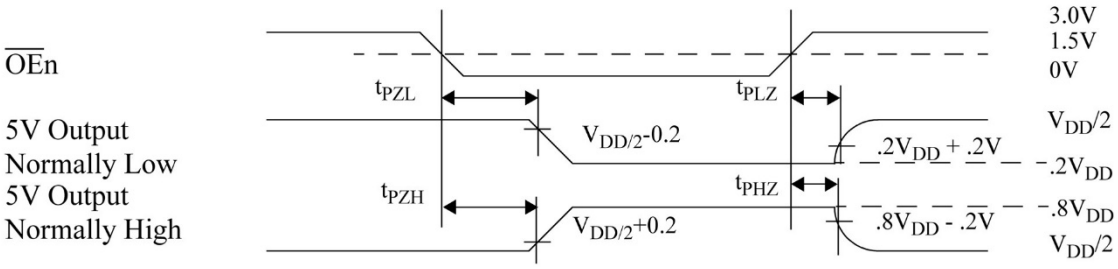
Note:

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

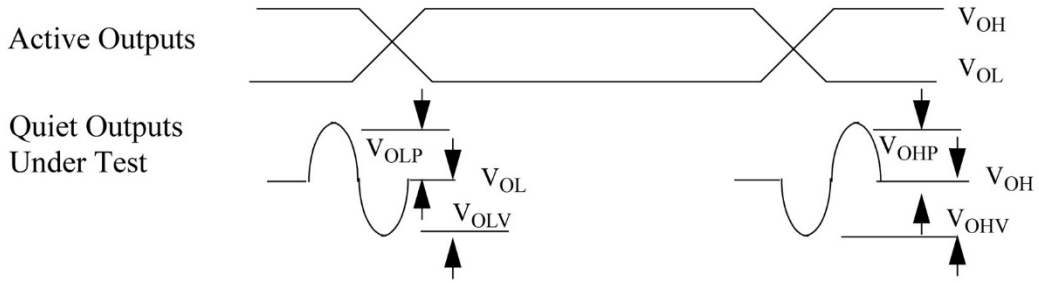
Propagation Delay



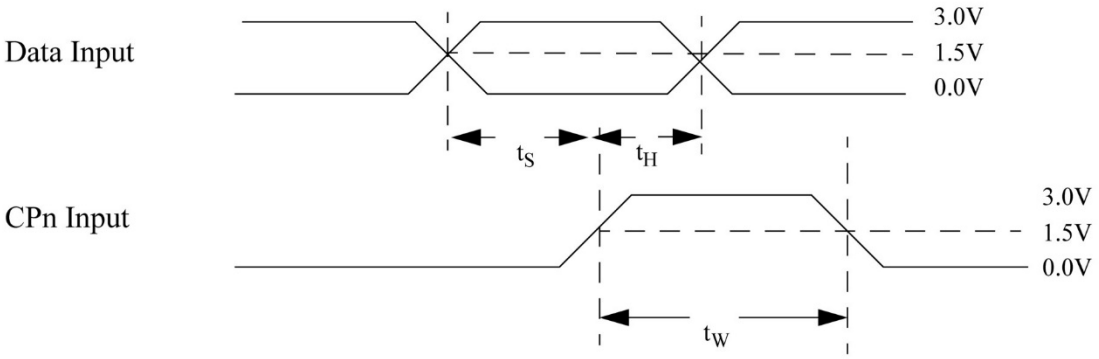
Enable Disable Times



Bounce Noise



Setup and Hold Measurements



Package

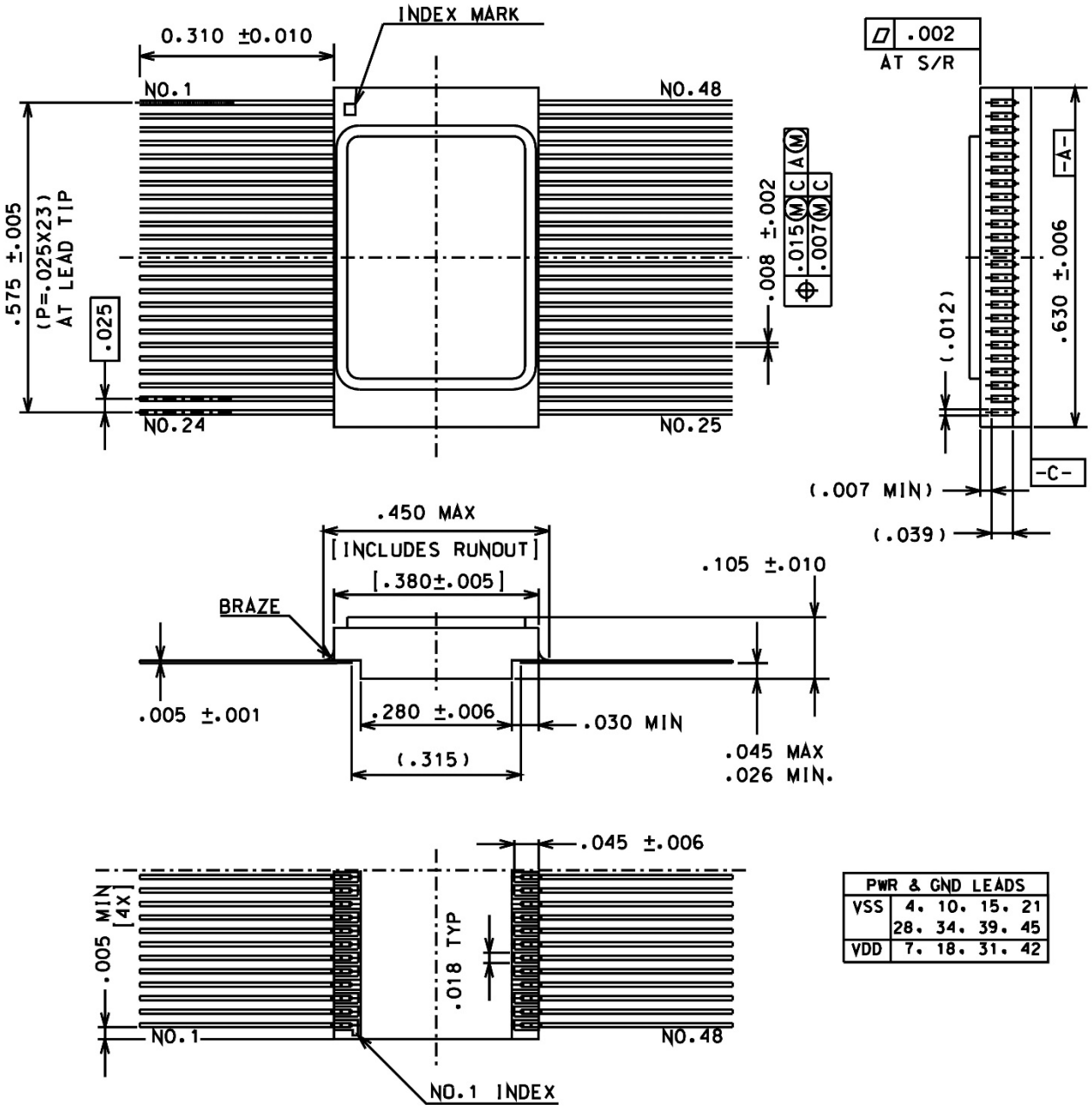


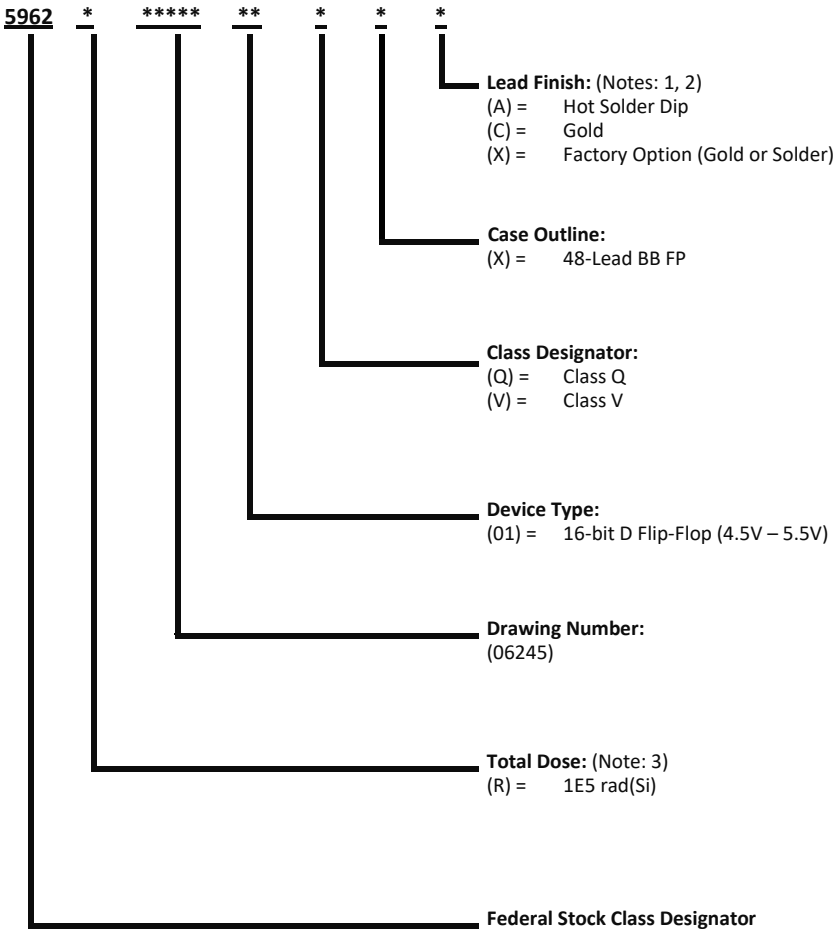
Figure 1: 48-Lead Flatpack

Notes:

1. Seal ring is connected to V_{SS}.
2. Units are in inches.
3. All exposed metalized areas must be gold plated 100 to 225 microinches thick. Dyer electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

Ordering Information

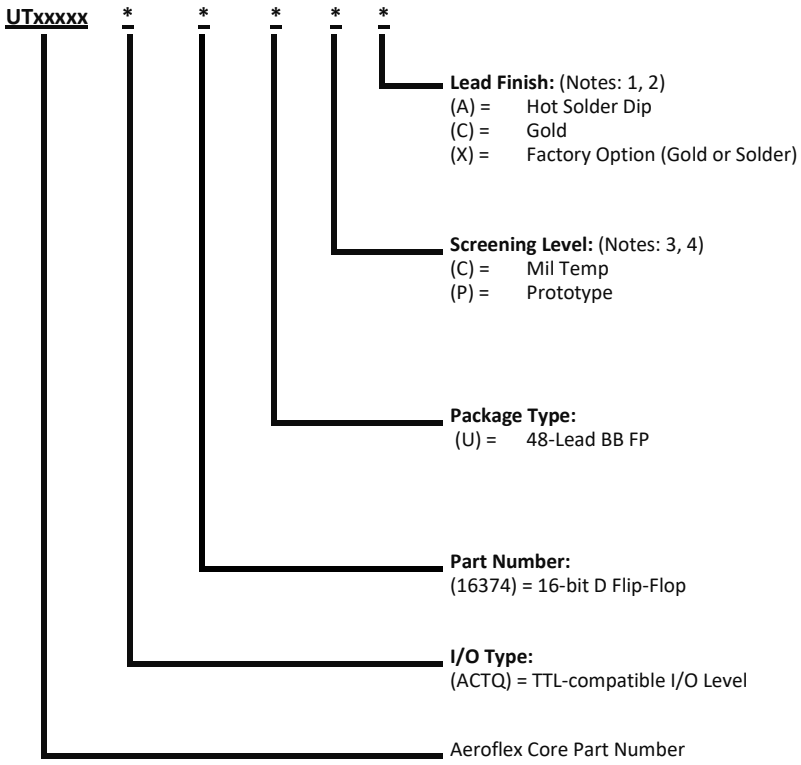
SMD Part Number Ordering Information



Notes:

1. Lead finish (A, C or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q not available without radiation hardening.

Frontgrade Part Numbering Ordering Information



Notes:

1. Lead finish (A, C or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Prototype flow per Frontgrade Manufacturing Flows Document. Tested at 25℃ only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Frontgrade Manufacturing Flows Document. Devices are tested at -55℃, room temp, and 125℃. Radiation neither tested nor guaranteed.

Revision History

Date	Revision #	Author	Change Description	Page #

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.