FRONTGRADE

DATASHEET

UT54ACS164245S/SE

Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver

4/30/2026

Version #: 1.0.1

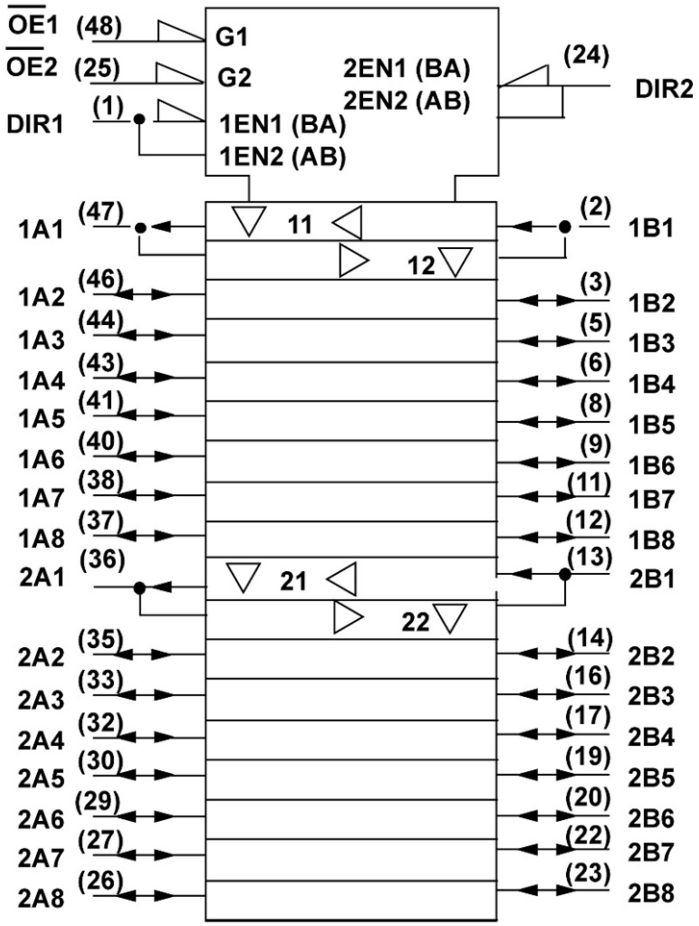
Features

- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
- Cold sparing
  - 1MΩ minimum input impedance power-off
- 0.6µm CRH CMOS Technology
- Operational environment:
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
- High speed, low power consumption
- Schmitt trigger inputs to filter noisy signals
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-98580
  - Device types 01, 02, 03, 04, 05
- Package:
  - 48-lead flatpack, 25 mil pitch (.390 x .640)

Description

The 16-bit wide UT54ACS164245S MultiPurpose transceiver is built using Frontgrade's CMOS technology and is ideal for space applications. This high speed, low power UT54ACS164245S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, and cold sparing. With V_{DD} equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 1MW making it ideal for "cold spare" applications. Balanced outputs and low "on" output impedance make the UT54ACS164245S well suited for driving high capacitance loads and low impedance backplanes. The UT54ACS164245S enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{OE}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

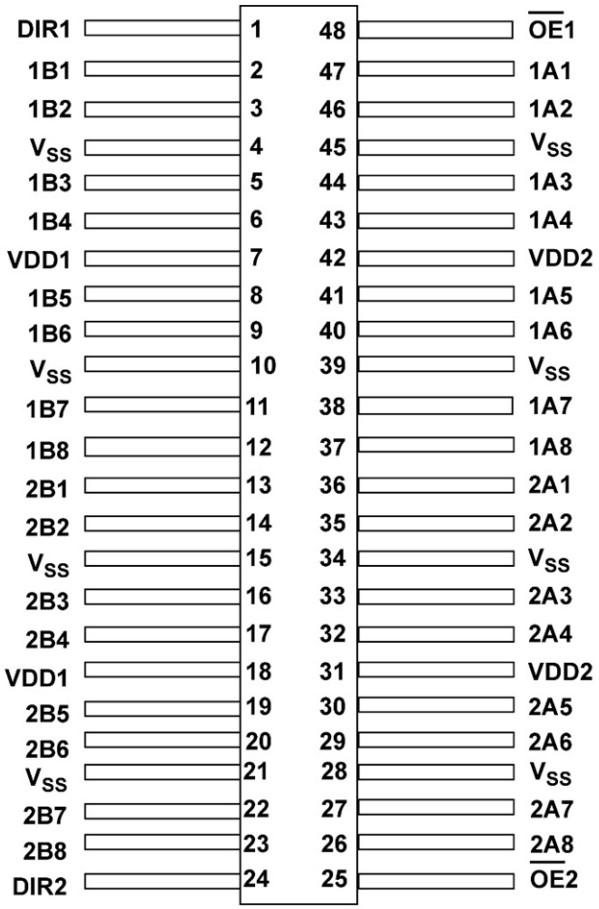
Logic Symbol



Pin Description

Pin Names	Description
$\overline{OE}$x	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

Pinouts



48-Lead Flatpack
Top View

Cold Spare

The UT54ACS164245S/SE places the device into "Cold Spare" mode when BOTH supplies are set to V_{SS} +/-0.25V with a maximum 1KΩ impedance between V_{DDx} and V_{SS}. While in Cold Spare, the device places all outputs into a high impedance state (see DC electrical parameters, Ics)

Power Table[1]

Port B	Port A	Operation
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non-Translating
3.3 Volts	3.3 Volts	Non-Translating
V_{SS}	V_{SS}	Cold Spare
V_{SS}	3.3V or 5V	Port B Cold Spare

Note:

1. V_{DDx} cannot be tied to V_{SS} while power is applied to V_{DD1}.

I/O Guidelines

Control signals DIRx and $\overline{OE}$x are 5-volt tolerant inputs. When V_{DDx} is at 3.3 volts, either 3.3 or 5 volt CMOS logic levels can be applied to all control inputs. Additionally, it is recommended that all unused inputs be tied to V_{SS} through a 1KΩ to 10KΩ resistor. It's good design practice to tie the unused input to V_{SS} via a resistor to reduce noise susceptibility. The resistor protects the input pin by limiting the current from high going variations in V_{SS}. The number of inputs that can be tied to the resistor pull-down can vary. It is up to the system designer to choose how many inputs are tied together by figuring out the max load the part can drive while still meeting system performance specs. Input signal transitions should be driven to the device with a rise and fall time that is <100ms.

Power Application Guidelines

For proper operation connect power to all V_{DD} pins and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). If V_{DD1} and V_{DDx} are not powered up together, then V_{DDx} should be powered up first for proper control of $\overline{OE}$x and DIRx. Until V_{DDx} reaches 2.75V + 5%, control of the outputs by OE and DIR cannot be guaranteed. During operation of the part, after power up, insure $V_{DD1} > V_{DDx}$.

Power Up

The direction control (DIRx) and output enable ($\overline{OE}$x) for the UT54ACS164245S/SE will only function properly if V_{DDx}, PortA, (3.3V) is powered up before V_{DD1}, PortB, (5.0V). The circuitry that powers $\overline{OE}$x and DIRx is powered internally from the V_{DDx} supply, as illustrated in Figure S/SE Planes. If this sequence is not followed there is no way to guarantee the state of $\overline{OE}$x and DIR if V_{DD1} was powered up before V_{DDx}. After power up V_{DD1} must be greater than or equal to V_{DDx}. However, V_{DDx} cannot be connected to V_{SS} while V_{DD1} is powered.

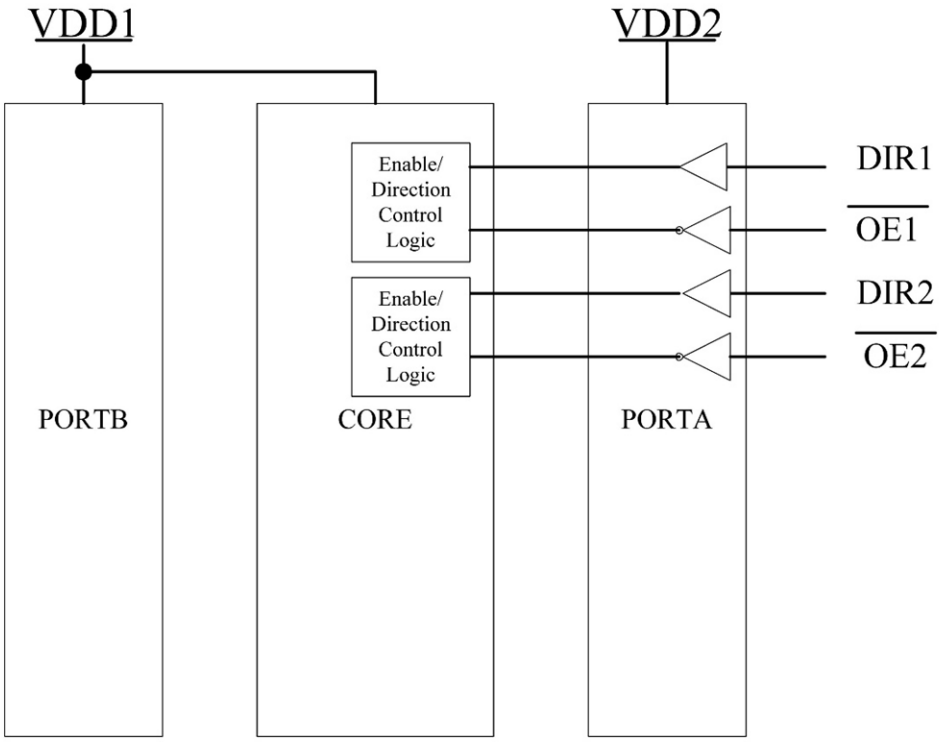


Figure S/SE Planes
Internal connection of ports and power supplies

Power Down

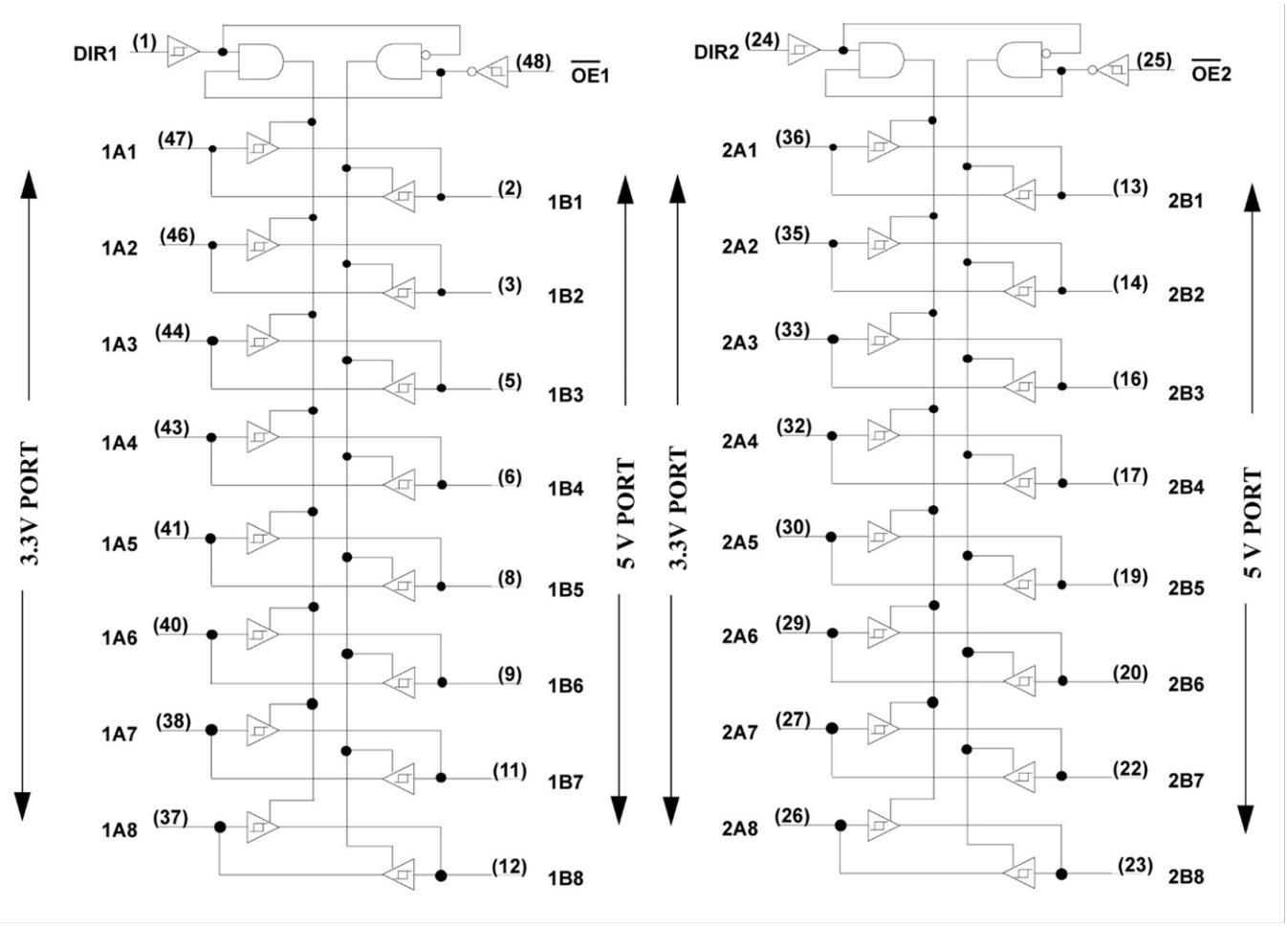
The proper power down sequence for the UT54AC164245SE requires that outputs on both Port A and Port B be disabled first,

1. $\overline{OE}$x high
2. Next power down V_{DD1}
3. Then power down V_{DDx}

Function Table

Enable $\overline{OEx}$	Direction DIRx	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

Logic Diagram



Operational Environment[1]

Parameter	Limit	Units
Total Dose	1.0E5	rad(Si)
SEL Latchup	>120	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limit (Mil Only)	Units
$V_{I/O}$ (Port B)[2]	Voltage any pin during operation	-.3 to V_{DD1} +.3	V
$V_{I/O}$ (Port A)[2]	Voltage any pin during operation	-.3 to V_{DDx} +.3	V
V_{DD1}	Supply voltage	-0.3 to 6.0	V
V_{DDx}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. For Cold Spare mode (V_{DD} = V_{SS}), $V_{I/O}$ may be -0.3V to the maximum recommended operating V_{DD}+0.3V.

Dual Supply Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD1}	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{DDx}	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{IN} (Port B)	Input voltage any pin	0 to V_{DD1}	V
V_{IN} (Port A)	Input voltage any pin	0 to V_{DDx}	V
T_C	Temperature range	-55 to + 125	℃

DC Electrical Characteristics[1]

(-55℃ < T_C < +125℃) (T_C = -55℃ to +125℃) Unless otherwise noted, T_C is per the temperature ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{T+}	Schmitt Trigger, positive going threshold[2]	V_{DD} from 3.00 to 5.5		.7V_{DD}	V
V_{T-}	Schmitt Trigger, negative going threshold[2]	V_{DD} from 3.00 to 5.5	.3V_{DD}		V
V_{H1}	Schmitt Trigger range of hysteresis[10]	V_{DD} from 4.5 to 5.5	0.6		V
V_{H2}	Schmitt Trigger range of hysteresis[10]	V_{DD} from 3.00 to 3.6	0.4		V
I_{IN}	Input leakage current[10]	V_{DD} from 3.6 to 5.5 V_{IN} = V_{DD} or V_{SS}	-1	3	µA
I_{OZ}	Three-state output leakage current[10]	V_{DD} from 3.6 to 5.5 V_{IN} = V_{DD} or V_{SS}	-1	3	µA
I_{CS}	Cold sparing input leakage current[3]	V_{IN} = 5.5 V_{DD} = V_{SS}	-1	5	µA
I_{OS1}	Short-circuit output current[6,11]	V_O = V_{DD} or V_{SS} V_{DD} from 4.5 to 5.5	-200	200	mA
I_{OS2}	Short-circuit output current[6,11]	V_O = V_{DD} or V_{SS} V_{DD} from 3.00 to 3.6	-100	100	mA
V_{OL1}	Low-level output voltage[4,10]	I_{OL}= 8mA I_{OL}= 100µA V_{DD} = 4.5		0.4 0.2	V
V_{OL2}	Low-level output voltage[4,10]	I_{OL}= 8mA I_{OL}= 100µA V_{DD} = 3.00		0.5 0.2	V
V_{OH1}	High-level output voltage[4,10]	I_{OH}= -8mA I_{OH}= -100µA V_{DD} = 4.5	V_{DD} - 0.7 V_{DD} - 0.2		V
V_{OH2}	High-level output voltage[4,10]	I_{OH}= -8mA I_{OH}= -100µA V_{DD} = 3.00	V_{DD} - 0.9 V_{DD} - 0.2		V

DC Electrical Characteristics[1]

Symbol	Parameter	Condition	MIN	MAX	Unit
P_{total1}	Power dissipation[5,7,8]	C_L = 50pF V_{DD} from 4.5 to 5.5		2.0	mW/ MHz
P_{total2}	Power dissipation[5,7,8]	C_L = 50pF V_{DD} from 3.00 to 3.6V		1.5	mW/ MHz
I_{DD}	Standby Supply Current V_{DD1} or V_{DDx}	VIN = V_{DD} or V_{SS} V_{DD} = 5.5			
	Pre-Rad 25°C	$\overline{OE}$=V_{DD}		10	µA
	Pre-Rad -55°C to +125°C	$\overline{OE}$=V_{DD}		100	µA
	Post-Rad 25°C	$\overline{OE}$=V_{DD}		500	µA
C_{IN}	Input Capacitance[9]	f = 1MHz @ 0V V_{DD} from 3.00 to 5.5		15	pF
C_{OUT}	Output Capacitance[9]	f = 1MHz @ 0V V_{DD} from 3.00 to 5.5		15	pF

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. All combinations of $\overline{OE}$x and DIRx
4. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
5. Guaranteed by characterization.
6. Not more than one output may be shorted at a time for maximum duration of one second.
7. Power does not include power contribution of any CMOS output sink current.
8. Power dissipation specified per switching output.
9. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
10. Guaranteed; tested on a sample of pins per device.
11. Supplied as a design limit, but not guaranteed or tested.

AC Electrical Characteristics*[1] (Port B = 5 Volt, Port A = 3.3 Volt)

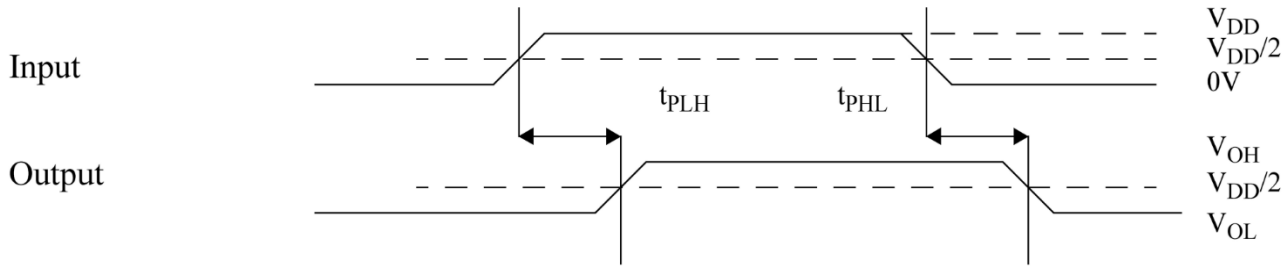
(V_{DD1} = 5V ±10%; V_{DDx} = 3.00V to 3.6V, -55°C < T_C < +125°C) Unless otherwise noted, T_C is per the temperature ordered.

Symbol	Parameter	MIN	MAX	MIN	MAX	Unit
		UT54ACS164245S		UT54ACS164245SE		
t_{PLH}	Propagation delay Data to Bus	1	20	3.5	11	ns
t_{PHL}	Propagation delay Data to Bus	1	20	3.5	11	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	18	2.5	16	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	18	2.5	16	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	2.5	16	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	2.5	16	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	18	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	18	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	20	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	20	1	20	ns
t_{SKEW}[3]	Skew between outputs			-	600	ps
t_{DSKEW}[4]	Differential skew between outputs			-	1.5	ns

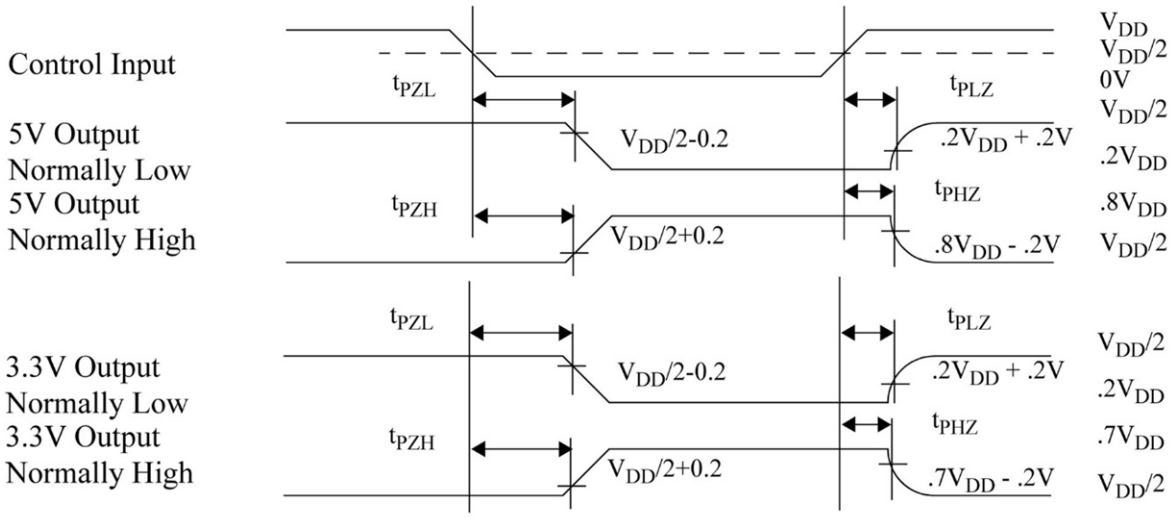
Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested.
3. Output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly, 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
4. Differential output skew is defined as a comparison of any two output transitions of opposite types at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus low-to-high; similarly, 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.

Propagation Delay



Enable Disable Times



AC Electrical Characteristics[1] (Port A = Port B, 5 Volt Operation)

(V_{DD1} = 5V ±10%; V_{DDx} = 5.0V ±10%, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature ordered.

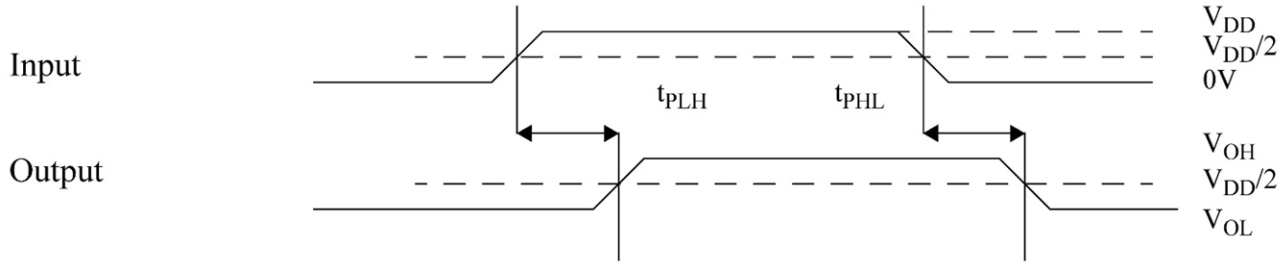
Symbol	Parameter		MIN	MAX	MIN	MAX	Unit
			UT54ACS164245S		UT54ACS164245SE		
t_{PLH}	Propagation delay Data to Bus	C_L = 40pF	1	15	3.5	9	ns
t_{PHL}	Propagation delay Data to Bus	C_L = 40pF	1	15	3.5	9	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus		1	12	3	9	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus		1	12	3	9	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance		1	15	3	9	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance		1	15	3	9	ns
t_{PZL}[2]	Output enable time DIRx to Bus		1	12	1	12	ns
t_{PZH}[2]	Output enable time DIRx to Bus		1	12	1	12	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance		1	15	1	15	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance		1	15	1	15	ns
t_{SKEW}[3]	Skew between outputs				-	600	ps
t_{DSKEW}[4]	Differential skew between outputs				-	1.5	ns

Notes:

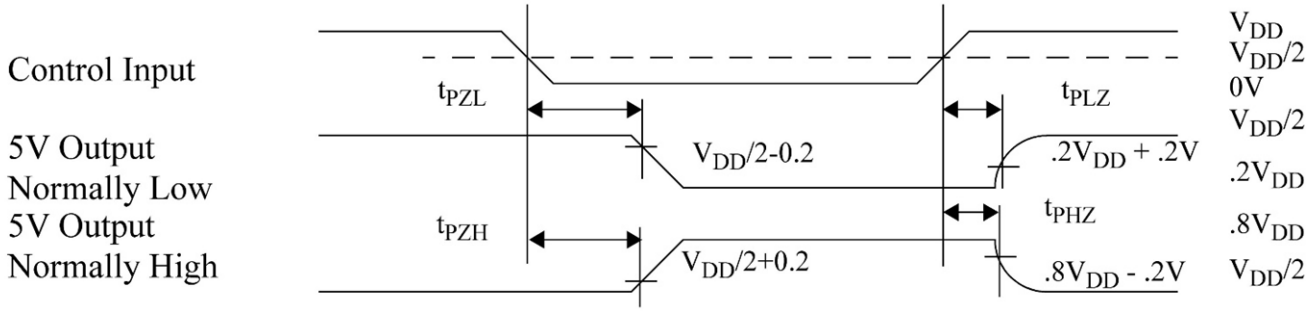
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MILSTD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs low-to-high.
4. Differential skew is defined as a comparison of any two output transitions high-to-low vs. low-to-high and low-to-high vs high-to-low.

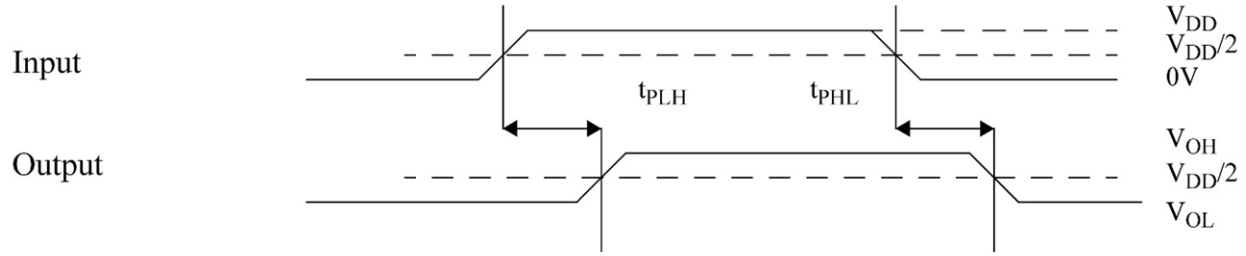
Propagation Delay



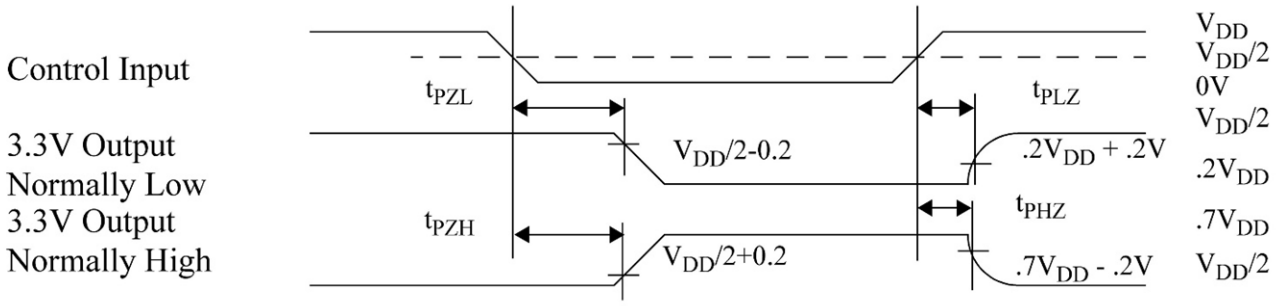
Enable Disable Times



Propagation Delay



Enable Disable Times



AC Electrical Characteristics*[1] (Port A = Port B, 3.3 Volt Operation)

(V_{DD1} = 3.00V to 3.6V; V_{DDx} = 3.00V to 3.6V, -55°C < T_C < +125°C)

Symbol	Parameter		MIN	MAX	MIN	MAX	Unit
			UT54ACS164245S		UT54ACS164245SE		
t_{PLH}	Propagation delay Data to Bus	C_L = 40pF	1	20	3.5	11	ns
t_{PHL}	Propagation delay Data to Bus	C_L = 40pF	1	20	3.5	11	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus		1	18	2.5	16	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus		1	18	2.5	16	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance		1	20	2.5	16	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance		1	20	2.5	16	ns
t_{PZL}[2]	Output enable time DIRx to Bus		1	18	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus		1	18	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance		1	20	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance		1	20	1	20	ns
t_{SKEW}[3]	Skew between outputs					600	ps
t_{DSKEW}[4]	Differential skew between outputs					1.5	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD883 Method 1019, Condition A up to the maximum TID level procured.

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. $\overline{OE}$x to bus times are tested
3. Output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the same byte: 1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly, 1B1 through 1B8 are compared, 2A1 through 2A8 are compared, and 2B1 through 2B8 are compared.
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Package

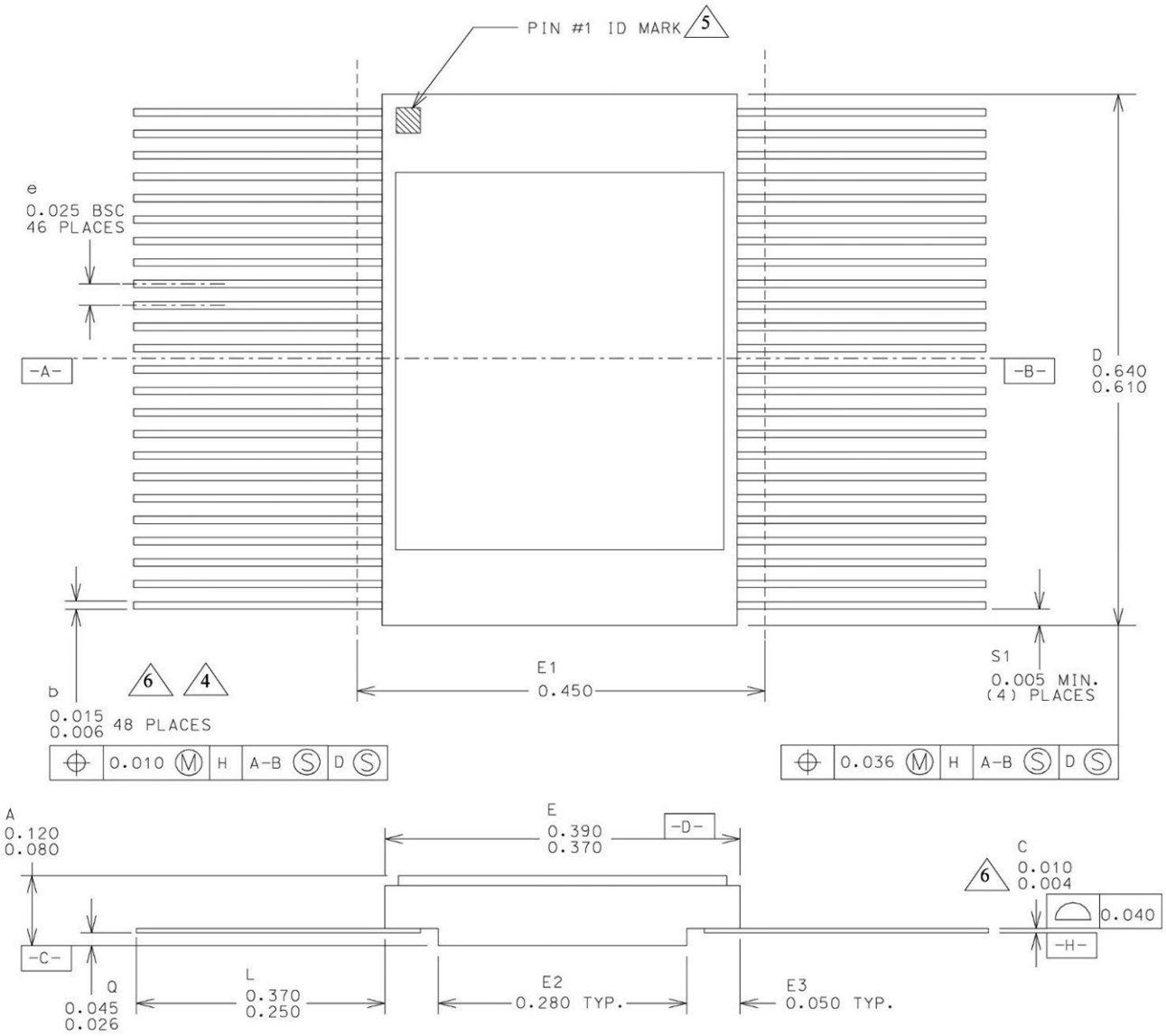


Figure 1. 48-Lead Flatpack

Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

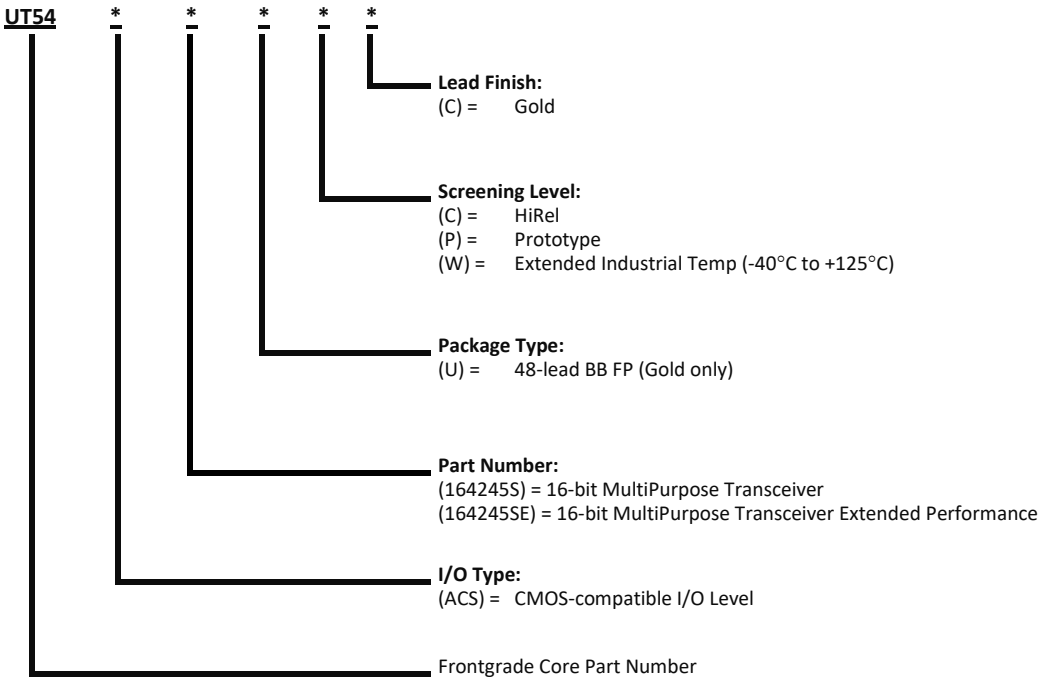
Ordering Information

UT54ACS164245S/SE: SMD

Notes:

1. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Frontgrade Part Numbering Ordering Information



Notes:

1. HiRel Temperature Range flow per Frontgrade Manufacturing Flows Document. Devices are tested -55C, room temp, and 125C.Radiation neither tested nor guaranteed.
2. Prototype flow per Frontgrade Manufacturing Flows Document Tested at 25C only. Lead finish is gold only. Radiation neither tested nor guaranteed.
3. Extended Industrial Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -40°C, room temp, and +125°C. Radiation is neither tested nor guaranteed.

Revision History

Date	Revision #	Author	Change Description	Page #
4/30/2026	1.0.1	MJL	Corrected proto part option from D to P typo. Previous version date was 4/1/2016	17

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.