FRONTGRADE

DATASHEET

UT54ACS138E

3-Line to 8-Line Decoders/Demultiplexers

7/1/2013

Version #: 1.0

Features

- 0.6 µm CRH CMOS process
  — Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range of 3.0V to 5.5V
- Available QML Q or V processes
- 16-pin flatpack
- UT54ACS138E-SMD-5962-96544

Description

The UT54ACS138E is a 3-line to 8-line decoders/demultiplexer designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times.

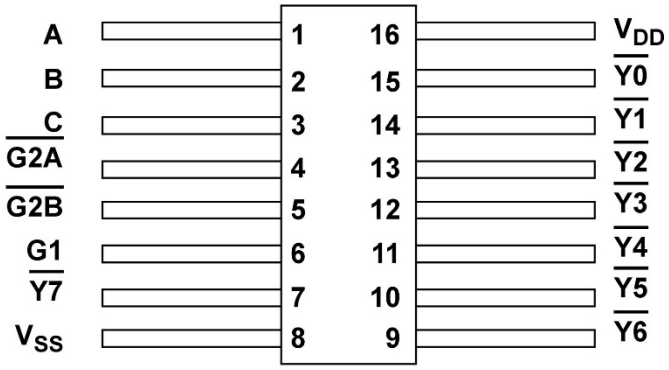
The conditions at the binary select inputs and the three enable inputs select one of eight output lines. Two active low and one active-high enable inputs reduce the need for external gates of inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The devices are characterized over the full military temperature range of -55°C to +125°C.

Function Table

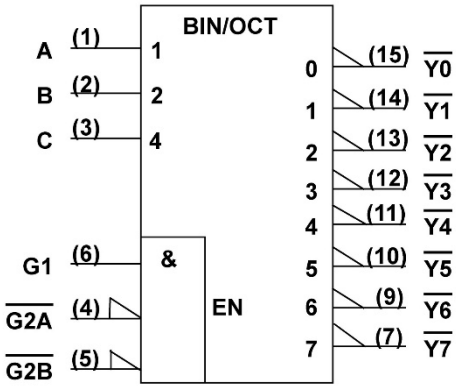
Enable Inputs			Select Inputs			Output							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

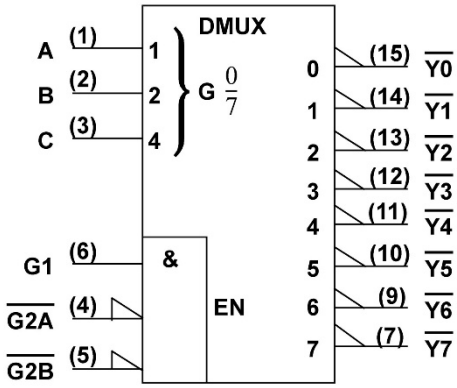
Pinout



16-Lead Flatpack
Top View

Logic Symbol

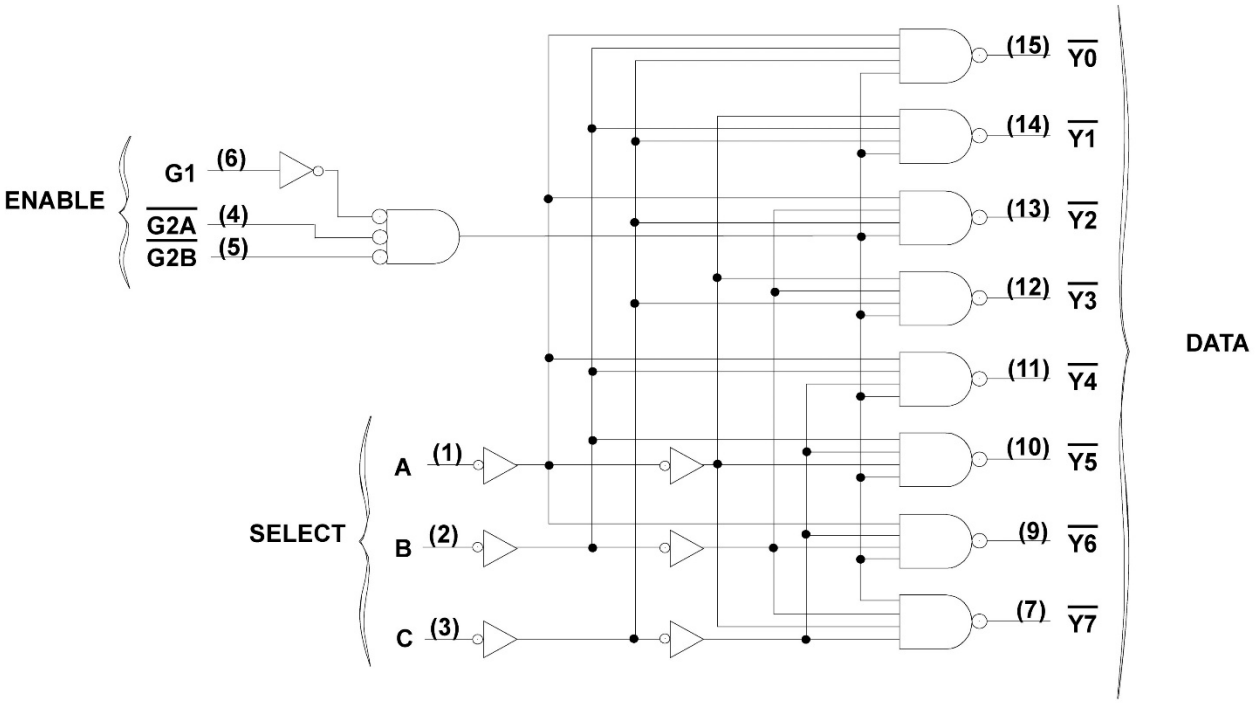


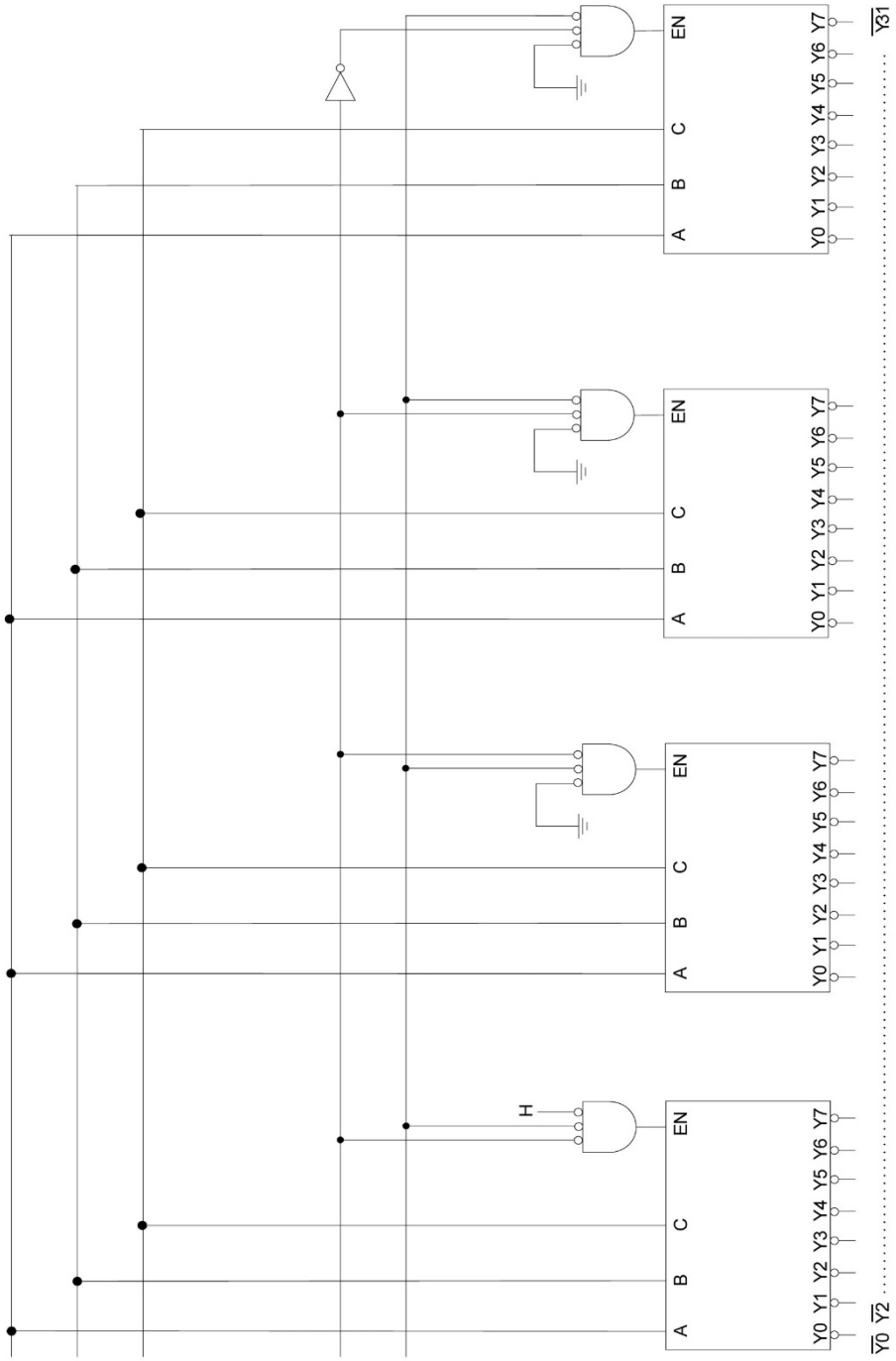


Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

Logic Diagram





Expansion to 1-of-32 Decoding

Operational Environment[1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold[2]	108	MeV-cm²/mg
SEL Threshold	120	MeV-cm²/mg
Neutron Fluence	1.0E14	n/cm²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15.0	°C/W
I_I	DC input current	±10	mA
P_D[2]	Maximum power dissipation permitted @ T_C=125°C	3.3	W

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{j(max)}\ T_{C(max)}) / \Theta_{JC}$

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

Electrical Characteristics (Pre- and Post-Radiation)*

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Description	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage[1]	V_{DD} from 3.0V to 5.5V		0.3 V_{DD}	V
V_{IH}	High-level input voltage[1]	V_{DD} from 3.0V to 5.5V	0.7 V_{DD}		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage[3]	I_{OL} = 100µA V_{DD} from 3.0V to 5.5V		0.25	V
V_{OH}	High-level output voltage[3]	I_{OH} = -100µA V_{DD} from 3.0V to 5.5V	V_{DD} -0.25		V
I_{OS1}	Short-circuit output current[2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5 V to 5.5V	-200	200	mA
I_{OS2}	Short-circuit output current[2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0 V to 3.6V	-100	100	mA
I_{OL1}	Low level output current[8] (sink)	V_{IN} = V_{DD} or V_{SS}; V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	8		mA
I_{OL2}	Low level output current[8] (sink)	V_{IN} = V_{DD} or V_{SS}; V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	6		mA
I_{OH1}	High level output current[8] (source)	V_{IN} = V_{DD} or V_{SS}; V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current[8] (source)	V_{IN} = V_{DD} or V_{SS}; V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation[7,8]	C_L = 50pF; V_{DD} = 4.5V to 5.5V		1.1	mW/ MHz
P_{total2}	Power dissipation[7,8]	C_L = 50pF; V_{DD} from 3.0V to 3.6V		0.5	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.6V to 5.5V		10	µA
C_{IN}	Input capacitance[5]	f = 1MHz, V_{DD} = 0V		15	pF
C_{OUT}	Output capacitance[5]	f = 1MHz, V_{DD} = 0V		15	pF

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. Power dissipation specified per switching output.
8. Parameter guaranteed by design and characterization, but is not tested.

AC Electrical Characteristics (Pre- and Post-Radiation)*

(V_{DD}=3.0V to 5.5V; V_{SS} = 0V[1], -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Parameter	Condition	V_{DD}	Minimum	Maximum	Unit
t_{PLH1}	Binary select to $\overline{Y}$n	C_L = 50pF	3.0V to 3.6V	4	19	ns
			4.5V to 5.5V	3	10	
t_{PHL1}	Binary select to $\overline{Y}$n	C_L = 50pF	3.0V to 3.6V	4	19	ns
			4.5V to 5.5V	3	10	
t_{PLH2}	Enable to Output $\overline{Y}$n	C_L = 50pF	3.0V to 3.6V	3	19	ns
			4.5V to 5.5V	3	10	
t_{PHL2}	Enable to Output $\overline{Y}$n	C_L = 50pF	3.0V to 3.6V	4	19	ns
			4.5V to 5.5V	3	10	

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Maximum allowable relative shift equals 50mV.

Packaging

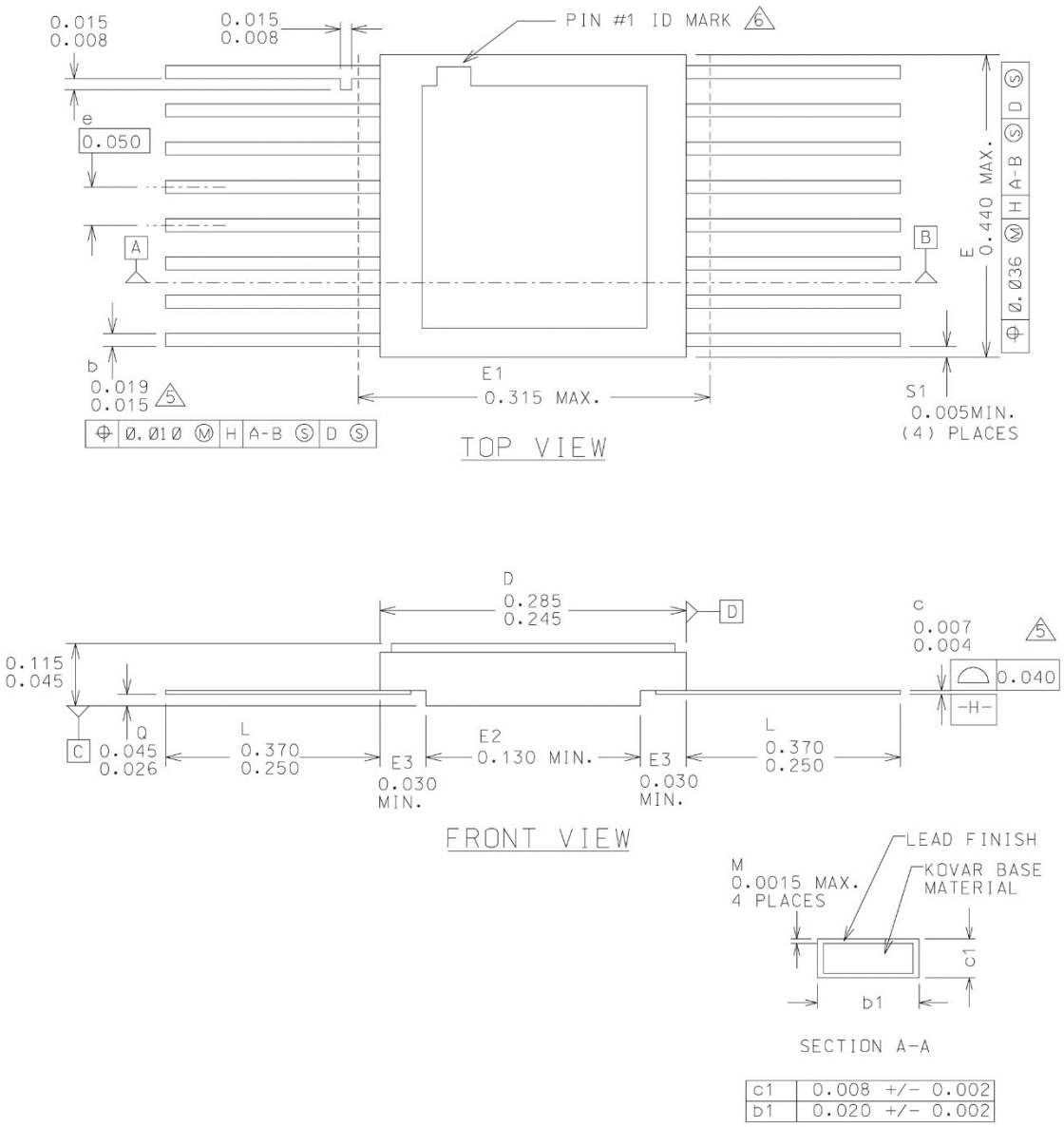


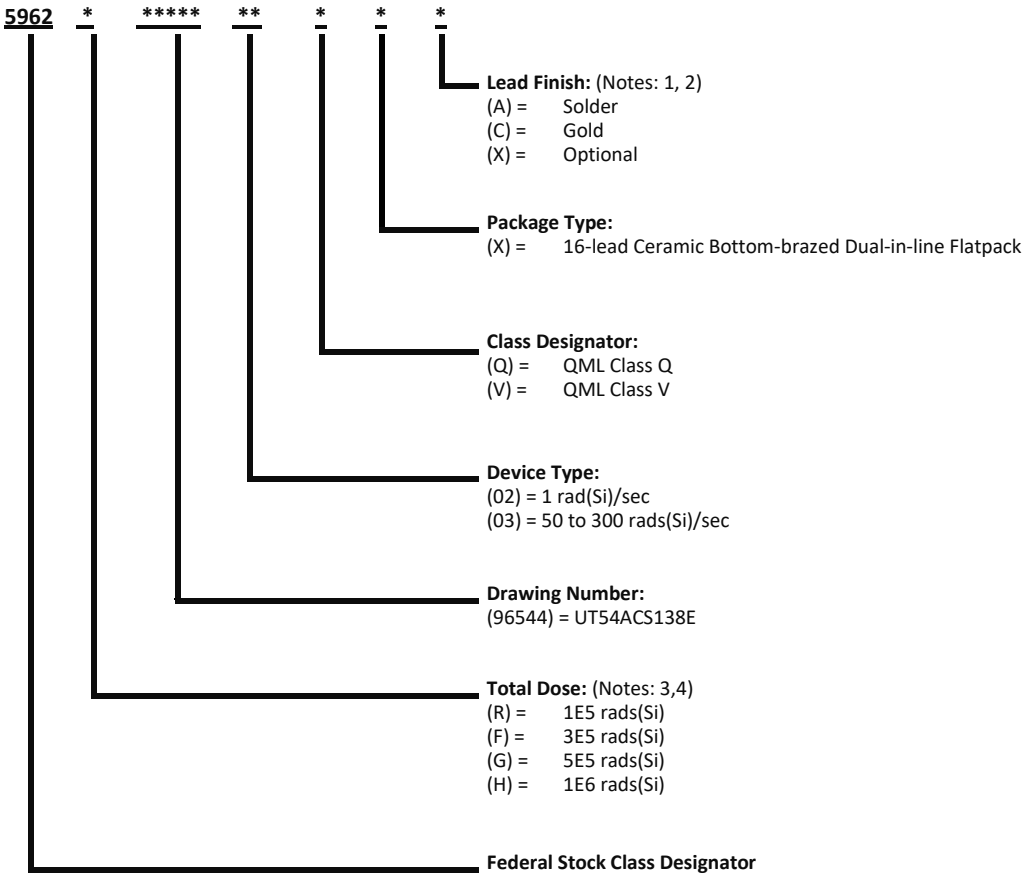
Figure 1. 16-lead Flatpack

Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-M-38510.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Package dimensions and symbols are similar to MIL-STD-1835 variation F-5A.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.

Ordering Information

SMD Part Number Ordering Information



Notes:

1. Lead finish (A, C or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.