FRONTGRADE

# DATASHEET

# UT28F256QLE

Radiation-Hardened 32K x 8 PROM

1/21/2025

Version #: 1.0.1

## Features

- Programmable, read-only, asynchronous, radiation- hardened, 32K x 8 memory
  - > Supported by industry standard programmer
  - > Programming yield estimated at 80% or greater (ref note on ordering page(s))
- 45ns maximum address access time (-55°C to+125°C)
- TTL compatible input and TTL/CMOS compatible output levels
- Three-state data bus
- Low operating and standby current
  - > Operating: 80mA maximum @25MHz
    - — Derating: 3mA/MHz
  - > Standby: 1.5mA maximum (post-rad)
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - > Total dose: 100krad to 1Megarad(Si)
  - > Onset LET: 57 MeV-cm$^2$/mg
  - > SEL Immune ≥110 MeV-cm$^2$/mg
- QML Q & V compliant part
  - > AC and DC testing at factory
- No post program conditioning
- Packaging options:
  - > 28-lead 50-mil center flatpack (0.490 x 0.74)
- $V_{DD}$: 5.0volts ±10%
- Standard Microcircuit Drawing 5962-96891

## Product Description

The UT28F256QLE amorphous silicon redundant ViaLink™ PROM is a high performance, asynchronous, radiationhardened, 32K x 8 programmable memory device. The UT28F256QLE PROM features fully asychronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F256QLE. The combination of radiation-hardness, fast access time, and low power consumption make the UT28F256QLE ideal for high speed systems designed for operation in radiation environments.

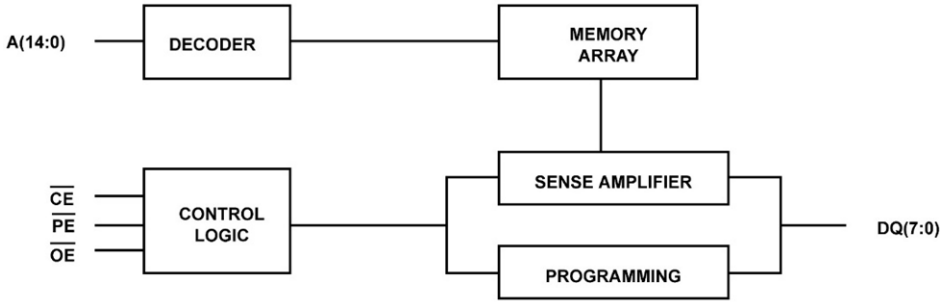
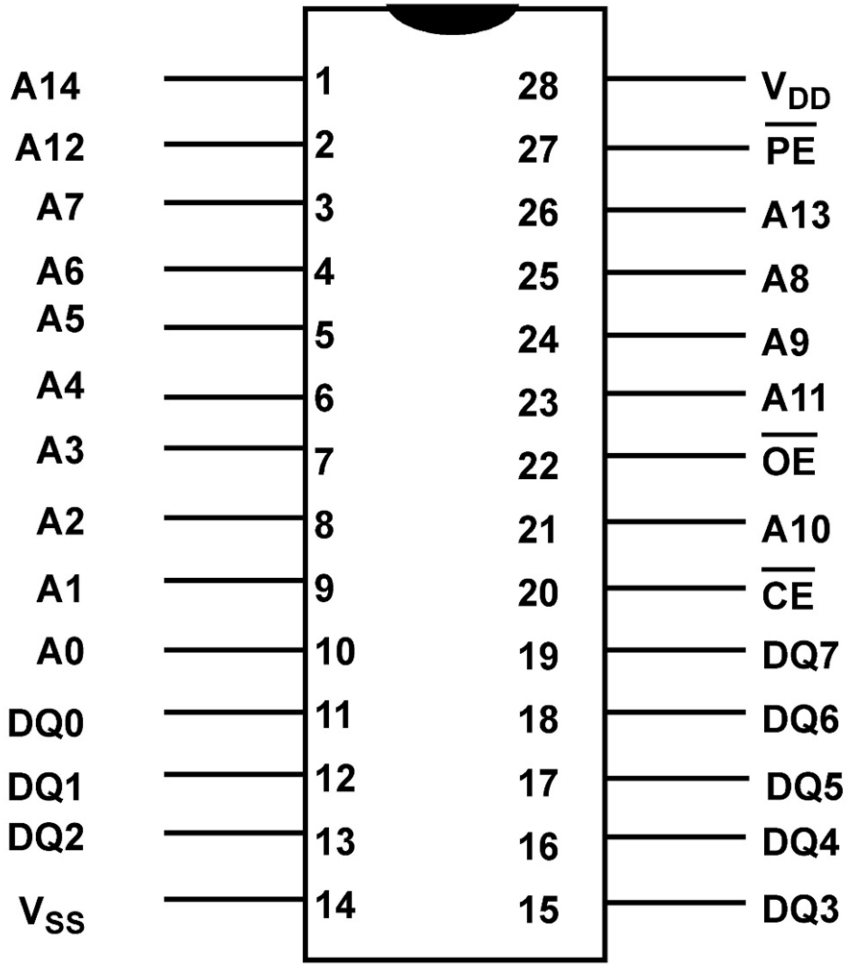



Figure 1: PROM Block Diagram

## Device Operation

The UT28F256QLE has three control inputs: Chip Enable ($\overline{CE}$ ), Program Enable ( $\overline{PE}$), and Output Enable ($\overline{OE}$ ); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\overline{CE}$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\overline{CE}$ causes IDD to rise to its active value and decodes the fifteen address inputs to select one of 32,768 words in the memory. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs.

## Pin Configuration



### Pin Names

| A(14:0) | Address |
|---|---|
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{PE}$ | Program Enable |
| DQ(7:0) | Data Input/Data Output |

### Table 1. Device Operation Truth Table [1]

| $\overline{OE}$ | $\overline{PE}$ | $\overline{CE}$ | I/O Mode | Mode |
|---|---|---|---|---|
| X | 1 | 1 | Three-state | Standby |
| 0 | 1 | 0 | Data Out | Read |
| 1 | 0 | 0 | Data In | Program |
| 1 | 1 | 0 | Three-state | Read 2 |

**Notes:**

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

## Absolute Maximum Ratings [1]

### (Referenced to VSS)

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{DD}$ | DC supply voltage | -0.3 to 6.0 | V |
| $V_{I/O}$ | Voltage on any pin | -0.5 to ($V_{DD}$ + 0.5) | V |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $P_D$ | Maximum power dissipation | 1.5 | W |
| $T_J$ | Maximum junction temperature | +175 | °C |
| $\Theta_{JC}$ | Thermal resistance junction to case2 | 3.3 | °C/W |
| $I_I$ | DC input current | ±10 | mA |

**Notes:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012, infinite heat sink.

### Recommended Operating Conditions

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{DD}$ | Positive supply voltage | 4.5 to 5.5 | V |
| $T_C$ | Case temperature range | -5.5 to +125 | °C |
| $V_{IN}$ | DC input voltage | 0 to $V_{DD}$ | V |

## DC Electrical Characteristics (Pre/Post-Radiation) *

### ($V_{DD}$ = 5.0V±10%; -55°C < $T_C$ < +125°C)

| Symbol | Parameter | Condition | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ [5] | High-level input voltage | (TTL) | 2.4 | | V |
| $V_{IL}$ [5] | Low-level input voltage | (TTL) | | 0.8 | V |
| $V_{OL1}$ | Low-level output voltage | $I_{OL}$ = 4.0mA , $V_{DD}$ = 4.5V(TTL) | | 0.4 | V |
| $V_{OL2}$ | Low-level output voltage | $I_{OL}$ = 200µA, $V_{DD}$ = 4.5V(CMOS) | | VSS + 0.10 | V |
| $V_{OH1}$ | High-level output voltage | $I_{OH}$ = -200µA, $V_{DD}$ = 4.5V(CMOS) | $V_{DD}$ - 0.1 | | V |
| $V_{OH2}$ | High-level output voltage | $I_{OH}$ = -2.0mA $V_{DD}$ = 4.5V(TTL) | 2.4 | | V |
| $C_{IN}$ [1] | Input capacitance, all inputs except $\overline{PE}$<br>Input Capacitance $\overline{PE}$ | ∫ = 1MHz, $V_{DD}$ = 5.0V<br>$V_{IN}$ = 0V | | 15<br>20 | pF |
| $C_{IO}$ [1] | Bidirectional I/O capacitance | ∫ = 1MHz, $V_{DD}$ = 5.0V $V_{OUT}$ = 0V | | 15 | pF |
| $I_{IN}$ | Input leakage current | $V_{IN}$ = 0V to $V_{DD}$, all pins except $\overline{PE}$<br>$V_{IN}$ = $V_{DD}$, $\overline{PE}$ only | -5 | +5 132 | µA<br>µA |
| $I_{OZ}$ | Three-state output leakage current | $V_O$ = 0V to $V_{DD}$<br>$V_{DD}$ = 5.5V<br>$\overline{OE}$ = 5.5V | -10 | +10 | µA |
| $I_{OS}$ [2, 3] | Short-circuit output current | $V_{DD}$ = 5.5V, $V_O$ = $V_{DD}$<br>$V_{DD}$ = 5.5V, $V_O$ = 0V | -120 | 120 | mA<br>mA |
| $I_{DD1}$(OP) [4] | Supply current operating<br>@22.2MHz (45ns product) | TTL input levels ($I_{OUT}$ = 0), VIL = 0.2V,<br>$V_{DD}$, $\overline{PE}$ = 5.5V | | 80 | mA |
| $I_{DD2}$(SB)post-rad | Supply current standby | CMOS input levels, $V_{IL}$ = $V_{SS}$ +0.25V<br>$\overline{CE}$= $V_{DD}$ - 025, VIH = $V_{DD}$ - 0.25V | | 1.5 | mA |

**Notes: *Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1E6 rads(Si).**

1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Derates at 3.2mA/MHz.
5. $V_{IL}$ and $V_{IH}$ for input signals A6, A7, A8, A9, A12, A13 and A14 guaranteed by design.

## Read Cycle

A combination of $\overline{PE}$ greater than $V_{IH}$(min), and $\overline{CE}$ less than VIL(max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data output, DQ(7:0), after the specified tAVQV is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

The chip enable-controlled access is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified tELQV is satisfied, the eight-bit word addressed by A(14:0) appears at the data outputs DQ(7:0).

Output enable-controlled access is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is $t_{GLQV}$ unless $t_{AVQV}$ or $t_{ELQV}$ have not been satisfied.

## AC Characteristics Read Cycle (Post-Radiation)*

**($V_{DD}$ = 5.0V±10%; -55°C < $T_C$ < +125°C)**

| Symbol | Parameter | 28F256-45 | | Unit |
|---|---|---|---|---|
| | | MIN | MAX | |
| $t_{AVAV}$ [1] | Read cycle time | 45 | | ns |
| $t_{AVQV}$ | Read access time | | 45 | ns |
| $t_{AXQX}$ [2] | Output hold time | 0 | | ns |
| $t_{GLQX}$ [2] | $\overline{OE}$ -controlled output enable time | 0 | | ns |
| $t_{GLQV}$ | $\overline{OE}$ -controlled access time | | 15 | ns |
| $t_{GHQZ}$ | $\overline{OE}$ -controlled output three-state time | | 15 | ns |
| $t_{ELQX}$ [2] | $\overline{CE}$ -controlled output enable time | 0 | | ns |
| $t_{ELQV}$ | $\overline{CE}$ -controlled access time | | 45 | ns |
| $t_{EHQZ}$ | $\overline{CE}$ -controlled output three-state time | | 15 | ns |

**Notes: *Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).**

1. Functional test.
2. Three-state is defined as a 200mV change from steady-state output voltage.

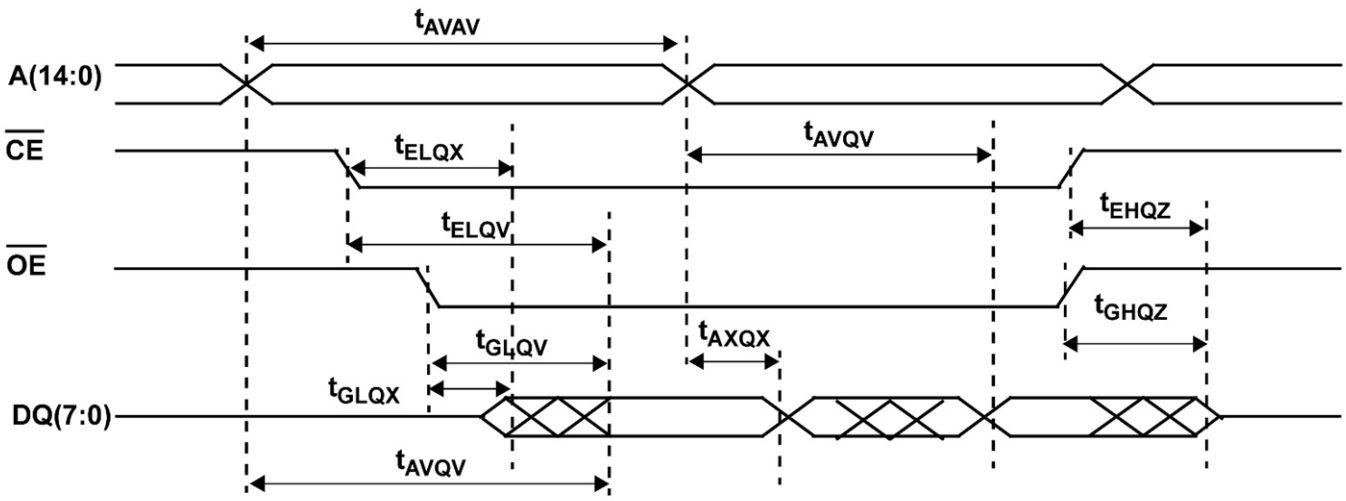



Figure 2: PROM Read Cycle

## Radiation Hardness

The UT28F256QLE PROM incorporates special design and layout features which allow operation in high-level radiation environments. Frontgrade Colorado Springs has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, Frontgrade builds all radiation hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, Frontgrade pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

### Radiation Hardness Design Specifications [1]

| Total Dose | 1E6 | rad(Si) |
|---|---|---|
| Latchup LET Threshold | >110 | MeV-cm²/mg |
| Memory Cell LET Threshold | >100 | MeV-cm²/mg |
| Logic Onset LET | >57 | MeV-cm²/mg |
| SEU Cross Section | 9.4E-7 | cm²/device |
| Error rate - geosynchronous orbit, Adams 90% worst case environment | 5.1E-15 | errors/device day |

**Note:**

1. The PROM will not latchup during radiation exposure under recommended operating conditions.

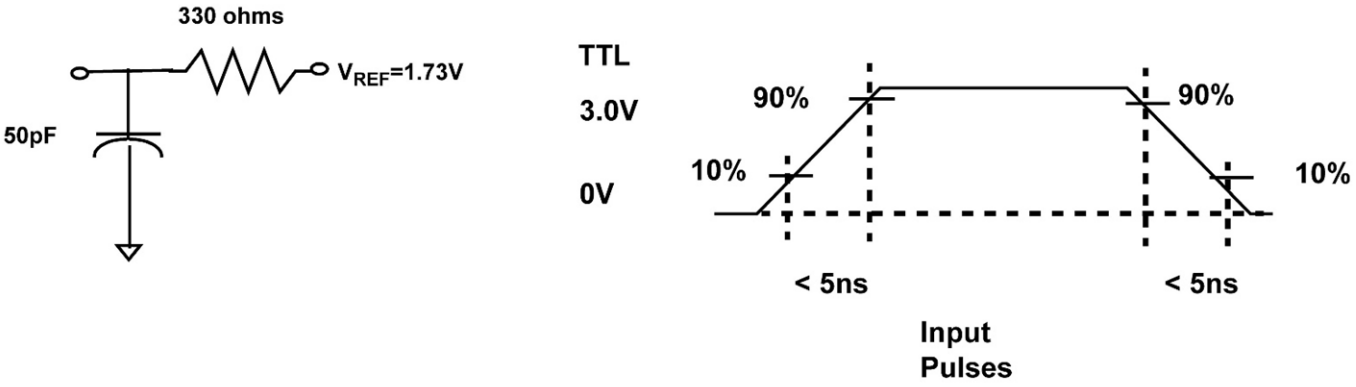



Figure 3: AC Test Loads and Input Waveforms

**Notes:**

1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (TTL input =1.5V).

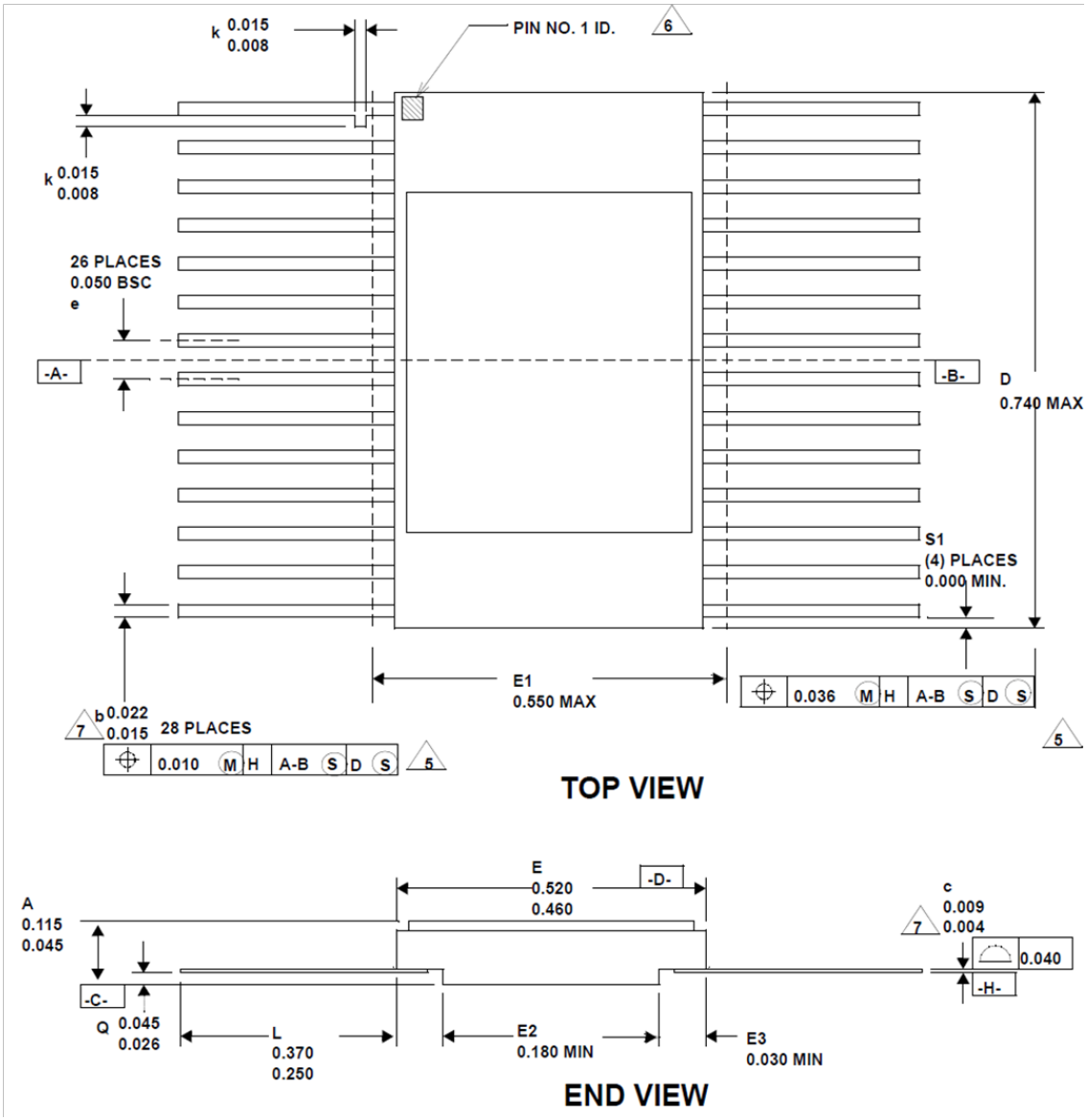



Figure 4: 28-Lead 50-mil Center Flatpack (0.490 x 0.74)

**Notes:**

1. All exposed metalized areas to be plated per MIL-PRF-38535.
2. The lid is connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension letters refer to MIL-STD-1835.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.
8. Total weight is approximately 2.4 grams.

## Ordering Information

**SMD Part Number Ordering Information**

**5962 * 96891 * * * ***

**Lead Finish:**
(A) = Solder
(C) = Gold
(X) = Optional

**Case Outline:**
(X) = 28-Lead-Flatpack

**Class Designator:**
(Q) = Class Q
(V) = Class V

**Device Type:**
(09) = 45ns Access Time, CMOS compatible inputs and CMOS compatible outputs
(10) = 45ns Access Time, CMOS compatible inputs and CMOS compatible outputs Extended Industrial Temp (-40°C to 125°C)

**Drawing Number:**
96891

**Total Dose**
(F) = 3E5 rad(Si)
(G) = 5E5 rad(Si)
(H) = 1E6 rad(Si)
(R) = 1E5 rad(Si)

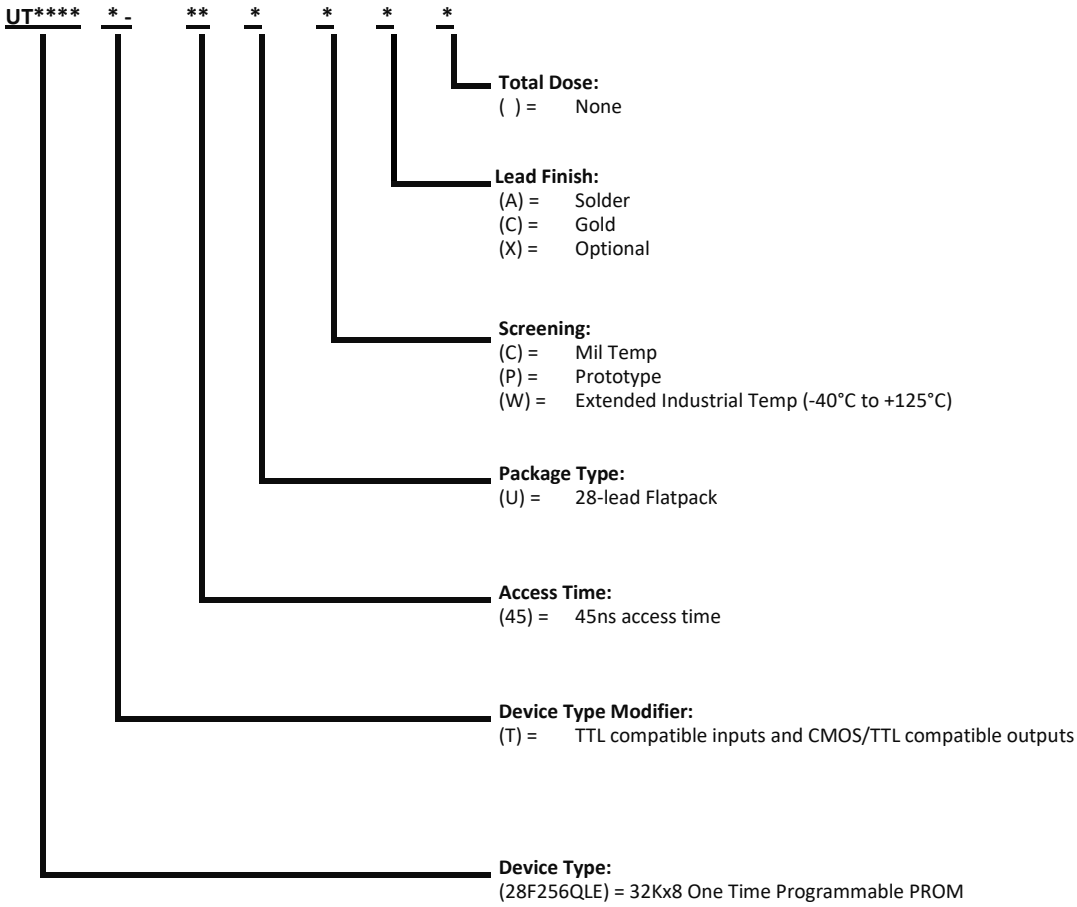
**Federal Stock Class Designator**
**No Options**

**Notes:**

1. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. Notes:
2. Lead finish (A, C, or X) must be specified.
3. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
4. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
5. Device type 09 available with total dose of 1E5 rads(Si) or 3E5 rads(Si).
6. Users should reference the "QLE Programming Guide" and the "QLE Programming Notes" documents available under the Applications Notes tab of the Frontgrade HiRel Microelectronics Memory device webpage for programming instructions and information.

## Ordering Information

**Frontgrade Part Number Ordering Information**




**Notes:**

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military Temperature Range flow per Frontgrade Colorado Springs Manufacturing Flows Document. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototype flow per Frontgrade Manufacturing Flows Document. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is gold only.
5. Extended Industrial Range flow per Frontgrade Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
6. Users should reference the "QLE Programming Guide" and the "QLE Programming Notes" documents available under the Applications Notes tab of the Frontgrade HiRel Microelectronics Memory device webpage for programming instructions and information.

## Revision History

| Date | Revision # | Author | Change Description | Page # |
|---|---|---|---|---|
| March 2007 | | | Initial revision used for change tracking purposes | |
| Feb 2020 | MJL | | Added programming yield estimate on page #1<br>Added note 5 to page 9 and note 6 to page 10. | p.1, 9, 10 |
| April 2022 | | | Added reference to note 5 to VIL VIH specifications and added note 5 to bottom of DC Electrical Characteristics table page 4. | p. 4 |
| Jan 2025 | 1.0.1 | MJL | Corrected ordering pages part number which was corrupted during Frontgrade conversion. Removed programming failure non guarantee notice from notes on both SMD and Frontgrade ordering information pages | p.10, 11 |

## Datasheet Definitions

| | Definition |
|---|---|
| Advanced Datasheet | Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.** |
| Preliminary Datasheet | Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available. |
| Datasheet | Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes. |