



FRONTGRADE

APPLICATION NOTE

UT699E

Migrating from the UT699 to the UT699E

1/15/2015
Version #: 1.0.0

Table 1.1 Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC1 Number:
UT699E 32-bit Fault-Tolerant SPARC V8/LEON 3FT Processor	UT699E	5962-13237	01, 02	WQ02

1. PIC = Product Identification Code

1.0 Overview

The UT699E is an enhanced version of the UT699. The main development objective for the UT699E was to improve performance and reduce power consumption over the UT699 while supporting backward compatibility. The UT699E is a drop-in replacement to the UT699, and customers utilizing the UT699 have a simple migration path to the new device. Since there are significant performance improvements, consideration should be given to evaluate real-time systems to capitalize on the improvements. Beyond the change to core voltage, there are several minor differences between the two devices that are explained in this document and summarized in the following table.

Table 2: Summary of UT699 Versus UT699E Differences

Attribute	UT699	UT699E	Recommendations
LEON3 Cache Size	I-8kB, D-8kB	I-16kB, D-16kB	No action necessary
LEON3 Data Cache Misses	Cache fetches 32-bit word(s) containing missed data	Cache misses always result in cache line fill	Must initialize all cachable data memory and evaluate real-time systems for latency changes
LEON3 Cache Snooping	Not functional	Fully functional	Replace software snooping routines with hardware snoop operations
LEON3 Cache Freeze	Cache freeze is available for data and instruction cache	Only instruction cache freeze is available	Primarily a software analysis feature. Evaluate all software using this feature and adjust for no data cache freeze
LEON3 Load Delay	Pipeline load delays is 2	Pipeline load delays is 1	Evaluate real-time systems for latency changes
LEON3 MMU	8 + 8 I/D TLB entries 2 clocks stall on write hit	16 + 16 I/D TLB entries No stall on write hit	No action necessary
LEON3 FPU	GRFPU with errata	Improved GRFPU, correcting previous errata	Consider recompiling code without the -mtune option
LEON3 Register File	Protected against SEU using 7-bit BCH (SEC/ DED)	Protected against SEU using TMR	No action necessary
LEON3 Multiplier	16-bit multiplier requiring 5 clocks per MUL instruction	32-bit multiplier requiring 1 clock per MUL instruction	No action necessary
LEON3 Instruction Trace Buffer	128 lines	256 lines	No action necessary
LEON3 Integer Unit	Pipeline restart on correction	Correction without pipe-line restart	No action necessary
LEON3 AHB Trace Buffer	128 lines	256 lines	No action necessary

Attribute	UT699	UT699E	Recommendations
Core Voltage	2.5V	1.2V	Change core supply voltage
Memory interface I/O drivers	12mA	24mA	Evaluate PCB signal integrity and consider adding series termination resistors
Memory Controller Register 3, factory test bit (bit 28 of MCFG3)	Not Supported	Supported	Must be set to '0' for proper memory operations
SpaceWire Receive Clock to system clock relationship	Derived RX clock (RxCLK £ 2 x SYS_-CLK)	No longer tied to SYS_-CLK, relationship is now related to the SPW_CLK	SPW_CLK ³ 3/4 receive data rate (max)
SpaceWire IP Core	GRSPW (with RMAP present on ports 2 and 3)	GRSPW2 (with RMAP on 4 ports)	No action necessary
SpaceWire Timer and Disconnect Register	Present	Not used	No change unless software is dependent on register values
SpaceWire Write Synchronization Error bit	Present	Not used	No action necessary
SpaceWire RMAP error code	No support for RMAP invalid destination address error code	RMAP invalid destination address error code is supported	No action necessary
SpaceWire SPW_CLK to system clock relationship	SPW_CLK £ 4 x SYS_-CLK	SPW_CLK £ 8 x SYS_-CLK	No action necessary
SpaceWire Control Register Port Loopback bit (bit 22)	Not Supported	Supports internal loopback	Ensure initialization routines set this feature disabled ('0') for normal operations
Ethernet Debug Communications Link	Not Supported	Supported	No action necessary
PCI Parity Error (PERR) Flag	Target parity error notification not supported	Target parity error notification is supported	No action necessary for current designs
CAN Transmit Interrupt clear race condition	CAN OC: interrupt can be cleared before read	CAN Transmit Interrupt operates normally	No action necessary
Plug & Play IP core detection	Cores detected normally	Inactive cores detected	No action necessary

2.0 Hardware Considerations: LEON 3FT

2.1 Cache Size

The UT699 has 8kB of instruction cache and 8kB of data cache configured as 2-way set associative. The UT699E has 16kB of instruction cache and 16kB of data cache configured as 4-way set associative. The CPU core automatically manages cache memory when cache is enabled. Therefore, no modification to code is required. If application software makes direct accesses to cache for diagnostic purposes, software designers may choose to redesign these applications to take advantage of the larger cache sizes.

2.2 Data Cache Misses

For the UT699, a data cache miss that occurs on a 32-bit word read results in the cache fetch of a single word. A similar cache miss in the UT699E results in the fetch of an entire cache line (4 words). This enhancement potentially reduces the frequency of access to memory and improves performance when accessing SDRAM. Additionally, system designers should evaluate latency changes affecting real-time systems.

2.3 Cache Snoop

The UT699E provides the capability to perform automated bus snooping of the AHB bus. This feature monitors the AHB for transactions involving cachable address space and forces the cache to be marked as invalid when a bus master performs a write on the associated address. Cache Snoop is not supported for the UT699.

2.4 Cache Freeze

The UT699 has the ability to freeze both address and data cache. The UT699E can only freeze the instruction cache. The ability to perform a cache freeze is a feature used to reduce the impact of interrupts on software timing and to simplify worst case execution time (WCET) analysis. Enabling cache freeze for the UT699E will not prevent the data cache from being updated. For information regarding the effect this will have to software, see Section 6.

2.5 Pipeline Load Delay

The pipeline data load delay is reduced from 2 clock cycles in the UT699 down to 1 clock cycle for the UT699E.

2.6 Memory Management Unit (MMU)

Translation Lookaside Buffer (TLB) is increased to 16 entries for the UT699E, improving performance in applications using the MMU by allowing for a higher hit TLB rate. The UT699 supports only 8 entries.

2.7 Floating Point Unit (FPU)

The UT699 FPU unit requires a compiler workaround to ensure single-precision floating point data is stored correctly in the FPU. The workaround inserts NOPs between FPU load and store operations. The UT699E does not require a special workaround for FPU operations, permitting optimal performance for FPU operations. For more information regarding the effect this will have to software, see Section 6.

2.8 Register File

The UT699E uses a Triple Modular Redundant (TMR) architecture to protect the Integer Unit register files against errors due to Single Event Upset (SEU). This change provides a reduction in processor execution time since the instruction(s) don't need to be restarted. The UT699 uses a 7-bit BCH EDAC architecture to protect against errors due to SEUs. Although robust, the 7-bit BCH increases the processor execution time in the event of a SEU.

2.9 Multiplier

The Multiplier used for the UT699E is improved to permit operations on 32-bit words at 1 clock cycle per instruction. This improvement is transparent to software. The UT699 permits operations on 16-bit words at 5 clock cycles per instruction.

2.10 Integer Unit (IU)

The UT699E IU is capable of correcting data without a pipeline restart to support register file error correction where the UT699 causes a pipeline restart each time data is corrected.

2.11 Instruction Trace Buffer

The UT699E Instruction Trace Buffer attached to the IU consists of 256 lines deep by 128-bits wide storage to form a circular buffer used to capture instructions used by the IU. In contrast, the UT699 Instruction Trace Buffer is a 128 lines deep by 128-bit wide circular buffer. This enhancement permits monitor of longer instruction history than the UT699.

2.12 Core Voltage

Core voltage used in the UT699 has been reduced to 1.2V for the UT699E. Power pin functionality remains unchanged between the two devices which will require a designer to change the VDDC pin power supply from 2.5V to 1.2V. The reduction in core voltage results in a reduction of core power consumption by as much as 87%, when compared to the UT699.

2.13 AHB Trace Buffer

The UT699E AHB Trace Buffer attached to the AHB controller consists of 256 lines deep by 128-bits wide storage to form a circular buffer used to capture AHB transactions. In contrast, the UT699 AHB Trace Buffer is a 128 lines deep by 128-bit wide circular buffer. This enhancement permits monitoring of longer instruction histories than the UT699.

3.0 Hardware Considerations: Memory Interface

3.1 Memory Interface Drivers

The memory interface output buffers in the UT699 are implemented with 12mA drivers. The UT699E output buffers are improved with 24mA drivers to meet the demands of higher capacitive loads. In a more lightly loaded system, the printed circuit board design might require higher valued series resistors on the outputs in order to maintain desired signal integrity. Frontgrade recommends that system designers make use of the UT699E IBIS model in order to determine required changes for signal integrity.

3.2 Memory Controller Register 3 (MCFG3)

The UT699E is designed with the same memory controller IP as used for the UT700. The IP has the capability of performing Reed-Solomon EDAC operations. However, the additional EDAC pins required to perform this operation are internally terminated. The UT699E is capable of only BCH EDAC. Memory controller register 3 is used to configure the SDRAM, enable EDAC, and perform EDAC related testing. Functionality related to bit 28 of MCFG3 has been added for factory test. Bit 28 is not writable in the UT699. Section 6 describes any concerns and considerations affecting software.

4.0 Hardware Considerations: SpaceWire

4.1 SpaceWire Clock

The GRSPW core in the UT699 uses a transmit clock, SPW_CLK, input to clock the transmit subsystem. The receiver clock is a recovered clock that is generated from the data and strobe inputs. The receive clock is limited by the system clock frequency, $RxCLK \leq 2 \times SYS_CLK$, for the UT699. The SPW_CLK used by the UT699 is limited by the SYS_CLK to $SPW_CLK \leq 4 \times SYS_CLK$.

The GRSPW2 core in the UT699E uses the SPW_CLK to clock the transmit subsystem and to sample the receive signals for the receive subsystem. The receive data rate for the UT699E is limited by the SPW_CLK to $4/3 \times SPW_CLK$. The SPW_CLK for the UT699E cannot be greater than 8 times the system clock frequency.

4.2 RMAP on all Four SpaceWire Ports

RMAP protocol is only supported on SpaceWire ports 2 and 3 in the UT699. The UT699E supports the RMAP protocol for all SpaceWire2 ports (i.e. 0, 1, 2, and 3). Section 6 describes any concerns and considerations effecting software.

4.3 Timer and Disconnect Register

The Timer and Disconnect Register is no longer used with the GRSPW2 core for the UT699E. This register is not needed as the configuration is done by setting the CLKDIVSTART field in the Clock Divisor Register. Section 6 describes any concerns and considerations affecting software.

4.4 Write Synchronization Error (WE) Bit Not Used

The Write Synchronization Error bit in the SpaceWire Status Register is not used with the GRSPW2 core in the UT699E. The UT699 uses this bit to detect a write synchronization error condition related to each GRSPW core. This bit will always be read as '0' in the case of the GRSPW2 core used with the UT699E. Section 6 describes any concerns and considerations affecting software.

4.5 SpaceWire Port Loopback

The SpaceWire2 core implemented in the UT699E now supports an internal loopback feature. This feature provides the capability to internally loop the transmit output to the receive input. This feature is enabled by setting the bit 22 in the SpaceWire Control Register to '1'. The internal loopback feature is not supported by the SpaceWire core in the UT699.

4.6 SpaceWire RMAP Error Code

UT699 does not support RMAP invalid destination address error code. The UT699E supports RMAP invalid destination address error code.

5.0 Additional Hardware Considerations

5.1 Ethernet Debug Communications Link (EDCL)

The UT699E now supports EDCL. EDCL permits access to the Debug Support Unit (DSU) and other system resources using the Ethernet interface. The UT699 does not support this feature.

5.2 PCI Parity Error Flag

The UT699 is not capable of decoding a parity error signal sent by a target device. The UT699E now supports the requirement to decode a parity error signal sent by a target device.

5.3 CAN Transmit Interrupt

The CAN core in the UT699 exhibits a race condition that causes the Transmit Interrupt to be cleared before read. A read access to the Interrupt Register in the same clock cycle as the transmitter logic updates the interrupt register can cause the bit to be cleared. The race condition is corrected for the UT699E.

6.0 Software Considerations

6.1 Data Cache Misses

System software must ensure that all cachable data memory is properly initialized to ensure that data words that were previously never read during execution may now be read because they align to same cache line as the word that triggered the miss such as instances where the top of used RAM is not aligned to a cache line boundary. While using memory that is EDAC protected, ensure all words of all accessed cache lines are fully washed after power-up to avoid EDAC errors

6.2 Cache Snooping

Enabling cache snooping legacy UT699 code can be recompiled to use ordinary loads (LD) when accessing DMA'd data instead of using special load instructions that force a cache miss (i.e. LDA ASI=1). That gives performance benefits by serving reads from cache when the data has not been changed (for example when polling a potentially unchanged descriptor or data buffer), and it may allow some reduction in code size because the normal load opcode has more addressing modes (e.g. `ld [%reg1+%reg2]` and `ld [%reg1+<14-bit const>]`)

6.3 Cache Freeze

The UT699E does not have the ability to freeze the data cache while freezing the instruction cache. Take this into consideration while doing WCET analysis of a code segment which has IRQs enabled. None of the Frontgrade BSPs or OSeS use this feature. Therefore, custom code would potentially be impacted.

6.4 FPU

The Floating point controller errata does not affect the UT699E. Therefore, recompilation of legacy code without the `- mtune-ut699` option optimizes performance.

6.5 Memory Configuration Register 3

Bit 28 is writable in the UT699E. Inadvertently enabling bit 28 in MCFG3 cause memory access errors. To prevent this from occurring, system software must ensure bit 28 is always set to a '0'. Bit 28 is read only in the UT699 and always reads as '0'.

6.6 SpaceWire RMAP

Each of the four SpaceWire controllers has a dedicated SpaceWire Control Register that contains several bits pertaining to RMAP configuration. These bits are ignored for SpaceWire ports 0 and 1 in the case of the UT699. However, system software must properly set these bits for all four SpaceWire ports in the case of the UT699E, as all four ports can utilize the RMAP protocol.

SpaceWire Timer and Disconnect register

The SpaceWire Timer and Disconnect register is not used with the UT699E. The only potential problem with using existing code written for the UT699 would be the case where system software attempts to write a value to this register and then read it back. Otherwise, no changes to SpaceWire code are necessary with this register.

Write Synchronization Error bit

The Write Synchronization Error bit (bit 6 of the SpaceWire Status Register) previously used with the UT699 is no longer used in the case of the UT699E. No changes to system software are necessary as this bit was previously set to a '1' indication an error and will now always be read as a '0'. Therefore, system software will never be notified of an error.

SpaceWire RMAP Packet Error Code

Drivers or code monitoring the status of RMAP packets should be updated to support the RMAP invalid destination address error code. Otherwise, no action is required.

SpaceWire Port Loopback

Initialization software written for the UT699 should be evaluated to ensure bit 22 is not set during normal operations.

7.0 Development Tool Considerations

7.1 Plug & Play IP Core Detection

The UT699E has a SPI core and a MIL-STD-1553 core that are permanently disabled. Although disabled, the cores are detected and reported by any Plug & Play scanning routines, such as routines used by GRMON. Neither the user nor system software need take any action related to these cores.

Revision History

Date	Revision #	Author	Change Description	Page #
1/15/2015	1.0.0	N/A	Initial Release	

Frontgrade Technologies Proprietary Information Frontgrade Technologies (Frontgrade or Company) reserves the right to make changes to any products and services described herein at any time without notice. Consult a Frontgrade sales representative to verify that the information contained herein is current before using the product described herein. Frontgrade does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by the Company; nor does the purchase, lease, or use of a product or service convey a license to any patents, rights, copyrights, trademark rights, or any other intellectual property rights of the Company or any third party.