FRONTGRADE

APPLICATION NOTE

UT65CML8X8FD 3.125 Gbps Crosspoint Switch (XPS) – Cold Spare Functionality of the High-Speed I/O

5/9/2022

Version #:1.0.0

Table 1: Cross Reference of Applicable Products

Product Name	Mfr. Part # (UT54ACS)	SMD # (5962-)	Device Types	Internal PIC* #
UT65CML8X8FD 3.125 Gbps Crosspoint Switch (XPS)	UT65CML8X8FD	17213	01, 02	WQ04A

***PIC = Product Identification Code**

Overview

The purpose of this Application Note (AN) is to provide some general background information and a brief description of the recommended operation and implementation of Redundancy and Cold Sparing for the UT65CML8X8FD Crosspoint Switch (XPS) high-speed Inputs/Outputs (I/Os).

Technical Background

Cold Sparing of Redundant devices in a point-to-point channel is a proven method of building fault tolerant data links and networks in high reliability systems, such as space-based applications. A common topology for Cold Sparing implementation is for the Primary devices to be powered-up (ON) and active, while the Redundant (Spare) devices are powered-down (OFF) and inactive. Cold Sparing for LVDS point-to-point channels at data rates up to 400 Mbps has typically been achieved via the topology shown in Figure 1, while the topology of Figure 2 is more commonly used in higher data rate systems, for reasons described below.

Cold Spare Operation

Redundancy via Cold Sparing has been used successfully over many years for Complementary Metal Oxide

Semiconductor (CMOS) and Low-Voltage Differential Signaling (LVDS) I/O logic standards. The application is in highrel., space flight hardware, at data rates up to approximately 200 Mbps for CMOS and 400 Mbps for LVDS, respectively.

However, Cold Sparing hasn't been commonly applied to or implemented in high-speed, multi-Gbps Current-Mode Logic (CML) I/Os to date, such as in FPGA SERDES, or specifically for the XPS operating at 3.125 Gbps, for example. These new parts support the VITA 78 / SpaceVPX standard, among others. Figure 1 and Figure 2 show the two main topologies for Cold Sparing of legacy LVDS I/O signaling standard links as part of a data link redundancy implementation.

As shown in these figures, for lower data rate LVDS links, the Primary and Redundant Transmitter (TX) and Receiver (RX) I/Os are typically configured as separate devices, i.e.: two separate TX devices and two separate RX devices.

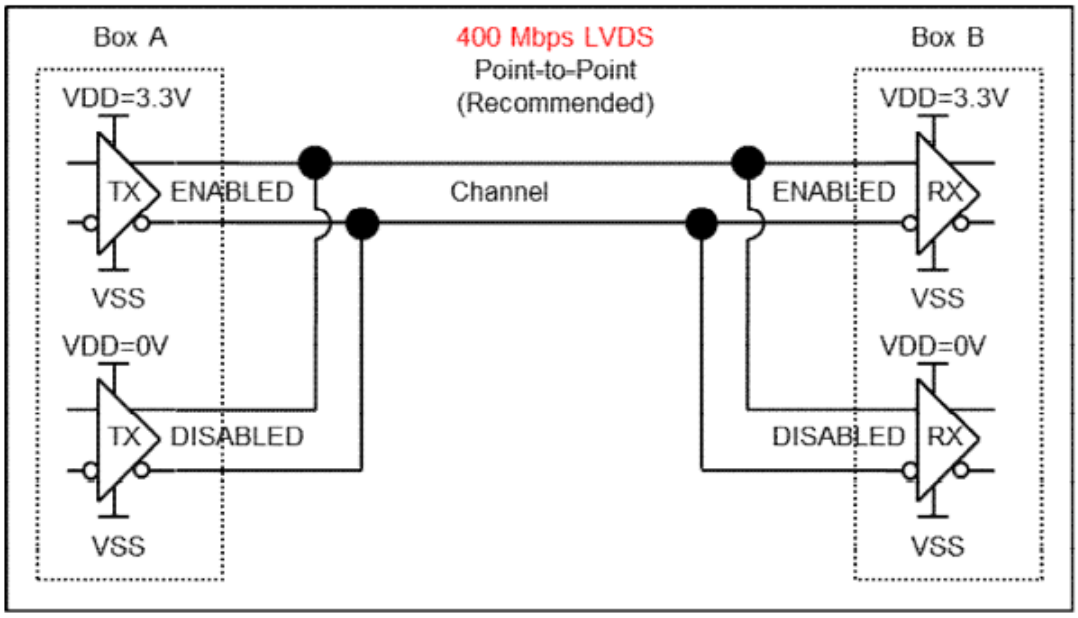

Figure 1: 400Mbps LVDS Redundancy in Point-to-Point Signaling Channels **(Recommended)**

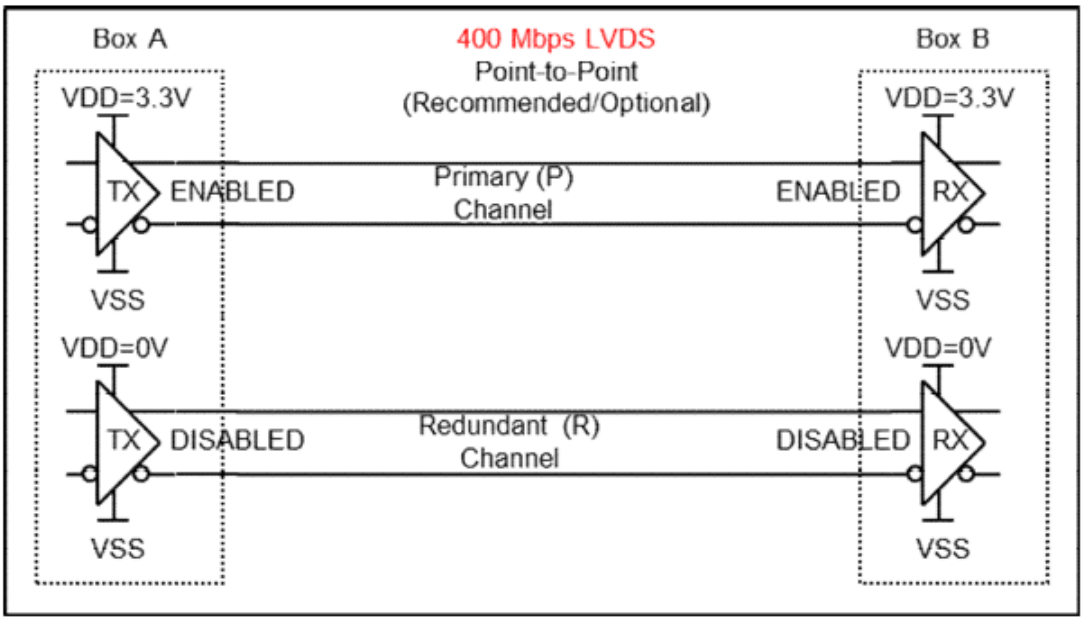

Figure 2: 400Mbps LVDS Redundancy in Point-to-Point Signaling Channels **(Optional)**

Figures 3 - 6 show example topologies for the CML XPS, including both recommended, and not recommended methods of achieving Redundancy for multi-Gbps CML data links.

The Primary and Redundant TX (RX) channels may be on either a) two separate devices, or b) a single shared device, i.e.: two separate devices with a single TX (RX) channel each, or one single device with two TX (RX) channels. The selected topology depends on system requirements and actual redundancy implementation.

Figure 3 indicates the preferred, point-to-point data channel configuration, which uses Primary and Redundant channels and devices in a half-duplex topology. Figure 4 shows an alternate Redundancy implementation. These are the two recommended Cold Spare Mode topologies for the XPS device.

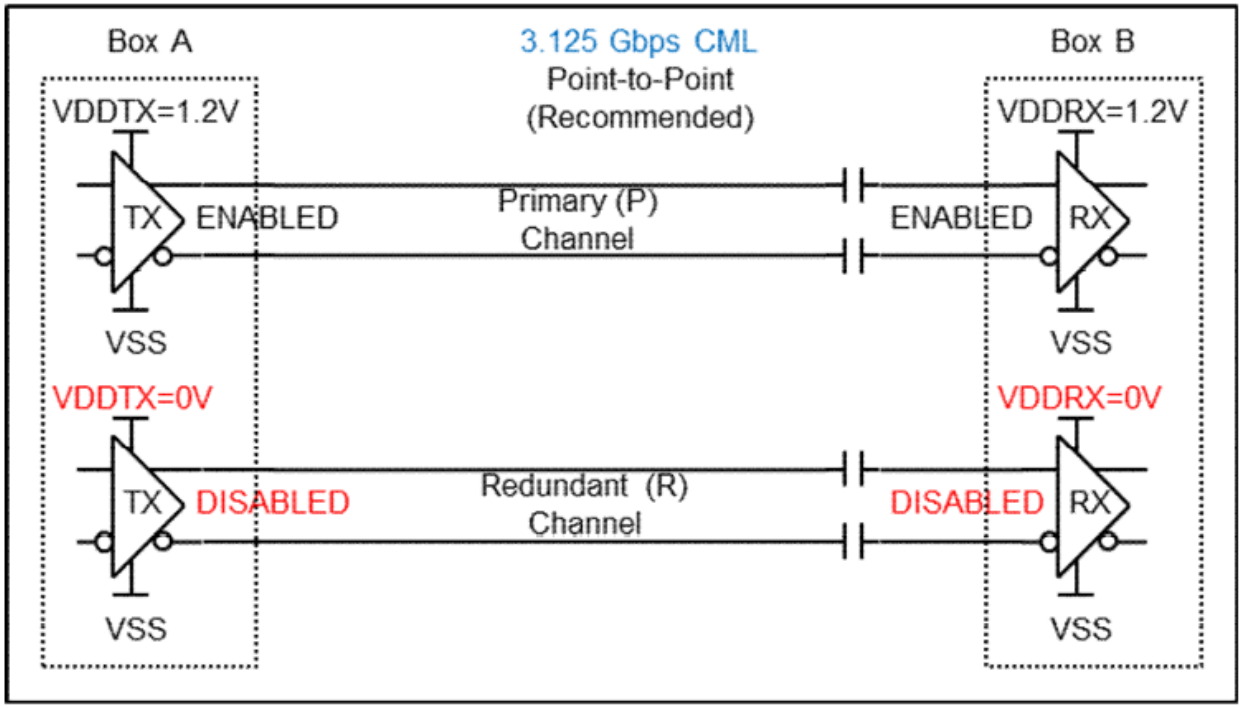

Figure 3: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels **(Recommended).**

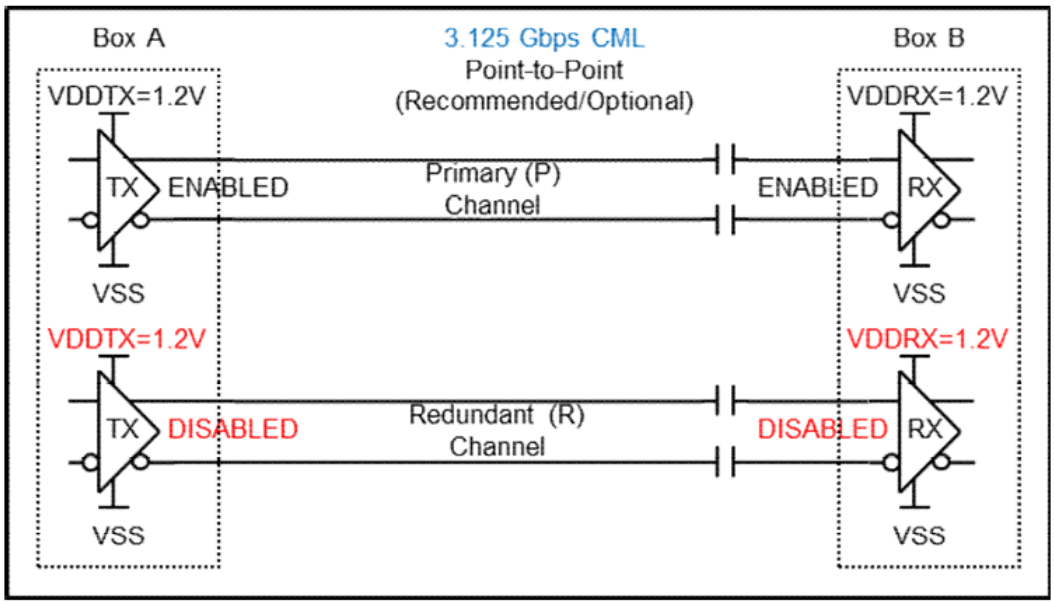

Figure 4: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels (Optional).

The example of Figure 5 shows a redundancy topology that's neither recommended nor supported. The main issue

is that the Signal Integrity (SI) of the point-to-point channel is compromised for the 3.125 Gbps data rate application. This is due to excessive loading, impedance mismatch, and discontinuities from the I/O of the Redundant devices on the common, point-to-point channel. For example, all CML TX/RX I/O include 100Ω differential terminations, so the TX/RX termination impedance is halved due to parallel devices if the Redundant device termination resistors aren't isolated via the high impedance (high-Z) mode control circuit. The problem is aggravated at higher data rates where channel impairments have an increasingly detrimental effect.

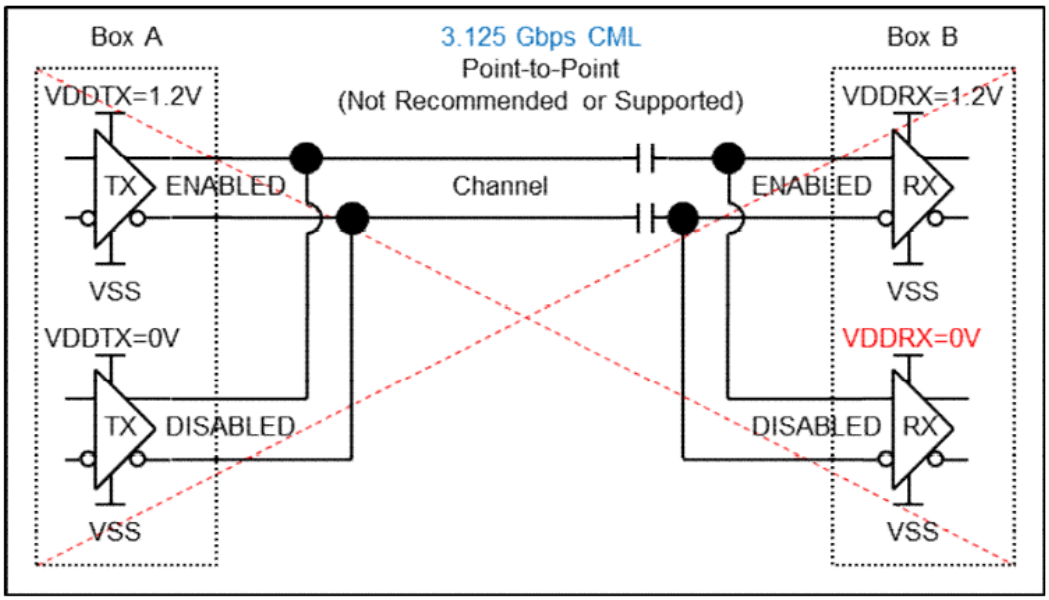

Figure 5: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels (Not Recommended or Supported)

Cold Spare Specific Use Case for VDDTX=1.2V±5%

At Customer request, Frontgrade Design Engineering performed circuit analysis and determined that the XPS can support the following Cold Spare topology, with all XPS integrated circuit (IC) devices remaining within safe operating area (SOA), provided that the following requirements, as described below, are observed. Please see Figure 6.

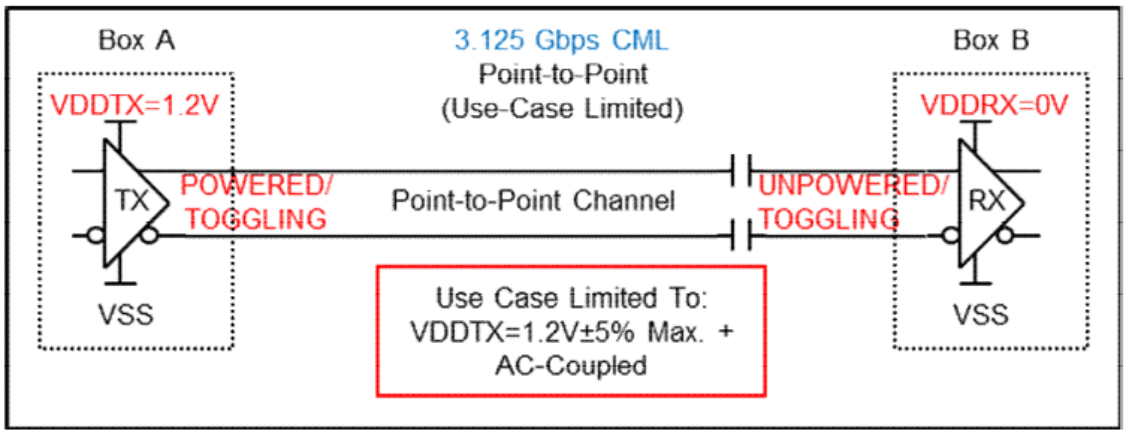

Figure 6: 3.125 Gbps CML Redundancy in Point-to-Point Signaling Channels (Specific Use Case of VDDTX=1.2V±5% Max.)

In this use case, the powered (VDDTX=1.2V) and toggling near-end TX transmitter is driving the far-end unpowered (VDDRX=0V) and inactive RX receiver input. In normal operating mode, the Frontgrade XPS device has been shown to operate with good jitter and bit error rate (BER) performance for VDDTX=VDDRX=1.2V (±5%), so the VDDTX limitation doesn't adversely impact on BER for systems that can operate at this VDDTX voltage at the lower end of the specified VDDTX range.

Configuring the XPS Prior to Sending or Receiving High-Speed Data -

Laboratory measurements show that the SPI port will correctly configure the internal XPS registers with only the core VDD (VDD), bias generator VDD (VDDA_BIAS), and the 2.5V SPI VDD (VDD_25) supplies powered-on. There is no adverse Reliability impact when the TX Analog (VDDATX) and TX Output (VDDTX) power domains are unpowered while these other three power domains are powered-on.

When RX and TX power domain supplies are powered-off, the core power dissipation will be slightly elevated. This is due the CMOS circuitry in the core having undefined inputs. In this semiconductor process technology, that usually means the NMOS device gates float up into conduction.

Example: Full Redundancy A-B Cross-Strapping Using XPS Devices

Figure 7 shows an example of full redundancy A-B cross-strapping using two XPS devices in a 3.125 Gbps full duplex, x4 channel data link. This is reproduced from the XPS Data Sheet, p.7, Figure 8. This diagram is provided for reference and ties together the XPS TX/RX I/O block redundancy topologies with broader system-level architectures and fault tolerance requirements.

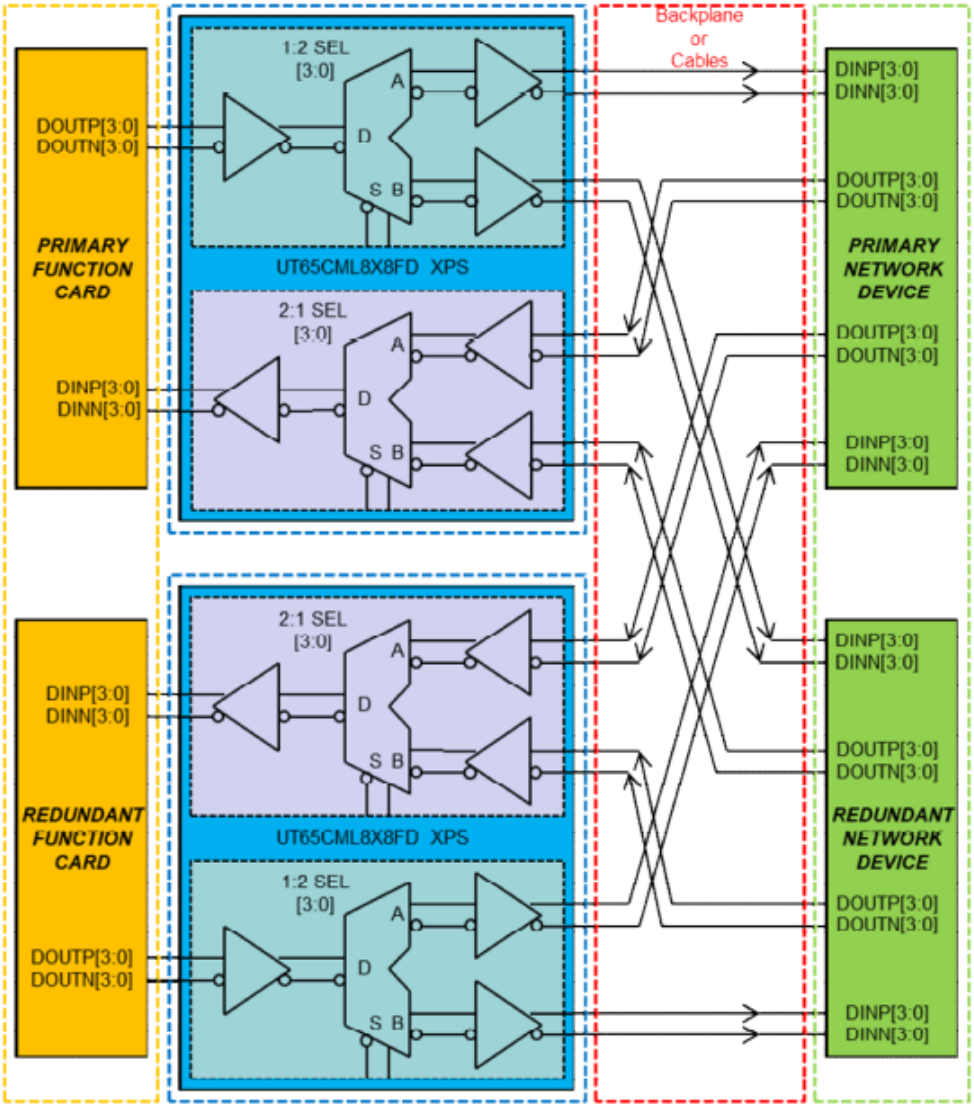

Figure 7: Example: Full Redundancy A-B Cross-Strapping Using Two XPS Devices 3.125 Gbps, 4 Channels Each Data Path, Full Duplex

The block diagram of Figure 8 provides another example of full data path redundancy using the XPS device. In this case, the data path is a point-to-point, unidirectional, or simplex channel. This topology can be implemented with either x2 or x4 separate XPS devices, depending on system-level fault tolerance requirements. Only one half of the XPS device is required per functional block. Unused XPS data channels, or one half of the XPS device for the x4 XPS device configuration, along with the x2 unused RX inputs, can be powered-down to reduce power consumption.

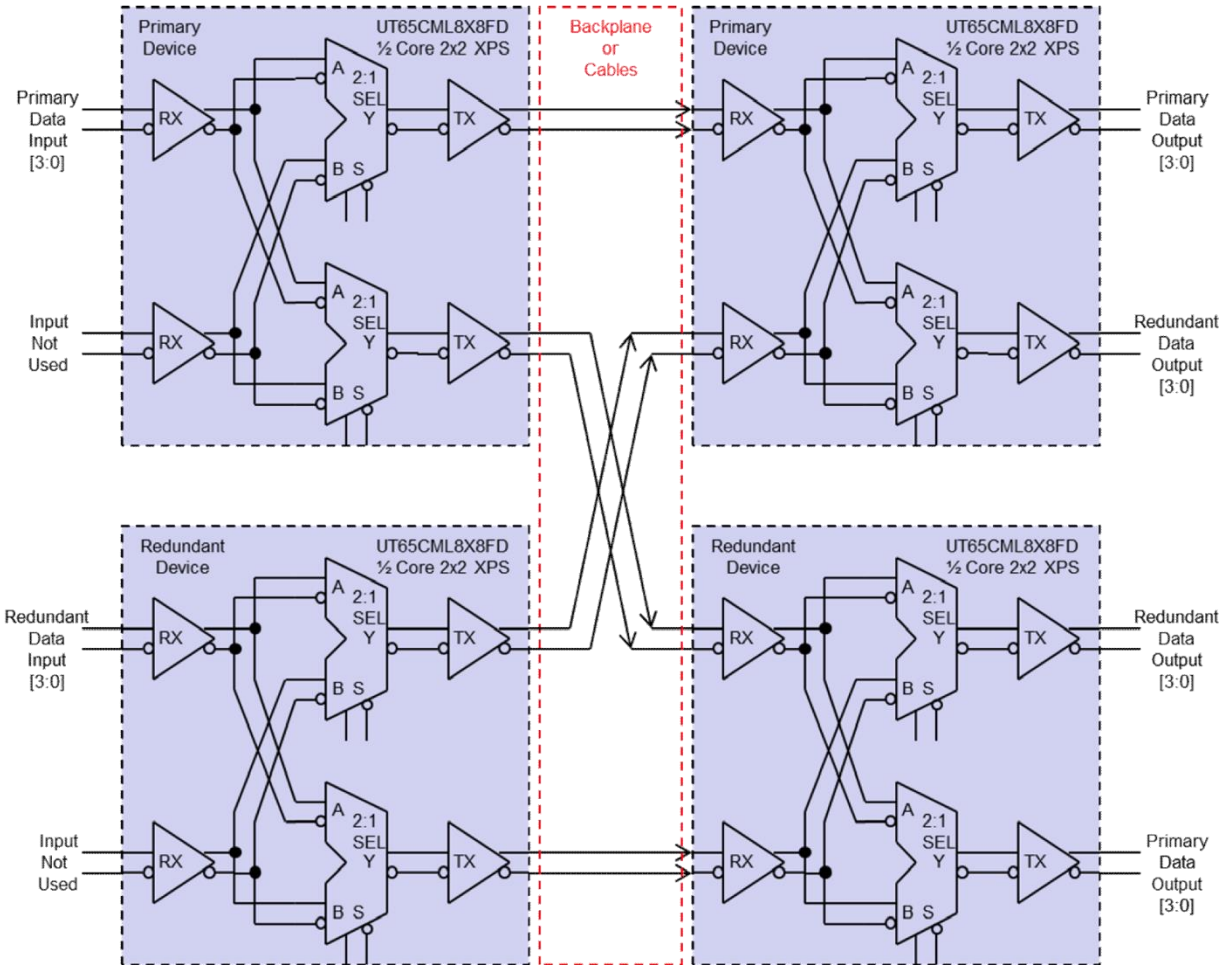

Figure 8: Example: Full Redundancy A-B Cross-Strapping Using Two XPS Devices 3.125 Gbps, 4 Channels Each Data Path, Simplex, Point-to-Point

CML TX/RX Channel – XPS Notional Circuit Schematic

CML is a point-to-point only signaling I/O logic standard. CMOS and LVDS, for example, can be point -to- point, multi-drop, or multi-point. These different topologies can be used for CMOS and LVDS I/O logic standards because they operate at much lower data rates – approximately one eighth of the CML XPS. Figure 9 shows a notional schematic for the Frontgrade CML-based XPS, and would generally apply to similar high-speed CML digital links, including other SpaceVPX/VITA 78 compatible Crosspoint Switches, SERDES, Re-drivers, Re-timers, etc. Note that all inputs are shown as AC-Coupled, which is required by many high-speed signaling protocols, such as XAUI, for example. ESD protection diodes are shown attached to the XPS high-speed I/O signal pins.

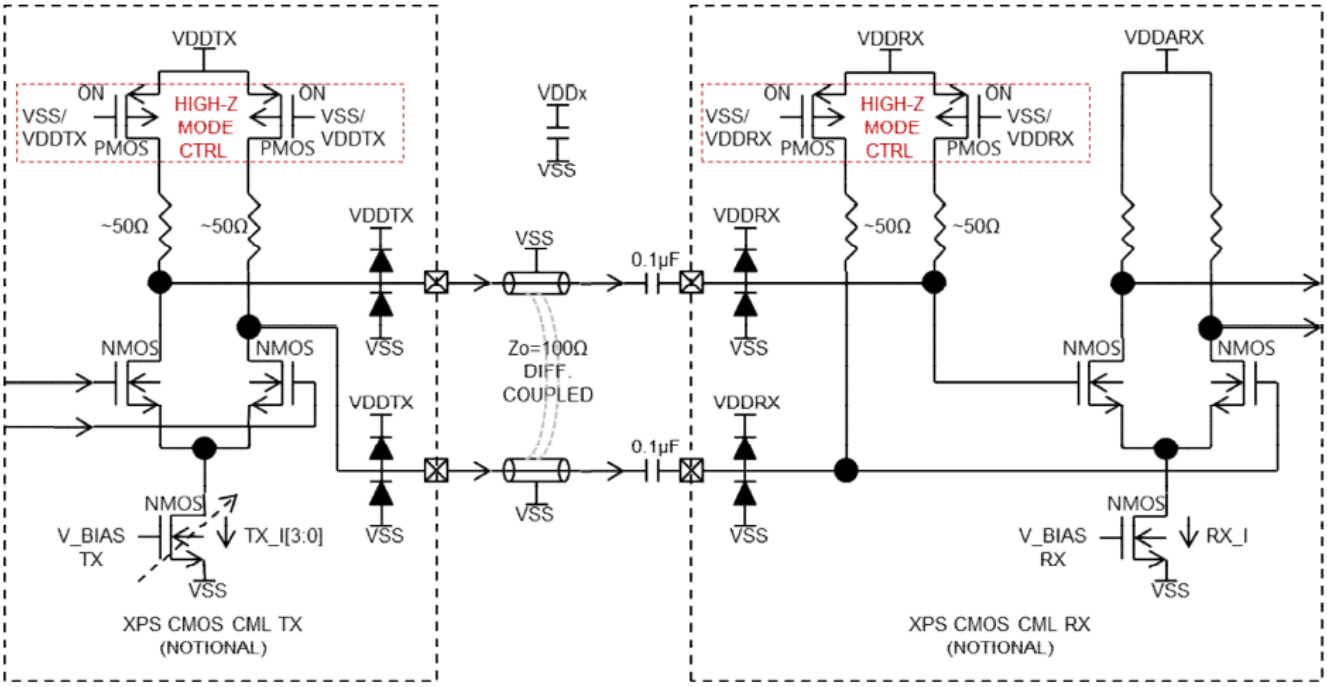

Figure 9: 3.125 Gbps XPS CML TX to RX Point-to-Point Channel – Notional Schematic

Summary and Conclusion

Implementing Redundancy via Cold Sparing methods and techniques doesn't directly translate from lower data rate CMOS and LVDS serial data links to CML multi-Gbps systems, as signal integrity (SI) requirements become more stringent at higher data rates. In addition, the SpaceVPX standard includes its own system-level redundancy, and fault tolerance functions. Also, the primary function of the XPS IC is as an A-B Redundant switch. Therefore, in view of these considerations, Redundancy and Cold Sparing for 3.125 Gbps SpaceVPX (VITA 78) networks must be determined in the context of the overall ecosystem.

For the intended A-B redundancy application in the general case, the XPS device can be powered-down for Cold Sparing (VDDx=0), as the high-speed I/Os are AC-coupled. However, for the point-to-point high-speed channel, the near-end TX output must not be toggling when driving the powered-down, far-end RX input. The only exception to this requirement that is allowed is for the specific use case as described in Section 3.1 and as shown in Figure 6.

The technical information related to Cold Sparing of the XPS device high-speed I/Os, in the context of SpaceVPX network applications is described in this AN. While the UT65CML8X8FD XPS wasn't specifically designed to support Cold Sparing, a description of limited Cold Spare functionality for the high-speed I/Os is given in Section 3 of this document. The SPI Port and all other low-speed I/O signals do not support Cold Sparing. Please observe all electrical requirements for these signals as spelled out in the Data Sheet (DS) and SMD specifications.

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Revision History

Date	Revision #	Author	Change Description	Page #
01/08/2019	1.0.0	BRM	New	
01/14/2019	1.0.1	BRM	Added Captions (Figure 1-N) + Cross-references (hyperlinks) to Figure Titles	
05-09-2022	2.0.0	BRM	Added Use case for VDDTX=1.2V±5% + other editorial changes	