FRONTGRADE

APPLICATION NOTE

AN_LVDS-012-01

Calculating Skew Margin for a UT54LVDS217 and UT54LVDS218 Link

6/20/2011

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
3.0V Serializer	UT54LVDS217	5962-01534	01, 02	WD11,WD13
3.0V Deserializer	UT54LVDS218	5962-01535	01, 02	WD12,WD14

1.0 Overview

Receiver Input Skew Margin (RSKM) is defined as the total available margin after accounting for transmitter pulse (TPPosN), receiver strobe (RSPosN), jitter, and interconnect media dependent factors. To ensure proper functionality of a LVDS link, the system designer must consider the factors that can cause errors during the high speed data transmission between the UT54LVDS217 Serializer (SER) and UT54LVDS218 Deserializer (DES).

This application note provides jitter, TPPosN, RSPosN data, and an example calculation for receiver skew margin (RSKM).

Note: The data in this application note is not guaranteed and intended to be used as a REFRENCE ONLY.

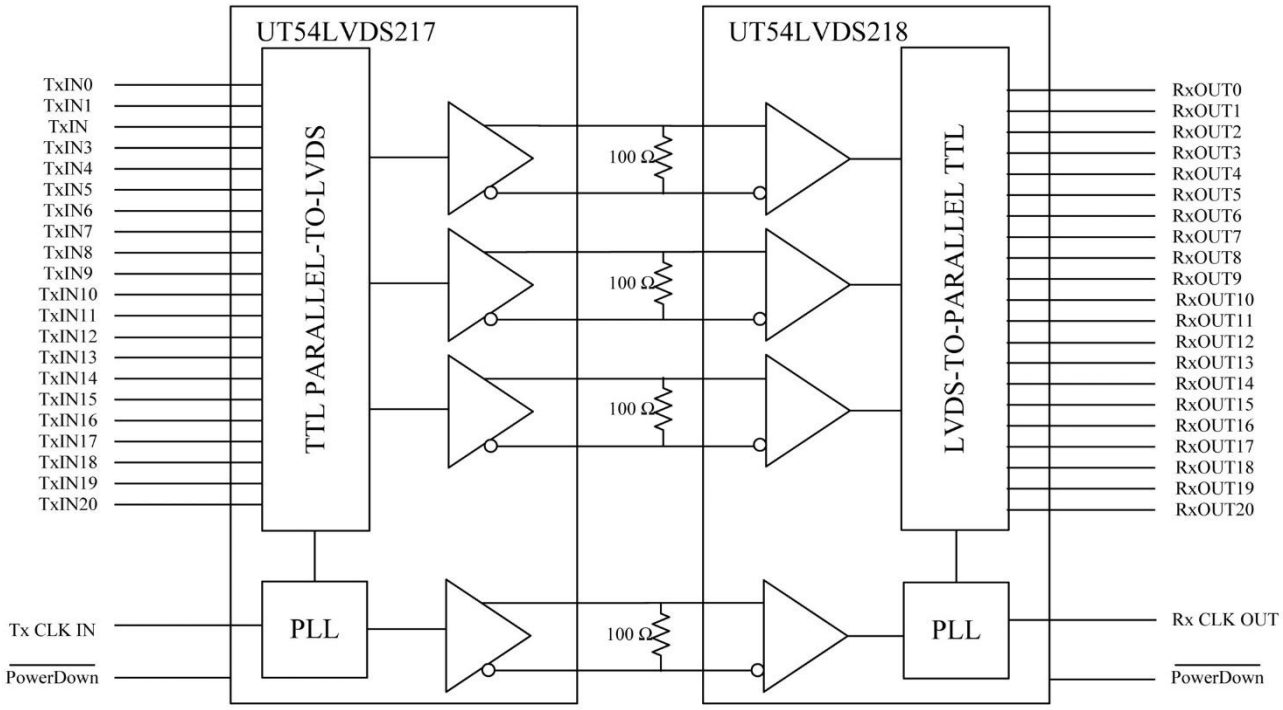

Figure 1. Standard UT54LVDS217 and UT54LVDS218 Configuration

2.0 RSKM Factors

Ideally the receiver strobe would occur directly in the middle of the strobe position window (RSPosN(MIN) and RSPosN(MAX)) and sample data correctly. Due to several factors that decrease the width of the sampling window, a skew margin is required to ensure valid data is sampled correctly by the UT54LVDS218 receiver. Figure 2 details the main factors that reduce the receiver strobe position window. The values calculated for variables A, B, C, and D must be divided in half and distributed on each side of the ideal strobe position.

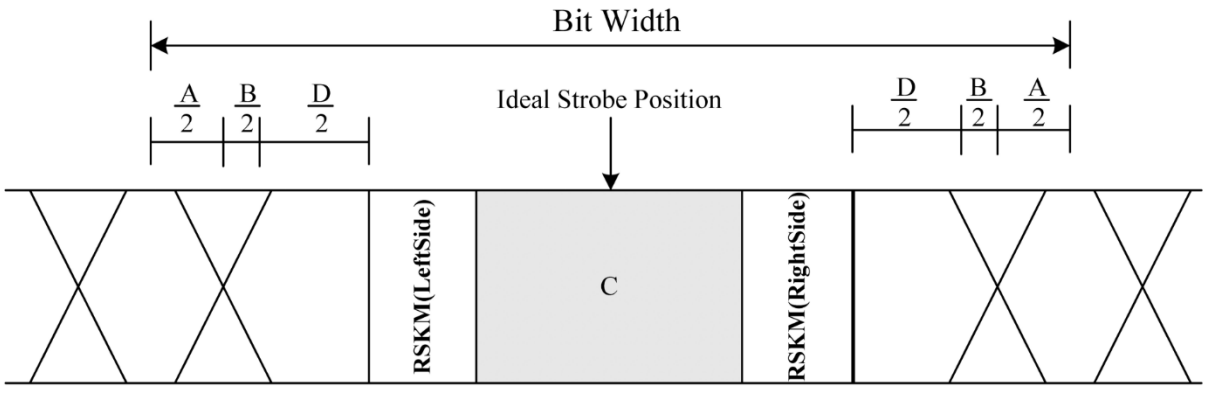

Figure 2. UT54LVDS218 RSKM diagram

A = Transmitter Pulse Variation (from ideal) TPPosN(MAX) - TPPosN(MIN)

A = TPPosN(MAX) - TPPosN(MIN)

B = Cable Skew, (typically 10-40ps per foot), and ISI (Inter symbol interference) both are media dependant.

B = SKEW * Cable Length

C = Set up and hold times for UT54LVDS218. (RSPosN(MIN)) and (RSPosN(MAX))

C = RSPOSn0(MAX) to RSPosN(MAX)

D = Total Source Clock Jitter, from UT54LVDS217

D = (See Figure 3)

3.0 EXAMPLE Calculating Bit0

This example estimates the skew budget for bit 0 transferred from the UT54LVDS217 to the UT54LVDS218 operating at 25MHz. Please reference Application note AN-LVDS-011 “UT54LVDS217 Transmitter Pulse Position (TPPosN) and UT54LVDS218 Receiver Strobe Position (RSPosN) Estimate Over Frequency” for TPPosN and RSPosN values at different frequencies.

Calculate Bit Width:

25MHz → $\frac{1}{25MHz}$ = 40.00ns

There are 7 bits in the bit stream:

Bit Width = $\frac{40.00ns}{7}$ = 5.7143ns = 5714.3ps

Using the "Estimated RSPosN" and "Estimated TPPosN" figures in application note AN-LVDS-011 we obtain the estimated pulse and strobe positions for the UT54LVDS218 and UT54LVDS217 operating at 25MHz.

A:

TPPon0(MAX)@25MHz = 0.08ns From AN-LVDS-011

TPPos0(MIN)@25MHz = -0.05ns From AN-LVDS-011

TPPon0(MAX)-TPPos0(MIN) = (0.08ns)-(-0.05ns) =0.13ns

$\frac{A}{2} = \frac{0.13ns}{2}$ = = 0.065ns = 65ps

B:

Assume the UT54LVDS217 and UT43LVDS218 are connected using a 1 meter cable and the cable characteristics are listed as 13ps SKEW/foot and ISI=0.

B = (13ps)*(3.2808 foot) = 42.65ps SKEW from the 1 meter cable

$\frac{B}{2} = \frac{42.65}{2}$ = = 21.32ps

Note:

B will change depending on system interconnect media. Calculate the amount of skew per foot, inch, mm, meter, etc for the interconnect layer. Cable Skew changes depending on the cables or PCB traces in the system. Contact the cable manufacturer or figure out your PCB trace parasitics and use that number here. This example assumed a 1 meter cable with 13ps SKEW/foot.

C:

RSPOSn0(MAX)@25MHz = RSPosN(MAX) for Bit0 = 2.77ns = 2770ps From AN-LVDS-011

RSPOSn0(MIN)@25MHz = RSPosN(MIN) for Bit0 = 1.72ns = 1720ps From AN-LVDS-011

D:

For this example assume temperature is 25℃, VDD=3.3V, the Serializers jitter is estimated using Figure 3 below. Please note that jitter for the UT54LVDS217 varies little over temperature, so the data at 25℃ provides a sufficient estimate.

217Jitter (25MHz) = $\frac{\text{Jitter (20MHz)} + \text{Jitter (32.4MHz)}}{2} = \frac{(303.7ps) + (179.8ps)}{2}$ = 241.75ps

$\frac{D}{2} = \frac{241.75ps}{2}$ = = 120.87ps

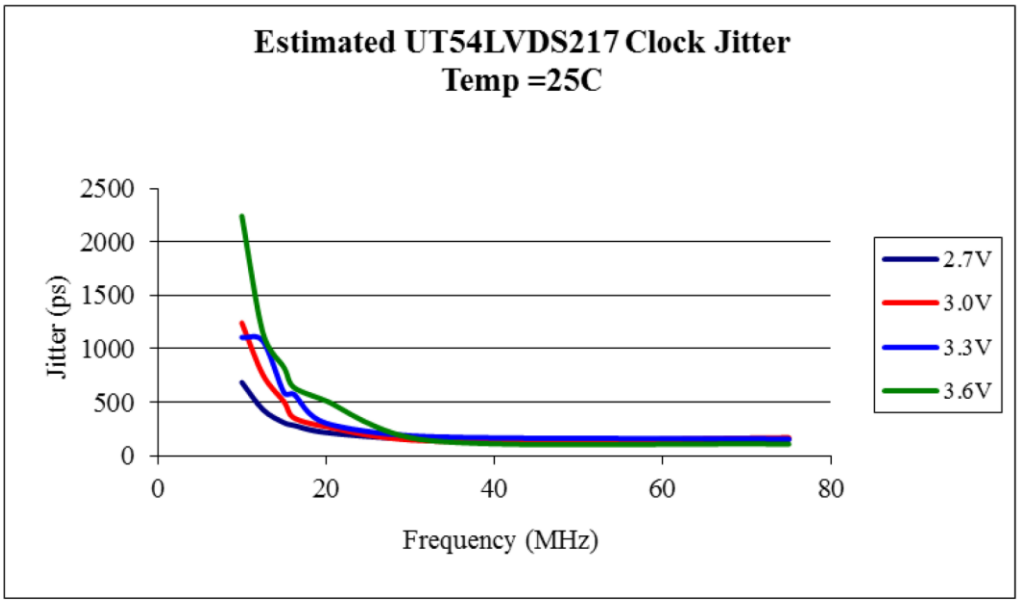

Figure 3. Estimated UT54LVDS217 SER Clock jitter, T=25℃

Table 2. Estimated UT54LVDS217 SER Clock Jitter, T=25℃ – Tabulated Data

T=25℃	Est. UT54LVDS217 SER Clock Jitter (ps) VDD (V)			
Frequency (MHz)	2.7	3.0	3.3	3.6
10.0	686	1242	1107	2241
12.5	431	756	1071	1147
15.0	308	505	590	825
16.2	283	352	572	638
20.0	217	272	304	513
32.4	154	139	180	142
75.0	151	170	158	109

Plugging variables A, B, C, and D to the RSKM budget, Figure 4:

$\frac{A}{2}$ = 65ps

$\frac{B}{2}$ = 21.32ps

$\frac{C}{2}$ = 1720ps to 2770ns

$\frac{D}{2}$ = 120.87ps

RSKM (LeftSide) @ 1512.81ps

RSKM (RightSide) @ 2737.11ps

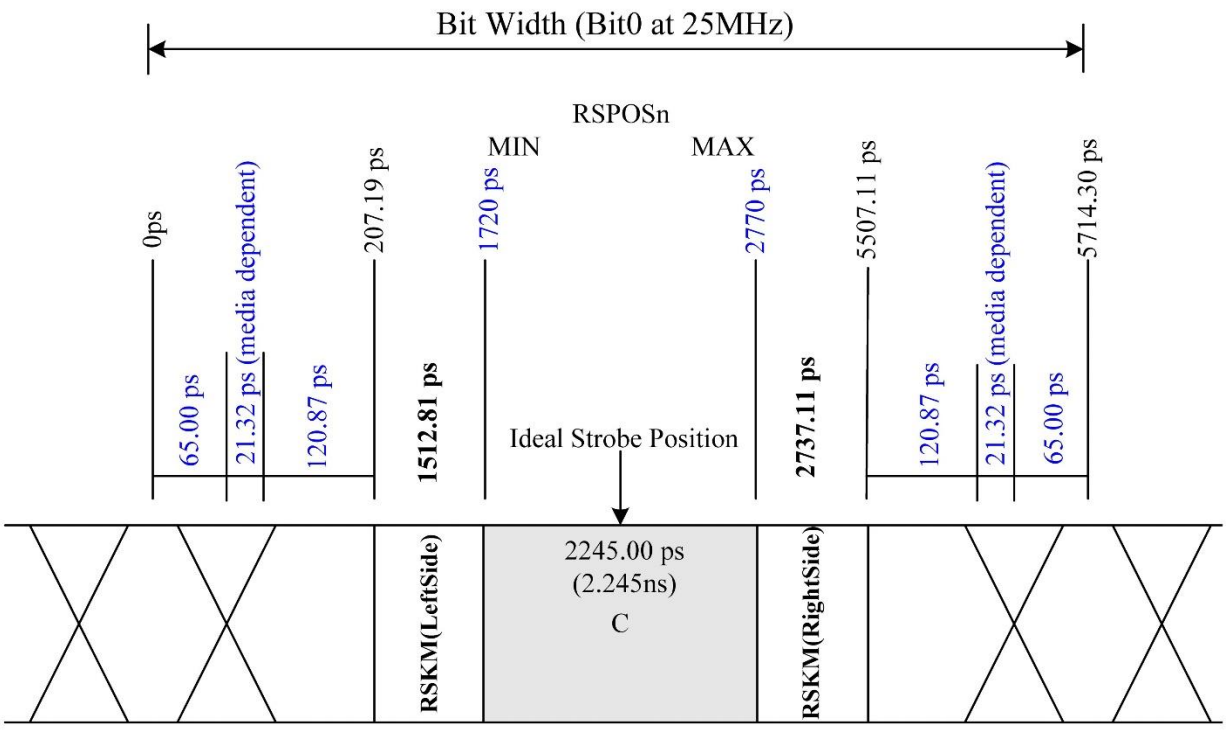

Figure 4. EXAMPLE Bit0 RSKM calculation diagram

4.0 Summary

Estimating for TPPosN and RSPosN for various clock frequencies aids the system designer in calculating the skew budget for the 217/218 system, as well as cable selection. Using data presented in AN-LVDS-011, UT54LVDS217 jitter data, and interconnect media factors, RSKM can be estimated. Estimating the receiver skew margin available in a system helps ensure proper functionality of a LVDS link between the UT54LVDS217 Serializer and UT54LVDS218 Deserializer.

Revision History

Date	Revision #	Author	Change Description	Page #