FRONTGRADE

APPLICATION NOTE

1Gb/64Mb NOR Flash

Interfacing to GR716

12/1/2021

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type
1 Gb SPI NOR Flash	UT81NFR1G1	5962-21210	All
1 Gb Parallel NOR Flash	UT81NFR128M8	5962-21209	All
64 Mb SPI NOR Flash	UT81NFR64M1	5962-21210	All
64 Mb Parallel NOR Flash	UT81NFR8M8	5962-21209	All

Overview

This Design Note provides the user with top-level information for interfacing the Frontgrade NOR Flash with the Frontgrade GR716 interfaces. This document focuses on the interface for booting the GR716 from the NOR Flash.

Design Implementation (Parallel)

The UT81NFR128M8 and UT81NFR8M8 devices both have a single voltage supply that can operate at either 3.3 or 2.5 Volts. The GR716 I/O supply voltage recommended operating conditions require the use of 3.3 Volts. Per the GR716 datasheet in Section 21.3, the interface is configured for 8-bit only.

2.1 Interface Pin List

GR716 Signal Name	GR716 Pin Name	NOR Flash Pin Name	Functional Description
MEM_ADDR[22:0]	GPIO[52:49,18:0]	A[21:0],A-1	Address inputs (DQ[15] is A-1 in x8 mode
MEM_OEN	GPIO[33]	OE#	Output enable
MEM_WRN	GPIO[34]	WE#	Write enable
MEM_CSN0	GPIO[35]	CE#	Chip enable
MEM_DATA[7:0]	GPIO[32:25]	DQ[7:0]	Data input/output
--	--	BYTE#	X16/x8 mode control
--	--	RESET#	Reset
--	--	RY/BY#	Device ready indicator
--	--	WP#	Write protect
--	--	PwrDN#	Power down (1Gb only)

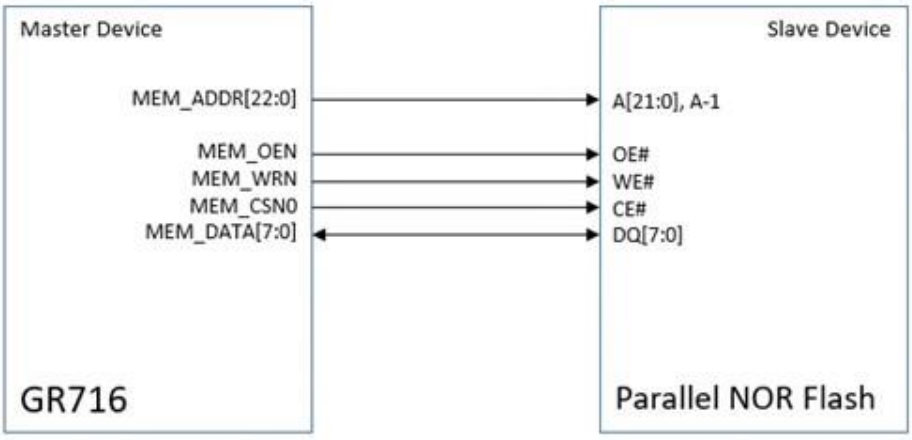

Figure 3: Basic Parallel NOR Flash to GR716 Connections

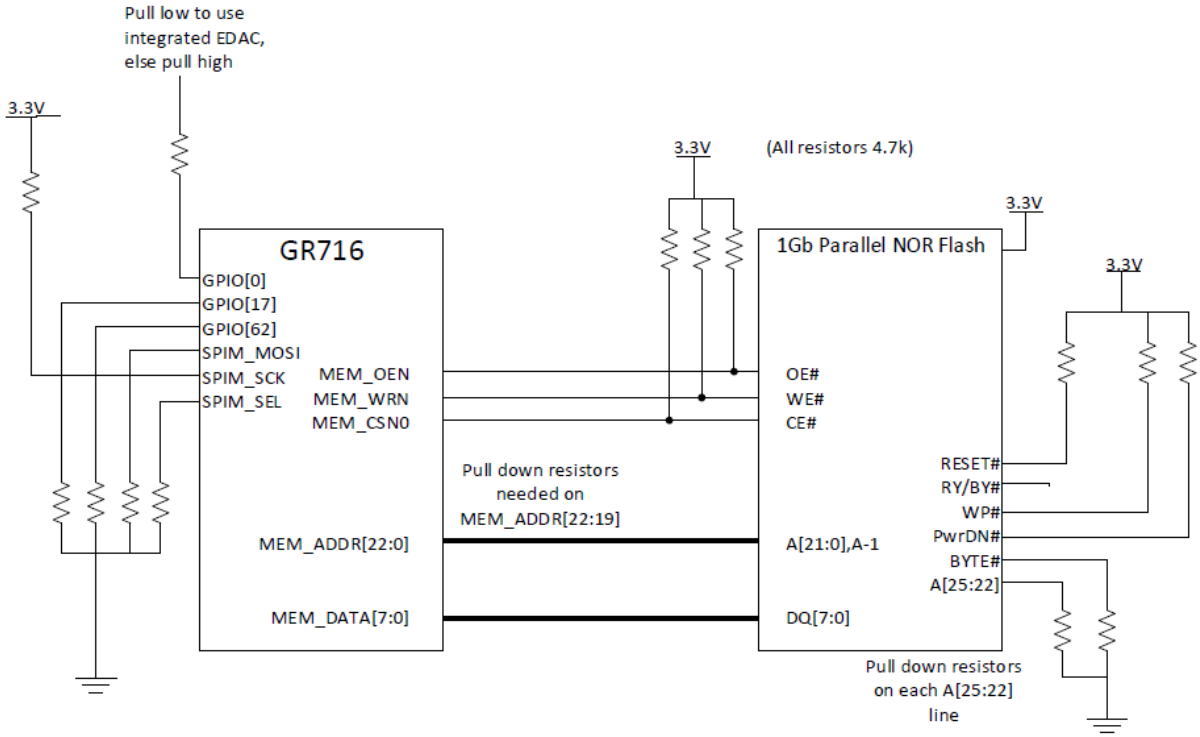

Figure 4: 8-bit PROM (boot) Mode Example

2.2 Setup

The configuration register at AMBA addresses 0x8000D000 through 0x000D01C sets up the GPIOs to interface to the parallel NOR flash. See Sections 7.1 and Table 2.6 in the GR716 datasheet for all the details. The below addresses and data values will configure the GR716 in PROM mode and allow for some available GPIO pins for use.

AMBA address	Acronym	Data
0x8000D000	SYS.CFG.GP0	0x22222222
0x8000D004	SYS.CFG.GP1	0x22222222
0x8000D008	SYS.CFG.GP2	0x00000222
0x8000D00C	SYS.CFG.GP3	0x22222220
0x8000D010	SYS.CFG.GP4	0x00002222
0x8000D014	SYS.CFG.GP5	0x00000000
0x8000D018	SYS.CFG.GP6	0x00022220
0x8000D01C	SYS.CFG.GP7	0x00000000

Note:

Register 0x8000D018 is the only location that software needs to write. The other registers are initialized to the values given in this table at reset, provided the bootstraps select boot from external [parallel] ROM.

In this configuration, GPIO37 thru GPIO40 is available for use to control the NOR flash, if needed.

The GR716 only supports 23 address lines of which only 19 are for boot up. Therefore, the NOR Flash parts are limited in array size for GR716 initialization. More of the array can be accessed using additional GPIO pins after the boot up has been completed. EDAC is supported by the GR716. If enabled, ECC symbols will be stored in the upper fifth of the memory. This will limit the amount of logical memory available to the user to 80% of the physically installed memory. For more information on EDAC, please refer to the follow in app note: https://www.gaisler.com/doc/antn/GRLIB-AN-0003.pdf.

2.3 Bootstrapping

The following pins are a part of the parallel interface and used as bootstrapping signals.

- GPIO[0]=MEM_ADDR[0]
  - — Determines the use of EDAC for external boot RAM when the GR716 microcontroller shall boot from external memory. Set to low for enabling EDAC and to high for disabling EDAC.
- GPIO[17]=MEM_ADDR[17]
  - — High to boot from external ROM
- GPIO[62]=ROM_CSN0
  - — Enable test of internal memories at startup. The processor starts checking internal memory for bit errors during boot if this bootstrap is set to 'high'. Setting this to 'high' will slow down the boot processes since the check is software based.
- GPIO[63]=ROM_CSN1
  - — Enables extra protection of external boot source or setting SpaceWire clock frequency. If boot from external RAM/ROM this pin enables the use of redundant memory if primary boot memory fails.

- DUART_TXD
  - If boot from external SRAM/ROM/SPI-ROM, this pin is used for selecting to copy ASW image from selected external boot RAM/ROM (If not set for this option, the GR716 microcontroller will start execute from the selected external memory)
- SPIM_MOSI
  - Enable remote access. When remote access is disabled, processor will start from selected external boot memory.
- SPIM_SCK, SPIM_SEL
  - When boot from external source is selected (SPIM_MOSI is low)
    - "00" - Boot from SPI Memory
    - "01" - Boot from external SRAM
    - "10" - Boot from external ROM

See figure 4 for recommendations on tying these bootstrapping signals.

Design Implementation (SPI)

3.1 Interface Pin List

GR716 Signal Name	NOR Flash Pin Name	Functional Description
SPIM_MOSI	MOSI	NOR SPI Input
SPIM_MISO	MISO	NOR SPI Output
SPIM_SEL	SS#	Slave Select
SPIM_SCK	SCLK	Serial Clock
--	WP#	Write Protect
--	RESET#	Reset
--	PwrDN#	Part Power down

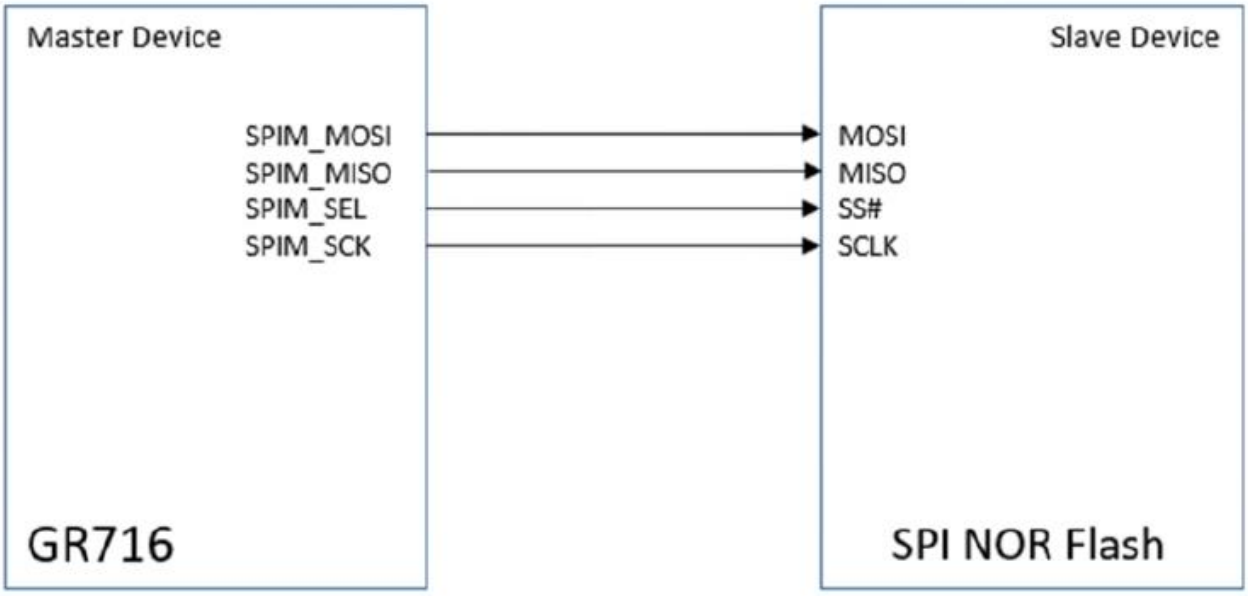

Figure 5: Basic SPI NOR Flash to GR716 Connections

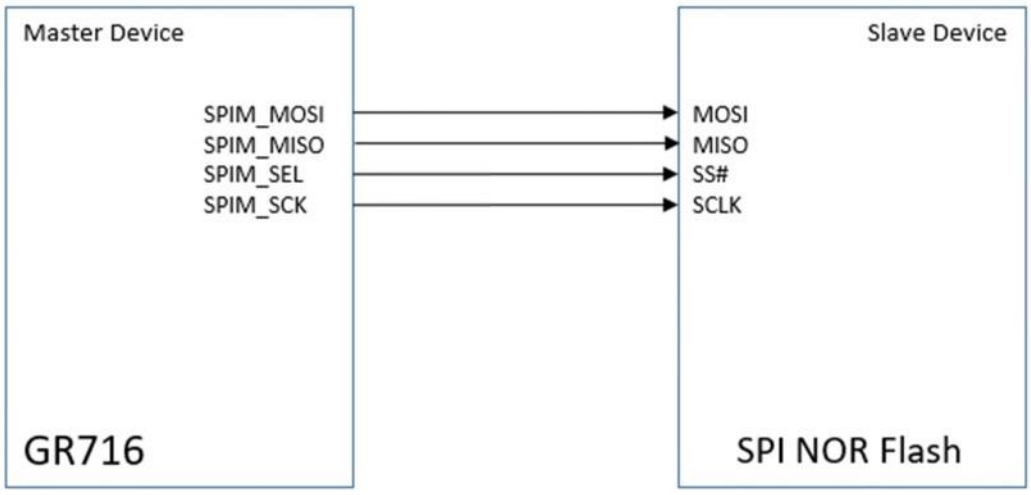

Figure 6: Master SPI (boot) interface Example

3.2 Setup

To setup the GPIOs to interface to the parallel NOR flash, the configuration register is located at AMBA addresses 0x8000D000 through 0x000D01C. See Sections 7.1 and Table 2.6 in the GR716 datasheet for all the details. The current revision of the GR716 only supports 3 address bytes for SPI flashes during boot up. This limits the maximum useable size during boot to 128 Mb. It is however possible for software in the GR716 to operate SPI flashes connected to SPIM pins in a user mode after boot completes. In this case the full 128MiB/1Gb is accessible.

EDAC is supported by the GR716. If enabled, ECC symbols will be stored in the upper fifth of the memory. This will limit the amount of logical memory available to the user to 80% of the physically installed memory. For more information on EDAC, please refer to the follow in app note: https://www.gaisler.com/doc/antn/GRLIB-AN0003.pdf.

3.3 Bootstrapping

Section 2.3 bootstrapping information is applicable to SPI. Figure 6 also covers the important bootstrapping signals

Revision History

Date	Revision #	Author	Change Description	Page #
12/2021			Initial release	