FRONTGRADE

APPLICATION NOTE

AN-LVDS-010-01

LVDS Receiver Input Thresholds

6/2/2011

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
3.3-Volt Quad Receiver	UT54LVDS032LV/E	5962-98652	02, 03, 04, 05	WD04, WD08, WD29, WD31
3.3-Volt Quad Receiver with Termination Resistor	UT54LVDS032LVT	5962-04201	01, 02	WD06, WD10
3.3V Dual Driver and Receiver	UT54LVDM055LV	5962-06202	01	WD22
5.0V Quad Receiver	UT54LVDS032	5962-95834	02	JR06. JR09
5.0V Quad Receiver with Cold Spare	UT54LVDSC032	5962-95834	03	JR11
3.0V Quad Bus LVDS Crosspoint Switch	UT54LVDM228	5962-01537	01	WD15,WD16
3.0V Octal Bus LVDS Repeater	UT54LVDM328	5962-01536	01	WD17, WD18
3.0V Deserializer with Cold Spare	UT54LVDS218	5962-01535	01, 02	WD12, WD14

Overview

Low Voltage Differential Signaling (LVDS) is a method used to transmit and receive hundreds of megabits per second over differential media using a low voltage signal swing (~350mV). LVDS communications are preformed by a driver and a receiver. The LVDS receiver, see Figure 1, senses a differential voltage across the termination resistor (RT) located across the receiver input terminals (RIN+/RIN-) and outputs a standard CMOS signal (ROUT). LVDS receivers generate their output state based on the direction the current is flowing across the termination resistor.

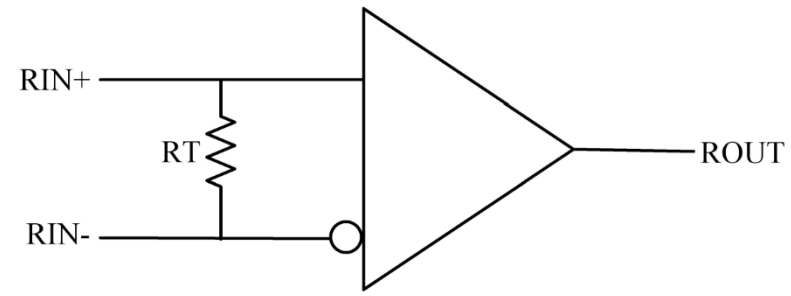

Figure 1. Notional LVDS Receiver diagram

Figure 2 shows the current flow through the driver/receiver system during a logic LOW state. The current flows through the termination resistor from negative to positive receiver terminals, a forward voltage drop occurs and a logical LOW appears at the output (ROUT) of the receiver. Figure 3 shows the current flow through the driver/receiver system during a logic HIGH state. Similarly, the current flows through the termination resistor from positive to negative receiver terminals, a reverse voltage drop occurs and a logical HIGH appears on the receiver output.

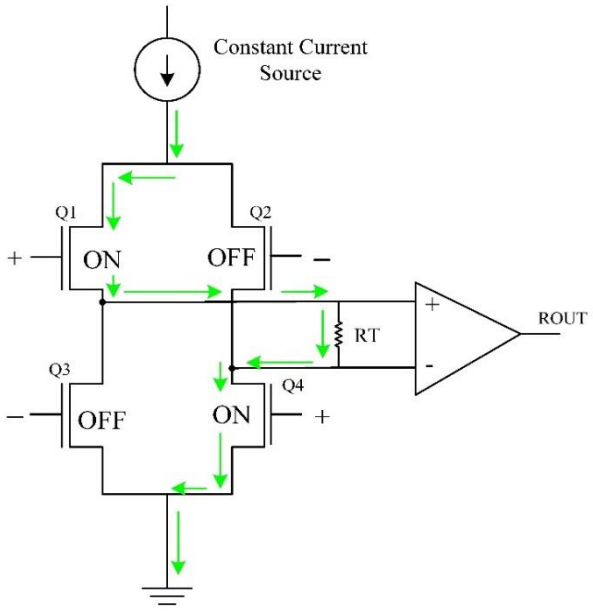

Figure 2. Logic Low (zero, 0) State

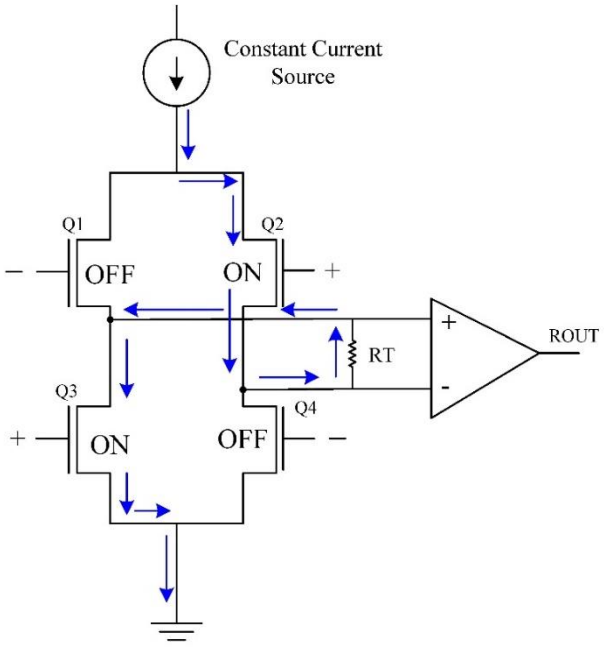

Figure 3. Logic High (one, 1) State

LVDS/LVDM Receiver Specifications

Low Voltage Differential Signaling input/output signal levels for LVDS are defined by the Telecommunications Industry Association/ Electronic Industries Association ANSI/TIA/EIA-644. ANSI/TIA/EIA-644 is an electrical standard only and does not define a protocol. Frontgrade LVDS Drivers and Receivers are compliant with this specification.

The differential input high threshold voltage, VTH, describes the minimum positive differential voltage on the receiver inputs that results in a logic HIGH state on the receiver output (ROUT). VTL, the differential input low threshold, describes the maximum negative differential voltage on the receiver inputs that results in a logic LOW on ROUT. Figure 4 details VTH and VTL limits with respect to ground and the maximum recommended input voltage on the receiver input pins.

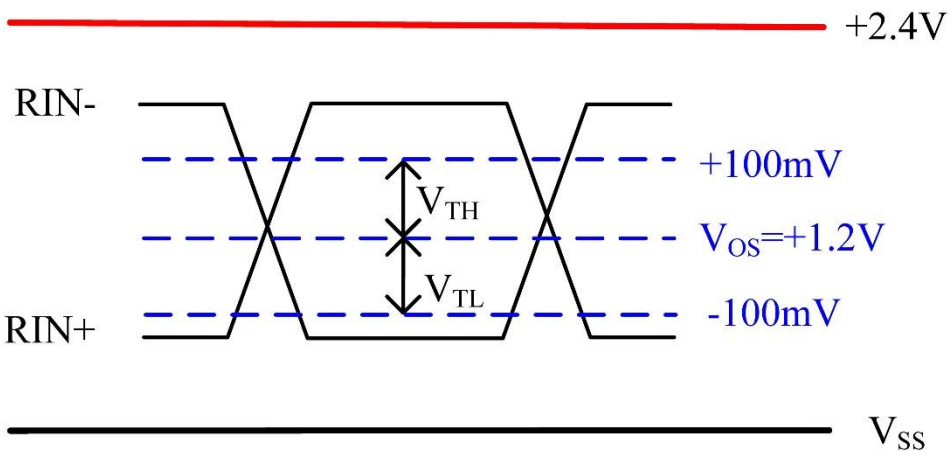

Figure 4. VTH and VTL diagram.

LVDS receiver differential input threshold levels are guaranteed to be +/-100mV; characterization of the devices has shown voltages within these limits and can cause the receiver output to switch state. The differential input threshold sensitivities are maintained over a wide common mode from 0V to 2.4V. LVDS also features a +/-1 V common-mode range around the driver offset voltage (+1.2V typical) which aids in the rejection of system noise that is coupled between the differential pairs.

During characterization of the receivers, Frontgrade Colorado Springs has seen the MIN voltage for VTH be ~40mV, and VTL MAX be ~60mV. Results of characterization data are listed in Table 2; this data is not guaranteed.

Table 2. Typical Receiver Differential Input Threshold Data

VTH (mV)		VTL (mV)	
MIN	MAX	MIN	MAX
+40	+100	-60	-100

Summary

LVDS receivers are designed to reject common-mode noise. Some customers have expressed concern regarding noise immunity of the LVDS receivers due to the low voltage, +/-350mV, swing along with the +/-100mV differential receiver input thresholds. The system designer should follow good design practices and be sure the differential signals run close together through controlled impedance traces or cables. Frontgrade Colorado Springs designs LVDS receivers to ignore common mode noise that is equally coupled on the differential signals and switch only when there is a difference between the differential input signals.

Revision History

Date	Revision #	Author	Change Description	Page #