



FRONTGRADE

ADV DATASHEET

UT8MNQ32GBeMMC51

32GB eMMC Managed NAND

6/17/2025

Version #: 0.0.1

1.0 Features

- 32 GByte Density
- eMMC 5.1 interface
- HS200 and HS400 support
- 300MB/s max read sequential
- 150MB/s max write sequential
- Retention: 10 years @ 55°C beginning of life, 1 year @ 55°C cycled life
- 40 TBytes Written (TBW) endurance
- NAND functions (ECC, wear leveling, block management, etc) handled by on board controller
- MSL 3
- 153-pin FBGA Package
 - 13mm x 11.5mm
 - 0.5mm pitch
- 3.3 V VDD
- 1.8V, 3.3V VDDQ
- Power: 330 mA peak current @3.3V/1.8V

Operational Environment

- Target Temperature Range: -25°C to +85°C
- Target TID: 30-50 krad(Si)
- SEL threshold: <60 MeV-cm2/mg

Applications

- Solid State Drive
- Microcontroller/Microprocessor/FPGA image storage

NOTE: This is a commercial part, upscreened for space use, and is assembled in China. Final PEM environmental and electrical testing is performed in the USA.

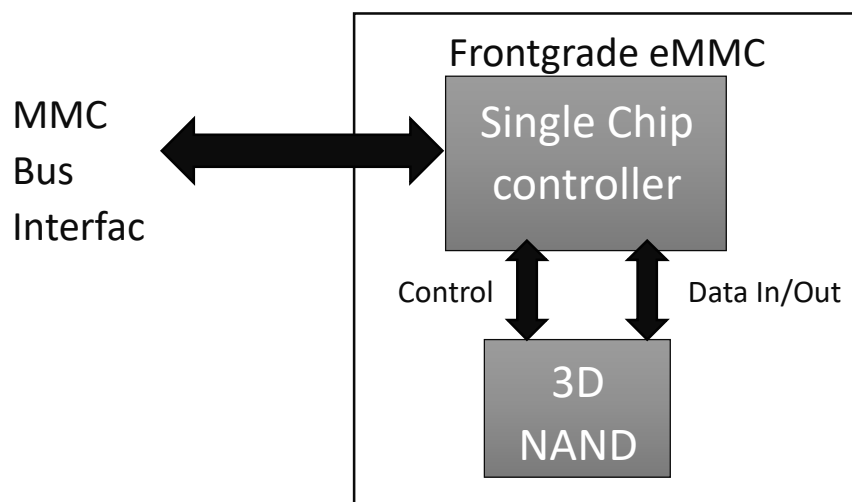


Figure 1: 32GB eMMC Block Diagram

2.0 Introduction

The 32GB eMMC Managed NAND is a high-performance, reliable storage solution for Low Earth Orbit (LEO) space applications. With built-in advanced error correction and wear leveling, this eMMC device ensures data integrity and extended lifespan, making it ideal for embedded space systems. Offering a seamless balance between performance and efficiency, it delivers fast read and write speeds to meet the demands of modern space applications. Its compact form factor and ease of integration make it a go-to choice for designers seeking a cost-effective, durable, and high-capacity NAND storage solution.

The 32GB eMMC is OEM assembled and tested in China. Screening and Qualification called out in Section 8 (PN build up) is performed in the USA, including electrical verification.

3.0 General Description

The eMMC is a managed memory capable of storing code and data. It offers the performance and features required for space application while maintaining low power consumption. The device includes features that support high throughput for large data transfers and performance for small random data more commonly found in code usage. It also contains many security features as well as eMMC communication which is based on an advanced 11-signal bus. The communication protocol is defined as a part of JESD84-B51.

3.1 Features Overview

Table 1: Supported Feature List

Device Features	Support
Interface	HS400
Bus Speed	Up to 300MB/s
Secure Erase/Trim	Yes
Boot and Mass Storage	Yes
Partitioning & Protection	Yes
Background Operations	Yes
Power Off Notification	Yes
Hardware Reset	Yes
HPI	Yes
RPMB	Yes
Extended Partition Attribute	Yes
Large Sector Size	No
Sanitize	Yes
Packed Commands	Yes
Discard	Yes
Cache	Yes
Production State Awareness	Yes
Device Health	Yes
Enhance Strobe	Yes
Command Queue	Yes

Device Features	Support
RPMB Throughput	Yes
Cache Flush and Barrier	Yes
BKOPS Controller	Yes
Secure Write Protect	Yes
HS400 Tuning	Yes

Table 2: Power Supply Voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ(Low)	1.7	1.95	V
	VCCQ(High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

Note: HS200, HS400 modes support only the 1.7-1.95 V VCCQ option.

Table 3: Bus Operating Conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	μA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	μA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	μA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	μA

3.2 Cache

The UT8MNQ32GBeMMC51 has an onboard cache that improves performance for both sequential and random access. For additional information, refer to JESD84-B51.

3.3 Discard

The Discard function allows the host to identify data that is no longer needed, allowing the device to erase the data if necessary during background erase events. Once applied, the contents of the affected write block where the discard function has been applied shall be ‘don’t care’. Depending on the device, some or all of the original data may remain accessible to the host, while portions that are no longer accessible may be removed or unmapped. The device ultimately determines the final state of the discarded write block. See JESD84-B51 for more information.

3.4 Error Management

The UT8MNQ32GBeMMC51 features a defect and error management system designed to ensure high data reliability. When a defective memory block is detected, the system automatically transfers the data to a functional block, maintaining integrity without requiring user intervention. This process, while transparent to the host, also preserves available storage space. If a read error occurs during data migration, built-in recovery algorithms work to retrieve and restore the affected data.

3.5 Power Off Notifications

The UT8MNQ32GBeMMC51 supports power-off notifications per JESD84-B51, enabling the device to better prepare itself for shutdown more effectively. Turning off the device means turning off all its power supplies, allowing it to properly shutdown and preserve critical data. This ensures faster boot times on the next power cycle. See JESD84-B51 for more information.

3.6 Packed Commands

The UT8MNQ32GBeMMC51 supports packed commands per JESD84-B51. This feature allows multiple read and write commands to be grouped together (either all read or all write), enabling the device to transfer all of the associated data in a single bus transaction. By reducing command overhead, packed commands enhance efficiency and optimize data transfer performance. See JESD84-B51 for more information.

3.7 Boot Partition

The UT8MNQ32GBeMMC51 supports boot partitions per JESD84-B51. There are two boot partitions, each with 4MB capacity. See JESD84-B51 for more information.

3.8 Replay Protected Memory Block (RPMB) Partition

The UT8MNQ32GBeMMC51 supports RPMB operation mode per JESD84-B51. One RPMB partition is available in a size of 16MB. See JESD84-B51 for more information.

3.9 Automatic Sleep Mode

Upon completing an operation, the device automatically enters sleep mode to conserve power when no further commands are received. The host does not need to intervene for this process to occur. However, to obtain the lowest possible sleep current, the host must disable the clock to the memory device. When the host is ready to access the device again, sending any command will wake it from sleep mode and prompt a response.

3.10 Sleep (CMD5)

The UT8MNQ32GBeMMC51 can transition between Sleep and Standby states using the SLEEP/AWAKE command (CMD5). In Sleep mode, the device power consumption is minimized and only responds to RESET (CMD0 with argument of 0x00000000, 0xF0F0F0F0 or H/W reset) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. Additionally, during the Sleep mode, the VCC power supply can be turned off. See JESD84-B51 for more information.

3.11 Enhanced Reliable Write

Enhanced Reliable Write enhances data integrity by ensuring stored data is more resilient and less susceptible to corruption. It ensures atomicity, meaning a write operation is either completed successfully, or it is not written at all. See JESD84-B51 for more information.

3.12 Sanitize

To execute a Sanitize operation, the device must physically clear data from the unmapped user address space. This process begins when a specific value is written to the extended CSD[165] SANITIZE_START. During the sanitize operation, the busy line remains asserted indicating active data removal. See JESD84-B51 for more information.

3.13 Secure Erase

In addition to the standard Erase command, there is also a Secure Erase command. Unlike the basic Erase command, Secure Erase ensures that the memory array is actively cleared when the command is issued. Additionally, both the device and host must remain idle until the operation is completed before moving to the next device operation. See JESD84-B51 for more information.

3.14 Secure Trim

NOTE: Secure TRIM is included for backward compatibility. For newer system level implementations (based on v4.51 devices and beyond), it is recommended to use TRIM in combination with Sanitize instead of Secure TRIM.

The Secure Trim command functions similarly to the Secure Erase command but applies to write blocks rather than erase groups. To reduce the impact on device performance and reliability, the Secure Trim operation is carried out in two distinct steps, ensuring efficient data removal while maintaining system integrity. See JESD84-B51 for more information.

3.15 Partition Management

This part offers the host the ability to configure additional split local memory partitions with independent addressable space, starting from logical address 0x00000000 for different usages. The memory block areas are categorized as follows:

- Factory configuration includes two boot partitions (See 3.7), which function as enhanced storage media, and one RPMB partition of 16MB (See 3.8).
- Up to four General Purpose Area Partitions can be configured for various uses, such as storing user data, sensitive data, or other host-defined uses. Partition sizes are determined as multiples of the write protect group and can only be programmed once during the device's life cycle (one-time programmable).

3.16 Device Health

Device Health provides device program/erase cycle information as a percentage of the device life span. The host can query this information using standard MMC command to retrieve the extended CSD structure:

- DEVICE_LIFE_TIME_EST_TYP_B[268]: SLC device health information
- DEVICE_LIFE_TIME_EST_TYP_B[269]: TLC device health information

The device health will be provided as a percentage of the wear of the part in 10% increments.

3.17 EOL Status

EOL status is implemented in accordance with the eMMC 5.1 specification.

3.18 Enhanced Write Protection

The part supports two levels of write-protection to protect against erase or write.

- By setting the permanent or temporary write protect bits in the CSD, the entire device, to include the Boot Area Partitions, General Purpose Area Partitions, and User Area Partition may be write-protected.
- Specific part segments may be write-protected, either permanently, power-on, or temporarily. The segment size may be programmed per the EXT_CSD register.

See JESD84-B51 for more information.

3.19 High Priority Interrupt (HPI)

In certain scenarios, different types of data within the device may carry varying levels of priorities for the host. For instance, writing operations may be time consuming and it therefore may be necessary to pause writing to accommodate demand paging requests, ensuring that a process launches promptly upon user request.

The High Priority Interrupt (HPI) mechanism allows the device to interrupt a lower priority operation before completion, within the OUT_OF_INTERRUPT_TIME timeout. If an operation is interrupted, the host may need to repeat the affected process or portions of it to complete the original request.

See JESD84-B51 for more information.

3.20 Hardware Reset

Hardware reset of a device may be accomplished by moving the device to Pre-idle state and disabling power-on period write protect on blocks set as power-on write protect before reset was asserted.

See JESD84-B51 for more information.

3.21 Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature enables STROBE to synchronize the CMD response, improving data exchange efficiency between the host and the device:

- CMD clocking remains SDR, maintaining Single Data Rate operation;
- Host commands are transmitted on the rising edge of the host clock, consistent with legacy eMMC devices;
- The device provides STROBE signaling, aligned with both the CMD response and DATA Out;
- The host can utilize STROBE signaling for DAT and CMD Response capturing, eliminating the need for a tuning mechanism.

To take advantage of this feature, host support is required, ensuring faster and more reliable operation.

3.22 Command-Queue

To facilitate command queuing in eMMC, the device manages an internal task queue the host can queue data transfer tasks.

See JESD84-B51 for more information.

3.23 Frequent Used Commands in CmdQ

In Command Queue mode, the device allows the host to issue the FLUSH, BARRIER, and DISCARD commands even when the queue is not empty. Utilizing these commands can enhance performance, optimizing the efficiency of the device's operation within this mode.

3.24 HS400 Tuning

The Host can utilize adjustable sampling to determine the optimal sampling point. Additionally, a predefined tuning block stored within the Device can assist the host in identifying the optimal data sampling point. To access and read the tuning block, the host may use the CMD21 tuning command.

See JESD84-B51 for more information.

4.0 Part Information

4.1 Pin List

Table 4: Operating Conditions

Signal	Ball Assignment	Type	Description
DAT0	A3	I/O	Data I/O: Bi-directional channel used for data transfer
DAT1	A4		
DAT2	A5		
DAT3	B2		
DAT4	B3		
DAT5	B4		
DAT6	B5		
DAT7	B6		
CMD	M5	I/O	Command: Bi-directional channel used for device initialization and command transfers
QRDY	E5	Output	An optional pin, disabled by default and can be left NC.
CLK	M6	Input	Clock: each cycle directs a 1-bit transfer on the command and DAT lines.
RST_n	K5	Input	Hardware Reset
RCLK	H5	Output	Data Strobe
VCC	E6, F5, J10, K9	Supply	Memory Power Supply
VCCQ	C6, M4, N4, P3, P5	Supply	Memory I/O Power Supply
VSS	E7, G5, H10, K8, A6, J5	Supply	Memory Power Ground
VSSQ	C4, N2, N5, P4, P6	Supply	Memory I/O Power Ground
VDDi	C2		Internal power node, A 0.1 μ F capacitor must be connected from VDDi to GND (Ground)
DNU	E9, E10, F10, K10, E8, G10, P10		Leave floating
N/C			Not Connected and can be connected to GND

4.2 Package Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	VSS	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDi	NC	VssQ	NC	VccQ	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC								NC	NC	NC
E	NC	NC	NC		NC	VCC	VSS	DNU	DNU	DNU		NC	NC	NC
F	NC	NC	NC		VCC					DNU		NC	NC	NC
G	NC	NC	NC		VSS					DNU		NC	NC	NC
H	NC	NC	NC		RCLK					VSS		NC	NC	NC
J	NC	NC	NC		VSS					VCC		NC	NC	NC
K	NC	NC	NC		RESET	NC	NC	VSS	VCC	DNU		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	VccQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	VssQ	NC	VccQ	VssQ	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	VccQ	VssQ	VccQ	VssQ	NC	NC	NC	DNU	NC	NC	NC	NC

Figure 2: 153 BGA Package Pinout (Top View)

5.0 Electrical Specifications

5.1 Absolute Maximum Information

Table 5: Max Conditions

Parameter	Min	Max	Unit
VCCQ (Low)	TBD		V
VCCQ (High)	TBD		V
VCC	TBD		

5.2 Recommended Operating Conditions

Table 6: Operating Conditions

Parameter	Min	Max	Unit
Operating Temperature Range ¹	-25	85	°C
Non-operating Temperature Range	-40	85	°C
VCCQ (Low)	1.7	1.95	V
VCCQ (High)	2.7	3.6	V
VCC	2.7	3.6	

Note:

1. Temperature is Tcase

5.3 Endurance and Data Retention

Table 7: Reliability Data

Parameter	Description	Value
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events, data can be lost.	1 sector in 10 ¹⁵ bits read
Write Endurance	Commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload written at certain operated temperature range. Representative workload description: • 80% Sequential write, 20% Random Write • Distribution of IO Transaction Sizes: - o <16KB: 82% - o 16KB-128KB: 17% - o >128KB: 1% • Cache On, Packed Off. • Host data is 4K aligned. • 30% of product lifetime operate @85°C T-case. • 70% of product lifetime operate @55°C T-case.	40 TBW

Parameter	Description	Value
Data Retention	Fresh or Early Life Device ¹	10 years @25°C & 55°C
	Cycled Device ²	1 year @25°C & 55°C ³

Notes:

1. A device whose total write cycles to the flash is <10% of the maximum endurance specification
2. Any device whose total write cycles are between 10% and the maximum endurance specification
3. In the case where the number of writes exceed the endurance spec, Read and Write performance can be intermediately reduced.

5.4 Operational Environment

5.4.1 DC Electricals

Table 8: DC Electricals

Ta=25°C@3.3V/1.8V

Parameter	Symbol	Test conditions	Min	Max	Unit
HS400 Sleep	Isb1	CMD5; VCCQ,VCC off		150	μA
HS200 Sleep	Isb2	CMD5; VCCQ,VCC off		150	μA
Active HS400	Icc1	Peak [2μs window]		170	mA
	Icc2	Max [1ms window]		330	mA
Active HS200	Icc3	Peak [2μs window]		170	mA
	Icc4	Max [1ms window]		330	mA
HS400	Iread1	RMS [100ms window] VCC		70	mA
	Iwrite1			50	mA
	Iread2	RMS [100ms window]		235	mA
	Iwrite2			150	mA
HS200	Iread3	RMS [100ms window] VCC		70	mA
	Iwrite3			50	mA
	Iread4	RMS [100ms window]		235	mA
	Iwrite4			150	mA

5.4.2 AC Electricals

Table 9: System Performance

Parameter	Condition	Typical	Unit
Write (Sequential)	HS400	150	MB/s
Read (Sequential)	HS400	300	MB/s
Write (Sequential)	HS200	145	MB/s
Read (Sequential)	HS200	170	MB/s
Write (Random)	HS400	15K	IOPS
Read (Random)	HS400	20K	IOPS
Write (Random)	HS200	14K	IOPS
Read (Random)	HS200	20K	IOPS

Note:

- Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bits at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB
- Random performance is measured with a chunk size of 4KB and address range of 1GB.
- Write performance is measured for 100MB host payloads

6.0 Register and Feature Overview

6.1 Register Values

Table 10: DSR Register

Parameter	CSD Slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

Table 11: CID Register

Parameter	DSR Slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Device BGA	01h	2
OID	[111:104]	Application ID	00h	8
PNM	[103:56]	Product name	32GB-DA4032	48
PRV	[55:48]	Product revision	01h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	Month, year	8
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Note: Refer to the definition of the MDT field as defined in eMMC Specification version 5.0.

Table 12: OCR Register

Parameter	DSR Slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7-3.6 range	1FFh	9
	[14:8]	VDD: 2.0-2.6 range	00h	7
	[7]	VDD: 1.7-1.95 range	1h	1

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

Table 13: CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	3h	3
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	8F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial block for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
*C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16:16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15:15]	File format group	0h	1
COPY	[14:14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Table 14: EXT_CSD Register

Parameter	ECSD Slice	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context Management Capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit Size	0h
EXT_SUPPORT	[494]	Extended Partitions Attribute Support	3h
SUPPORTED_MODES	[493]	FFU Supported Modes	3h
FFU_FEATURES	[492]	FFU Features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation Codes Timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
BARRIER_SUPPORT	[486]	Cache Barrier Support	1h
CMDQ_SUPPORT	[308]	Command Queue Support	1h
CMDQ_DEPTH	[307]	Command Queue Depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
HEALTH_REPORT	[301:270]	Health Report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation Type B (TLC)	1h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation Type A (SLC)	1h
PRE_EOL_INFO	[267]	Pre EOL Information	1h
OPTIMAL_READ_SIZE	[266]	Optimal Read Size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal Write Size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal Trim Unit Size	8h
DEVICE_VERSION	[263:262]	Device Version	5051h
FIRMWARE_VERSION	[261:254]	Firmware Version	FW Version
PWR_CL_DDR_200_360	[253]	Power Class for 200MHz, DDR at VCC=3.6V	0h
CACHE_SIZE	[252:249]	Cache size	1000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power Off Notification (Long) Timeout	19h
BKOPS_STATUS	[246]	Background Operations Status	Default=0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of Correctly Programmed Sectors	Default=0h
INI_TIMEOUT_AP	[241]	1 st Initialization Time After Partitioning	FFh
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power Class for 52MHz, DDR at VCC=3.6V	0h
PWR_CL_DDR_52_195	[238]	Power Class for 52MHz, DDR at VCC=1.95V	0h
PWR_CL_200_195	[237]	Power Class for 200MHz, DDR at	0h

Parameter	ECSD Slice	Description	Value
		VCCQ=1.95V, VCC=3.6V	
PWR_CL_200_130	[236]	Power Class for 200MHz, DDR at VCCQ=1.3V, VCC=3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM_MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature Support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot Partition Size	20h
ACCESS_SIZE	[225]	Access Size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase Unit Size	1h (see Table 16)
ERASE_TIMEOUT_MULT	[223]	High Capacity Erase Time Out	3h
REL_WR_SEC_C	[222]	Reliable Write Sector Count	1h
HC_WP_GRP_SIZE	[221]	High Capacity Write Protect Group Size	10h (see Table 16)
S_C_VCC	[220]	Sleep Current [VCC]	7h
S_C_VCCQ	[219]	Sleep Current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production State Awareness Timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake Timeout	13h
SLEEP_NOTIFICATION_TIME	[216]	Sleep Notification Timeout	17h
SEC_COUNT	[215:212]	Sector Count	See Table 15
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition Switching Timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt Busy Timing	19h

Parameter	ECSD Slice	Description	Value
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh (reporting four strengths, but supporting only one)
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default=0h Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	Dh
HS_TIMING	[185]	High Speed Interface Timing	Default=0h Updated in runtime by the host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default=0h Updated in runtime by the host
ERASE_MEM_CONT	[181]	Content of Explicit Erased Memory Range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default=0h
BOOT_CONFIG_PROT	[178]	Boot Config Protection	Default=0h Updated in runtime by the host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default=0h Updated in runtime by the host
ERASE_GROUP_DEF	[175]	High-Density Erase Group Definition	Default=0h Updated in runtime by the host
BOOT_WP_STATUS	[174]	Boot Write Protection Status Registers	Default=0h Updated in runtime
BOOT_WP	[173]	Boot Area Write Protect Register	0h
USER_WP	[171]	User Area Write Protect Register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	80h
WR_REL_SET	[167]	Write Reliability Setting Register	1Fh
WR_REL_PARAM	[166]	Write Reliability Parameter Register	15h
SANITIZE_START	[165]	Start Sanitize Operation	Default=0h Updated in runtime by the host
BKOPS_START	[164]	Manually Start Background Operations	Default=0h Updated in runtime by the host
BKOPS_EN	[163]	Enable Background Operations Handshake	2h
RST_n_FUNCTION	[162]	H/W Reset Function	Default=0h Updated

Parameter	ECSD Slice	Description	Value
			by the host
HPI_MGMT	[161]	HPI Management	Default=0h Updated by the host
PARTITIONING_SUPPORT	[160]	Partitioning Support	7h (Note: EUDA is not supported)
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	0h
PARTITION_ATTRIBUTE	[156]	Partitions Attribute	Default=0h Updated by the host
PARTITION_SETTING_COMPLETED	[155]	Partitioning Setting	Default=0h Updated by the host
GP_SIZE_MULT	[154:153]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AWARENESS	[133]	Production State Awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	0h
VENDOR_SPECIFIC_FIELD	[124:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native Sector Size	0h
USE_NATIVE_SECTOR	[62]	Sector Size Emulation	0h
DATA_SECTOR_SIZE	[61]	Sector Size	0h
INI_TIMEOUT_EMU	[60]	1 st initialization after disabling sector size emulation	Ah
CLASS_6_CTRL	[59]	Class 6 Commands Control	0h
DYNCAP_NEEDED	[58]	Number addressed group to be released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception Events Control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception Events Status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context Configuration	Default=0h
PACKED_COMMAND_STATUS	[36]	Packed Command Status	Default=0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed Command Failure Index	Default=0h Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default=0h Updated in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the Cache	0h
BARRIER_CTRL	[31]	Cache Barrier	0h

Parameter	ECSD Slice	Description	Value
MODE_CONFIG	[30]	Mode Config	0h
MODE_OPERATION_CODES	[29]	Mode Operation Codes	0h
FFU_STATUS	[26]	FFU Status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre Loading Data Size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max Pre Loading Data Size	See Table 17
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product State Awareness Enablement	3h
AUTO_PRE_SOLDERINGSECURE_REMOVAL_TYPE	[16]	Secure Removal Type	8h
CMDQ_MODE_EN	[15]	Command Queue	0h

Table 15: Write Protect Group Size

Capacity	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
32GB	0x1	0x10	0.5MB	8MB

Table 16: Max Preloading Data Size

Capacity	Max Preloading Image Size (in LBA Hex)	Max Preloading Image in MB
32GB	1,333,4C8	9,840

Table 17: Capacity for User Data

Capacity	LBA [Hex]
32GB	0x3A3E000

6.2 SLCBoost

The SLCBoost feature provides:

- Adaptive part performance adjustments based on application needs;
- Reduced WRITE-BUSY time through improving IO throughput;
- Vertical technology:
 - Host access to NAND flash performance capabilities;
 - Automatic detection by the controller and firmware of host requirements, enabling dynamic device behavior adjustments;
 - Host customizations and modifications in IDLE time management for optimal utilization of SLCBoost capabilities

This feature is implemented using allocated SLC blocks, without altering the device's overall capacity. A detection mechanism identifies sequential performance patterns. Upon recognition, the part defers background management operations (where feasible) and prioritizes SLC programming.

When an IDLE state exceeds tIDLE (ms), migration operations are triggered to free up sufficient space for upcoming bursts, preventing potential performance degradation.

The below table demonstrates the SLCBoost buffer size and performance:

Table 18: SLCBoost Buffer Size and Performance

Capacity	Buffer Size (GB)	Write Speed (MB/s)
32GB	8	150

6.2.1 Emptying the SLCBoost Buffer

There are multiple host-enabled mechanisms available to facilitate the emptying of the SLCBoost buffer (migration). These modes can be enabled, either individually or simultaneously, depending on the selected configuration. The greater the number of modes supported by the host, the more efficiently the buffer can be cleared, ensuring optimal availability for high-speed payload handling.

During migration, device performance remains unaffected, with no impact on latency or system responsiveness. The host has several optional configurations for SLCBoost including:

1. IDLE only mode (PoN=1) (Recommended Option);
2. BKOPs APIs with HPI; and
3. Sleep notification before standby (CMD5).

Table 19: Emptying SLCBoost Buffer

SLCBoost Buffer Migration	EXT_CSD REV [192]	AUTO_EN BKOPS_EN [163][1]	POWER_OFF_NOTIFICATION [34] (PON activated)	BKOPS_EN BKOPS_EN[163][0]	POWER_OFF_NOTIFICATION [34] (Sleep Notification)	Standby mode CMD5
Migration during in system IDLE with HPI	7h (eMMC 5.0)	Don't care	1h (Powered_on)	Don't care	No	If system uses CMD5, a delay of 5-10 sec is required before CMD5 transmission
Migration during in system IDLE with HIP	8h (eMMC 5.1)	1h	1h (Powered_on)	Don't care	No	If system uses CMD5, a delay of 5-10 sec is required before CMD5 transmission
Migration during BKOPs Busy	7h or 8h (eMMC 5.0/5.1)	0h	Don't care	1h	No	Don't care

6.3 Device Report

The part includes a device report feature providing Device Status updates.

- Activating Device Report Mode: Send CMD62 w/argument of 0x96C9D71C. A R1b response will be returned.
- Retrieving the Report: Once the host has entered Device Report mode, sending a CMD63 w/argument 0x00000000 will retrieve the report. The host will receive 512 Bytes.
- Returning to Normal Operations: After executing the Device Report read command (CMD63), the device automatically resumes normal operation.
- Table 20: Device Report

Field Name	Description	Motivation (Host perspective)	Offset (Dc)	Size (Bytes)
Average Erase Cycles Type A (SLC)	The average erase cycles value out of all SLC blocks	To check real life product endurance and lifetime	4	4
Average Erase Cycles Type B (TLC)	The average erase cycles value out of all TLC blocks	To check real life product endurance and lifetime	8	4
Read reclaim count Type A (SLC)	The amount of SLC read operations which passed read-scrub thresholds and requires reclaim	To check device data retention preventions mechanism on SLC area	16	4
Read reclaim count Type B (TLC)	The amount of TLC read operations which passed read-scrub thresholds and requires reclaim	To check device data retention preventions mechanism on TLC area	20	4
Bad Block Manufactory	Number of Bad Blocks detected during manufacturing process	To check device number of bad blocks	24	4
Bad Block Runtime Type A (SLC)	All bad blocks related to the SLC area that were detected during run time	To check device runtime number of bad blocks on SLC area	32	4
Bad Block Runtime Type B (TLC)	All bad blocks related to the TLC area that were detected during run time	To check device runtime number of bad blocks on TLC area	36	4
Field FW updates count	Number of secure field firmware upgrades (sFFU) done from the beginning of the device lifetime	To know that number of times sFFU operations were done on the device.	40	4
FW Release Date	Firmware Release Date	To identify device firmware	44	12
FW Release Time	Firmware Release Hour	To identify device firmware	56	8
Cumulative Host Write data size	Accumulate the amount of host written payload in resolution of 100MB	To analyze host total write payload and typical daily workload	64	4
Number Vcc Voltage Drops Occurrences	Cumulative counter for voltage drops (power-off) during all device states (Idle/Read/Write/Erase).	To identify unstable power supply platform behavior	68	4
Number Vcc Voltage Droops Occurrences	Counts the times VDET indication was triggered due to Power-Droop (slight power droop below certain threshold and for a very short period of time)	To identify unstable power supply platform behavior	72	4
Number of failures recover new host data (After Write Abort)	Count the number of times device dismiss new host data due to write abort (either due to corrupted data or broken) command	To analyze write abort behavior by device	76	4
Total Recovery Operation After VDET	The total amount of recovery operations required to be done by the device while detecting internal slight power droop.	To analyze device recovery after VDET event occurs	80	4

Field Name	Description	Motivation (Host perspective)	Offset (Dc)	Size (Bytes)
Cumulative SLCBoost write payload	Accumulate the amount of host written payload that was written to SLCBoost buffer in resolution of 100MB.	To track and analyze device SLCBoost behavior	84	4
Cumulative SLCBoost BigFile mode write payload	Accumulate the amount of host written payload that was written to SLCBoost BigFile buffer in resolution of 100MB.	To track and analyze device SLCBoost BigFile mode behavior	88	4
Number of times SLCBoost BigFile mode was operated during device lifetime	Count the number of times host wrote payload to SLCBoost BigFile mode	To track and analyze device SmartLSC BigFile mode behavior	92	4
Average Erase Cycles of SLCBoost BigFile mode	The average erase count of SLCBoost BigFile buffer	To track and analyze device SmartLSC BigFile mode behavior	96	4
Cumulative Initialization Count	Number of device power up events from beginning of life	To analyze number of initialization events that occurred during device lifetime	100	4
Max Erase Cycles Type A (SLC)	The maximum erase value out of all SLC blocks.	To check product endurance variance	108	4
Max Erase Cycles Type B (TLC)	The maximum erase value out of all TLC blocks.	To check product endurance variance	112	4
Min Erase Cycles Type A (SLC)	The minimum erase value out of all SLC blocks.	To check product endurance variance	120	4
Min Erase Cycles Type B (TLC)	The minimum erase value out of all TLC blocks.	To check product endurance variance	124	4
Pre EOL warning level Type B (TLC)	Pre end-of-life (EOL) levels for device TLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode	To predict early lifetime of device	156	4
Uncorrectable Error Correction Code	The amount of UECC by the device	To analyze UECC probability during real lifetime	160	4
Current Temperature	Indicates the current temperature of the device in degrees Celsius	To track device environmental status	164	4
Min Temperature	Indicates the min temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	168	4
Max Temperature	Indicates the max temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	172	4
Reserved			176	4
Enriched Device Health Type B (TLC)	Device health (age) level in resolution of 1% (1-100) for TLC area	To check real life product endurance and lifetime	184	4
Reserved			188-190	3
Current Power mode	Device internal power state (5 states: highest 4 – lowest 0)	To know internal device power/performance state	191	1
Enriched Device Health Type A	Device health (age) level in resolution of	To check real life product endurance	192	4

Field Name	Description	Motivation (Host perspective)	Offset (Dc)	Size (Bytes)
(SLC)	1% for SLC area	and lifetime		
Pre EOL warning level Type A (SLC)	Pre end-of-life (EOL) levels for device SLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode	To predict early lifetime of device	196	4

6.3.1 Power Loss Indications

The device is capable of alerting the host to power loss events and its internal response to those occurrences. Within the EXT_CSD register, a specific field indicates whether a power loss or write abort transpired during the last shutdown. This field also reports whether a power loss was detected and successfully recovered during the latest power-up. To access this information, the host must issue the CMD8 command – SEND_EXT_CSD. This command retrieves the entire EXT_CSD structure, returning 512 bytes of data as a single block. The following table outlines the details of this field:

Table 21: Power Loss Indications

Name	Field	Size (Bytes)	Cell Type	Hex Offset	Dec.
Power Loss Indication	POWER_LOSS_REPORT	1	R	0x79	121

- Bit[2]: Recovery success. 0x1: Recover passed successfully; 0x0: Recovery failed
- Bit[1]: Recover Old Data. 0x1: Recovery to old copy of data; 0x0: No data recovery required
- Bit[0]: Power Loss Detected. 0x1: Unexpected power loss was detected – Detection is done during initialization, immediately after power up.

Note: This register will show 0x00 if power loss did not occur on the last shut down.

6.3.1 Unstable Power Supply Indications

In the event of flash voltage drop, the device may not be able to recover data already transferred to the part but not committed in the Flash. In that event, the part will “abort” the current host write and return back to host with an error indication.

The device will use BIT19 and BIT20 (cc_error) in the command response to indicate VDET error status to the host. The VDET error indication can be seen only if CMD13 was issued or in the next command response.

Examples include:

- Open Mode (CMD25+CMD12+CMD13)
In both cases, where the voltage droop occurs before or after CMD21:
– CMD12 response will not have BIT19 and BIT20 set.
– CMD13 will identify the error indication – BIT19 and BIT20 will be set in CMD13 response.

NOTE: The host may send many CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.

- Close Mode (CMD23+CMD25+CMD13)

CMD13 will identify the error indication – BIT19 and BIT20 will be set in CMD13 response.

- Single Block Mode (CMD24+CMD13)

CMD13 will identify the error indication – BIT19 and BIT20 will be set in CMD13 response.

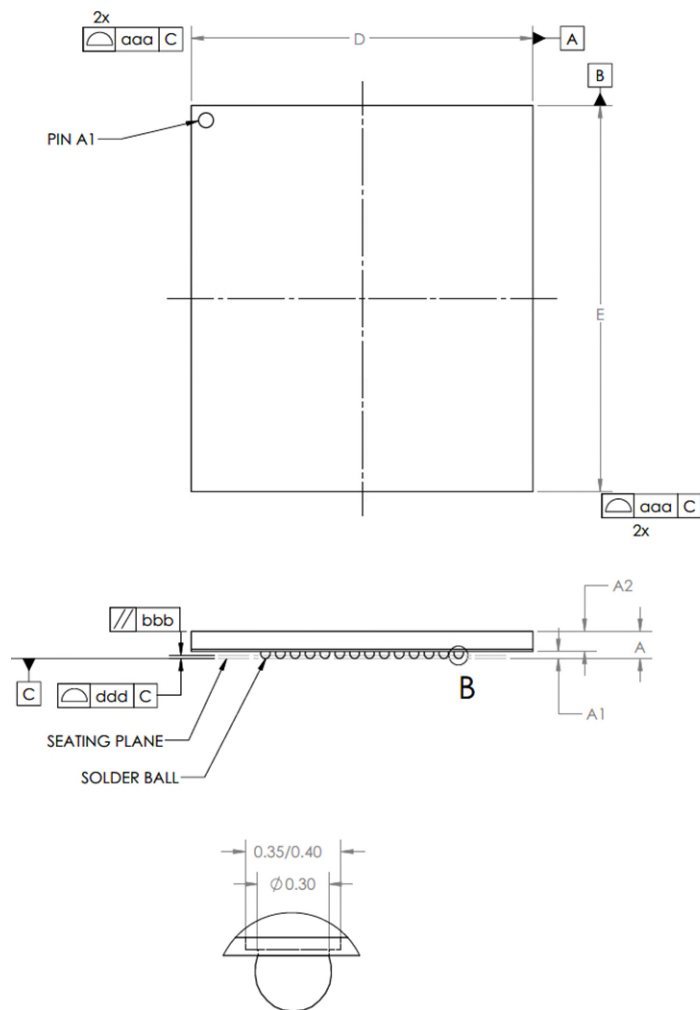
Host shall retry latest command as long as the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set.

6.4 RPMB Key

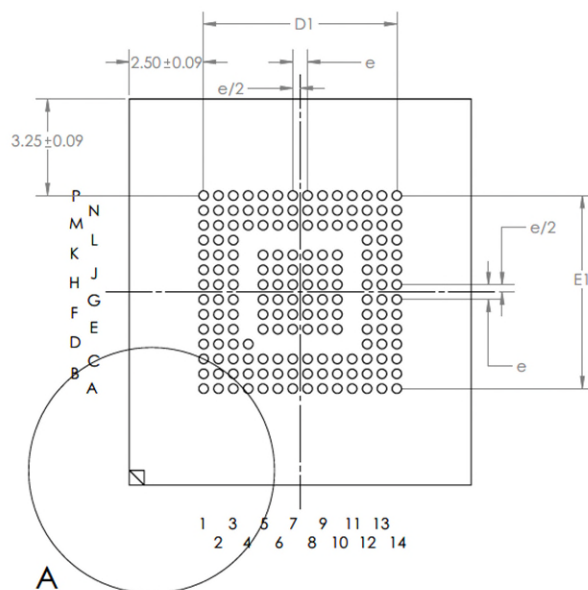
This component supports RPMB, as defined by the eMMC specification, version 5.1. RPMB provides a secure storage area for the host to safeguard critical data. To access this partition, the host programs a key into the eMMC, which serves as an authentication mechanism.

Writing to RPMB is restricted exclusively to the host that programmed the key, ensuring data integrity and security. While the stored data is readable by any entity, only the authenticated host can perform write operations.

7.0 Package Outline



BGA PAD CROSS-SECTION
(NOT TO SCALE)



DETAIL A
NOT TO SCALE

Symbol	Min	Nominal	Max
A	0.8	0.9	1
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	--	6.5	--
E1	--	6.5	--
e	--	0.5	--

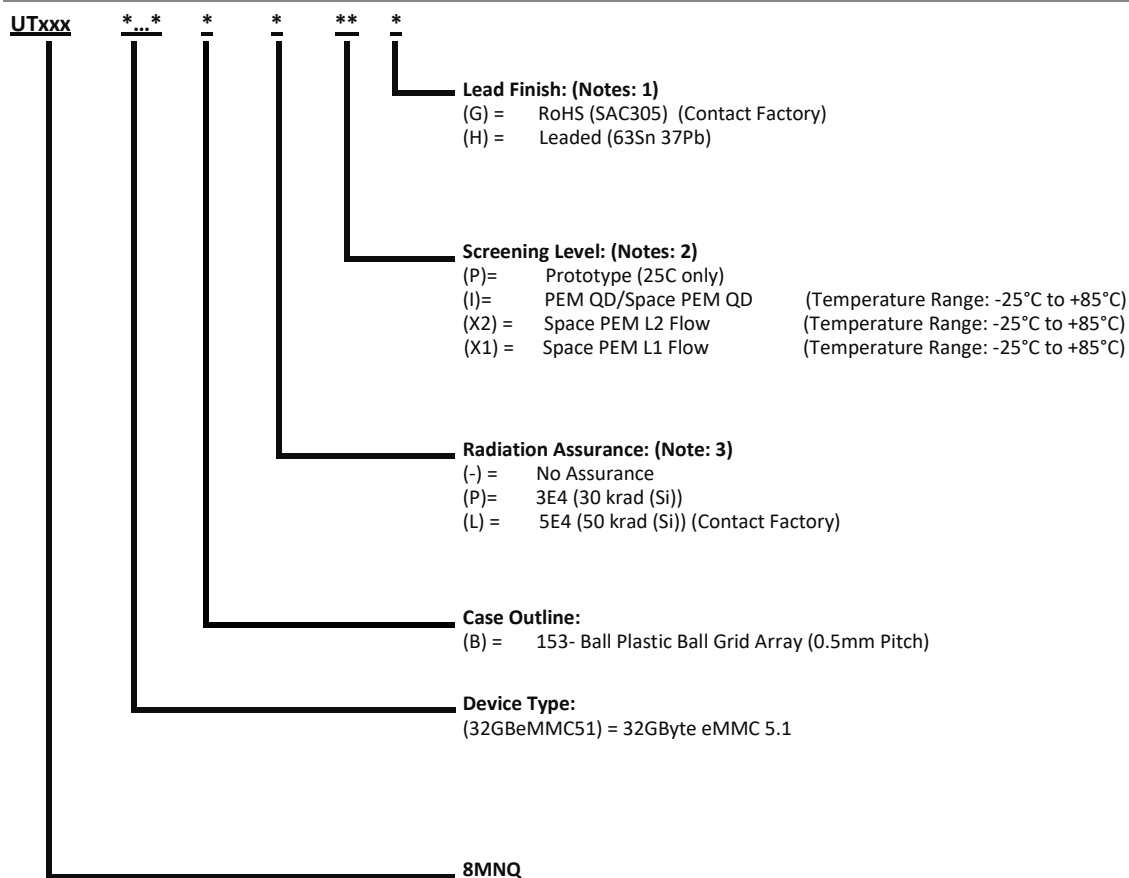
Symbol	Min	Nominal	Max
b	0.25	0.3	0.35
aaa	0.1	aaa	0.1
bbb	0.1	bbb	0.1
ddd	0.08	ddd	0.08
eee	0.15	eee	0.15
fff	0.05	fff	0.05

Note:

- all measurements in mm
- MSL 3

8.0 Ordering Information

Frontgrade Part Numbering Ordering Information



Notes:

1. Lead finish must be specified.
2. Space PEM L2 per Frontgrade Manufacturing Flows Document. Based on NASA PEM-INST-001 Level 2 criteria.
3. Radiation assurance levels may be selected for Space PEM L2 orders.

9.0 Revision History

Date	Revision #	Author	Change Description	Page #
06/16/2025	0.0.1	PBN	Initial release	

10.0 Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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