TECHNICAL NOTE

UT8SDMQ64M4x Bit Error Due To Aging

Summary

An aging study was performed on the CAES UT8SDMQ64M4x SDRAM product. The purpose of this study was to evaluate the increase of bit errors over time (ageing) as a function of temperature when biased. Ageing of the SDRAM product was performed on a total of 45 devices pulled from three different wafer lots. The devices were stressed at bias conditions of maximum supply voltage = 3.6 V and at a temperature = 125°C for an equivalent of 2600 hours when de-rated to a temperature of 105°C. The results of the study showed that all 45 devices increased in the number of bit errors as a function of stress time. Based on in-depth testing of 6 devices in obtaining the exact bit errors across the memory array, analysis indicated that the bit errors increased over time in a linear fashion. In analyzing the data, a model to predict the bit was developed to calculate the number of bit errors as a function of time (t) and temperature (T) using a linear model for the bit errors and an Arrhenius based model for temperature. The model predicts a maximum of 5497 bit errors when operating continuously for 15 years at 105°C. Additionally, the model was used in combination with a binomial distribution to calculate the probability of 1,2, and 3 bit errors per word.

1 Overview/Background

Synchronous dynamic random access memory (SDRAM) devices are used in a wide range of space applications. SDRAM is a type of volatile memory that needs to be periodically refreshed to retain its contents.

As with any memory device, bit errors are major concern, especially for high reliable systems. A bit error is an event that leads to one or more memory bits being read differently from how they were last written. Concern for bit errors stems from the fact that they can manifest from various events including aging.

In an effort to understand the bit errors due to aging in the UT8SDMQ64M48 SDRAM, CAES conducted an experiment. This document provides a summary of the experiment. This information is also applicable to the UT8SDMQ64M40 device.

2 Product Description

The product used in this experiment was the UT8SDMQ64M48 SDRAM, which is an MCM single package device utilizing six 512Mb SDRAM die.

3 Experiment

The main objective of this experiment was to investigate bit errors as a function of operational use hours (i.e. aging) Additionally, temperature acceleration effects were included in order to build product lifetime models to predict reliability in both long-term and harsh environments. Dynamic burn-in stress was utilized throughout the entire experiment in which all memory cells were continuously operated under accelerated temperature conditions.

3.1 Sample Selection

For this experiment, 45 UT8SDMQ64M48 devices were selected from production material. Device selection was based on a number of factors in order to insure the experiment population included a wide mix of material. The selection process covered items such as:

UT8SDMQ64M4x Bit Error Due To Aging

- Material from different wafer lots
- Material from different package assembly lots
- Material from different process flows (i.e. Q, Q+ level flows)
- Parts that pass 3-temp electrical test (aside from bit failures)
- Material that exhibited bit failures at each of the various temperatures

The following summarizes the mix of devices included in the experiment.

Table 1: Summary information from ATE testing.

Description	Quantity
Number of wafer lots	3
Package Styles	2
Process Flows[1]	2
Parts Passing All Electrical Tests across Temperature	17
Devices with only Bit Failures	28
Package Assembly Lots	6

Note 1: Based on the wafer lot information and data collected, this document is applicable to devices produced from wafer lots: 8009340, 8009350, 8009360, 8009370, 8009380, 8009390, 8009400.
Note 2: Includes QML Q and QML Q with additional screening as defined in SMD Section 4.1.2.

The selected devices were taken from available production material, which were at different points in the manufacturing flow. This indicates that the selected devices experienced various amounts of testing and burn-in prior to their selection for the experiment.

3.2 Test and Stress Methodology

For this experiment, a stress-measure-stress (SMS) methodology was utilized. Detailed in Figure 1 is an outline of the experiment flow.

The experiment included 6 stress cycles with both electrical and bit location testing conducted after each stress cycle. The experiment had defined stress cycles of 0, 168, 336, 504, 672, 840, and 1008 hours. During the stress cycles, devices were stressed at an accelerated temperature of 125°C to facilitate data collection for performing lifetime analysis.

The electrical test was performed using the same electrical test program used for production across three temperatures (-40°C, 25°C, 105°C). Electrical testing was performed on all 45 devices at the end of each stress cycle.

In addition to the use of the production electrical test program, a bit location test program was developed for this experiment. The bit location test program contains a collection of 32 patterns that when combined together test all memory bits in a device for both zeros and ones. The bit location testing was performed on 6 devices at the end of each stress cycle.

UT8SDMQ64M4x Bit Error Due To Aging

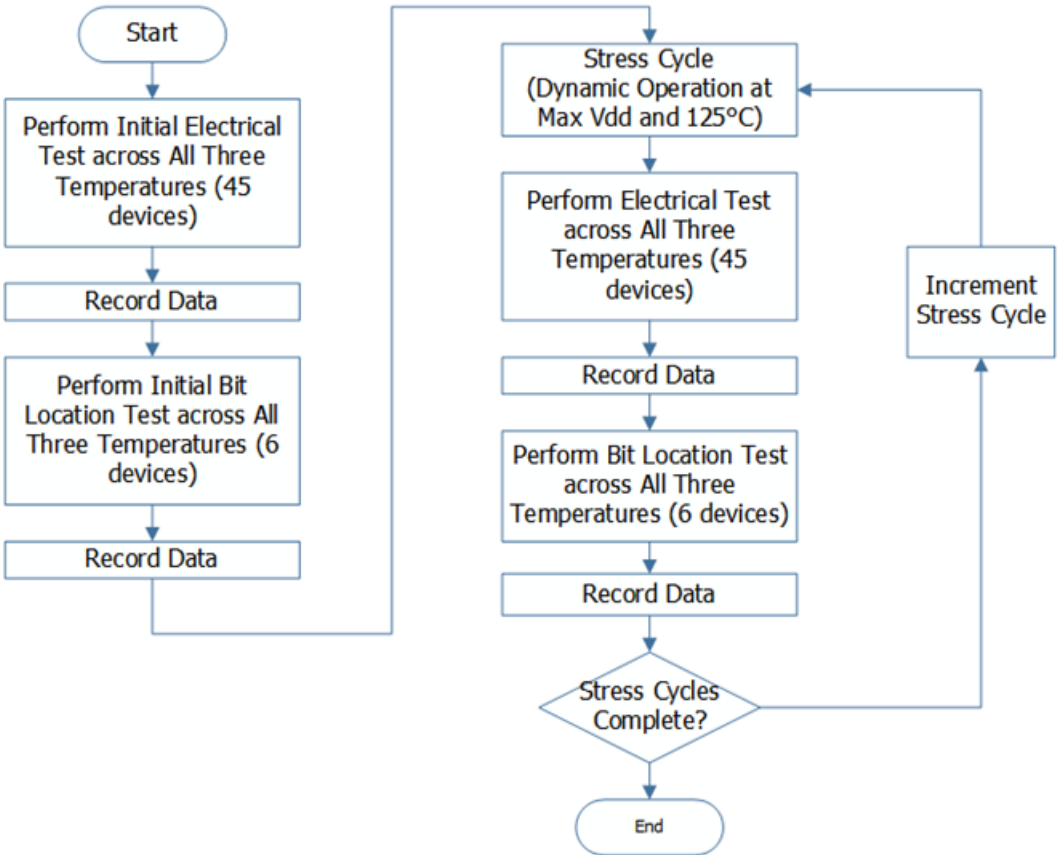


Figure 1: Flow diagram of experiment stress-measure-stress cycles.

The bit location patterns activate/write/read the data in each row/column in the same order each time. Each pattern writes values into the memory, reads the expected values, writes new values to the memory, and reads the expected values. These patterns use a 10 MHz clock frequency for writes and a 100 MHz clock frequency for reads. This combination of clock frequencies and patterns translates into a refresh time of 13.9 ms, product maximum refresh time is 32 ms.

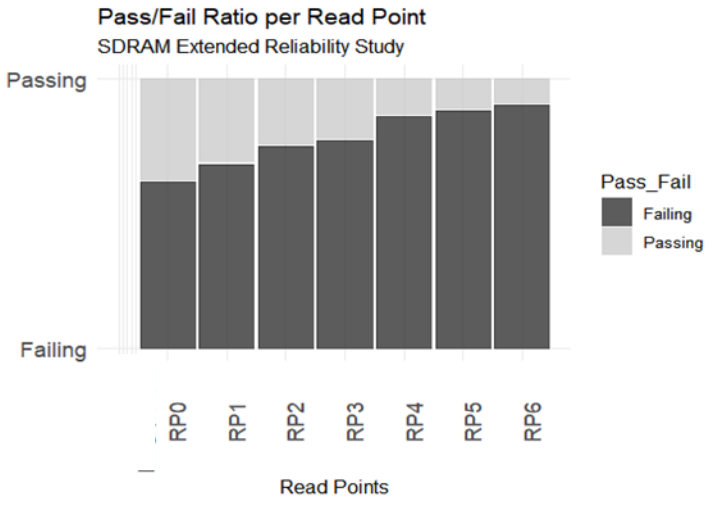
At the end of each stress cycle, product engineering performed a review of the electrical test data and retested any devices that were suspected of being false failures. This was done in an effort to minimize failure signatures that were not representative of device performance.

4 Results and Analysis

4.1 Observations from Production Electrical Tests

From the production testing, the data showed that the number of devices having bit failures increased over time. Figure 2 shows this in both graphical and table formats.

UT8SDMQ64M4x Bit Error Due To Aging



(a)

Read Point	Passing	Failing
RP0	17	28
RP168	14	31
RP336	11	34
RP504	10	35
RP672	6	39
RP804	5	40
RP1008	4	41

(b)

Figure 2: Trend results from production testing showing increasing bit errors at the end of each stress cycle. (a) Mosaic plot showing passing and failing trend. (b) Numerical account of passing and failing.

In addition to the bit failure increase across the stress cycles, the following trends were observed when analyzing the data one temperature at a time:

- Passing devices changed to failing
- Failing devices changed to passing
- Passing devices remained passing
- Failing devices remained failing

The nature of the bit failures causing passing devices to change to failing and then reverse across the different stress intervals was observed. This is discussed in a later section.

4.2 Observations from Bit Location Testing

4.2.1 Failure Mode Classifications

Two unique failure modes were identified from the bit location test results. The first failure mode ("Bit-to-Bit" Mode) is classified as having two bits that appear to have a variable resistive connection between them that share the same column address on neighboring row addresses. The Bit-to-Bit failure mode was observed during testing at all 3 temperatures, with hot being the worst case and cold being the best.

Shown in Figure 3 is a graph of the observed bit failures for the Bit-to-Bit Mode. The graph groups the rows for the specified pattern signature and shows the number of bit failures for each test temperature at each of the stress cycles. The graph provides information that some of the bit errors disappear after appearing. In addition, the graph illustrates that the bit errors range from 1 to 3, with a single occurrence of a 3 bit error.

UT8SDMQ64M4x Bit Error Due To Aging

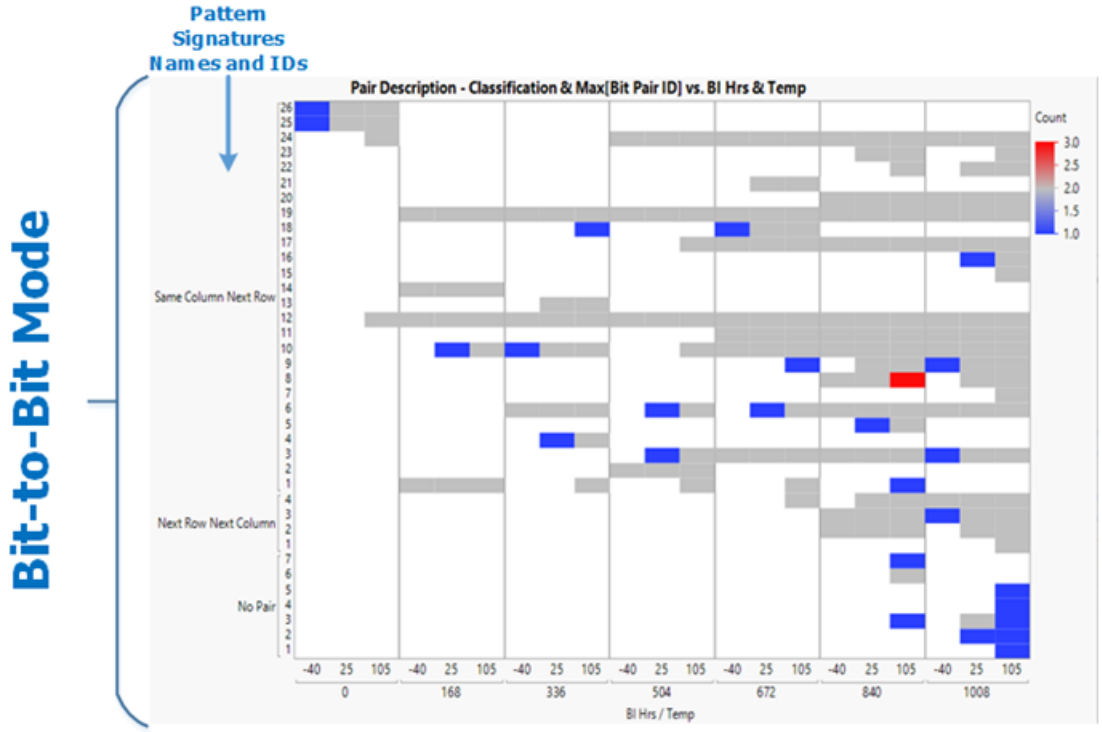


Figure 3: Graph showing Bit-to-Bit Mode bit errors for each stress cycle as a function of temperature. Numbers in the y-axis are row numbers associated with the pattern signature.

Observations of the Bit-to-Bit failure mode suggests that a variable resistive bridging between neighboring bit cells causes a progression of symptoms as the resistance values decreases. Based on the observations of the bit error changes over time, the progression appears to follow the resistive pattern of:

Resistance Between Neighboring Bit Cells			
High Resistance →			→ Low Resistance
No failure observed	One bit observed failure once	Two bits observed failure once each	One bit observed failing twice
Resistance between bits is high enough to prevent changes to the measured values	Bit fails when it should have been in charged state	Bits fail when they should have been in the charged state	Bit fails once for the charged state, once for the discharged state

Figure 4: Illustration of impact of bit-to-bit bridging resistance on bit errors.

The variable resistance shown in Figure 4 is also used to help explain the occurrence of the 1 bit failures and 3 bit failures.

The second failure mode ("Cold" Mode) was classified as having multiple bit errors on multiple column addresses, all on the same row address. This failure mode was observed only at cold (i.e. "Cold" Mode), and where only observed after some of the stress cycles. Another characteristic of the failure mode is that the bit errors often appeared and then disappeared as a function of the stress cycles. This is illustrated in Figure 5.

UT8SDMQ64M4x Bit Error Due To Aging

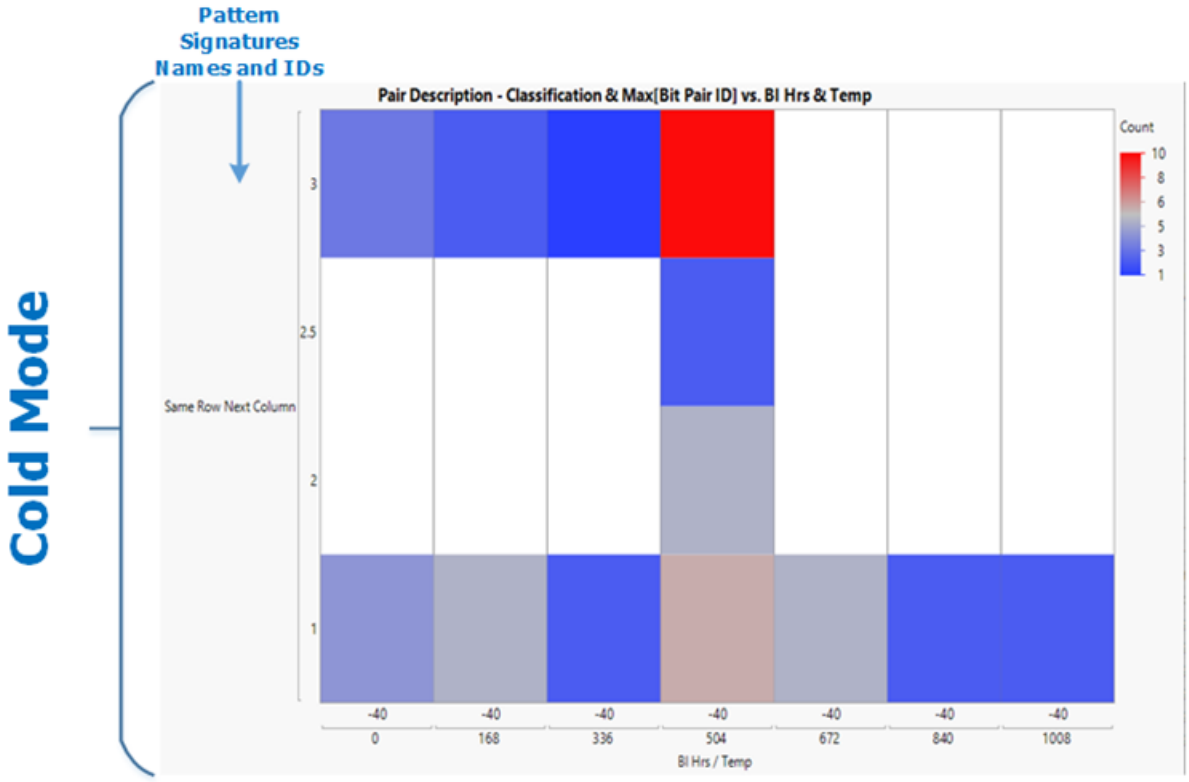


Figure 5: Graph showing Cold Mode bit errors for each stress cycle as a function of temperature. Numbers in the y-axis are row numbers associated with the pattern signature.

4.2.2 Row Locations for Unique Failing Bits

Further observations of the data indicated that a majority of the bit errors occurred in rows 0 and row 1 of the memory array. Figure 6 shows the number of bit errors captured for each unique row across all the die (6 device * 6 die = 36 total die) when tested at each of the test temperatures. Further analysis of the data indicated the ~70% of the observed failing bits were located in row 0 and row 1.

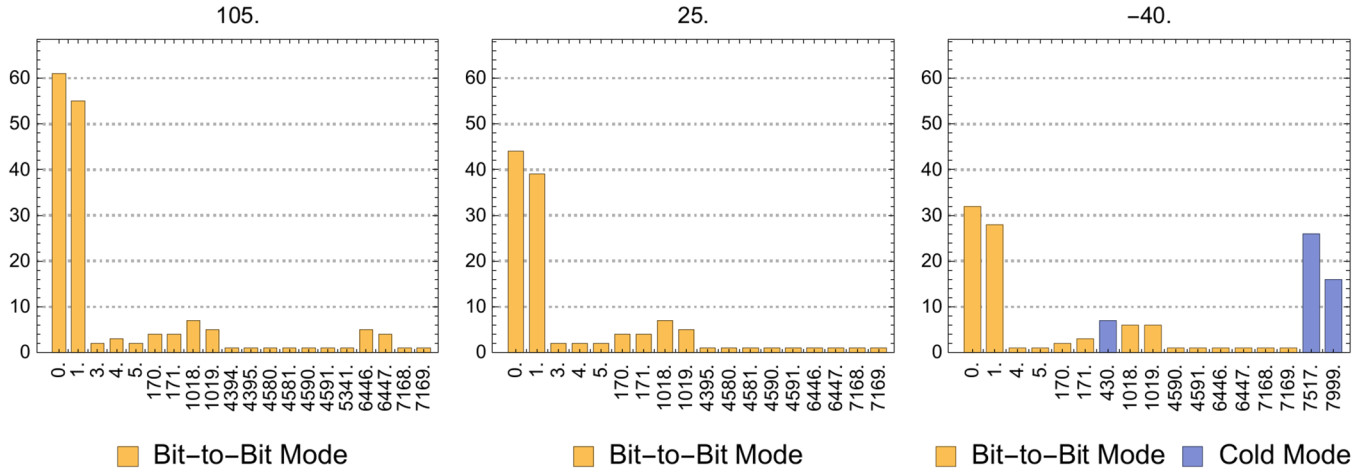


Figure 6: Graphs showing unique bit errors per row for both the Bit-to-Bit and Cold modes for each of the test temperature from the bit location testing.

UT8SDMQ64M4x Bit Error Due To Aging

4.2.3 Failing Bit Pairs

Failing bit pairs were observed between row number modulo 4 = 0&1 and 2&3. And based on review of the memory architecture, these are consistent with rows where one row stores true data while the other stores complement data. No failing bit pairs were observed between row number modulo 4 = 1&2 or 3&0. These row combinations are consistent with rows that use the same charge/logic (true data or complement data).

Given the charge/logic mapping and the test program methods, it is more likely that resistive bridging would be found between rows where the row number modulo 4 is 0&1 or 2&3.

Based on the test program used for the experiment, detection of resistive bridging between any two rows is expected to be observed on half of the rows. Therefore, the probability of observing failures between any given row is 50%. And although the presence of a majority of the failing bits occurred on row 0 and row 1 giving strong evidence that these failures are dependent on row position, the 50% estimate is to provide a conservative approach for the bit error prediction analysis described in upcoming sections.

4.2.4 Bit Pair DQs

Based on memory architecture reference material, it suggests that certain DQ pins are near each other as depicted in Figure 7. The reference material also suggests that in a given bank, the bits related to 4 DQ pins are located in the top half of the bank, and the bits related to the other 4 DQ pins are located in the bottom half of the bank.

Assuming that all DQ7 and DQ1 are adjacent and then all DQ6 and DQ0 are also all adjacent, the probability that the bit location program would find an existing failure would be near zero (1/2048). This is an estimate for the lowest probability. For a high side estimate, it is assumed that DQ7/DQ1 is interleaved with DQ6/DQ0 and the expectation for observing a failure would be half of the time.

4.3 Bit Error Prediction Model

Regression analysis of stress data over time allows for creating lifetime predictive modeling. For this experiment, time is based on the equivalent time at a use temperature of 105°C. Therefore, the total accumulated time that the devices were under temperature acceleration is normalized to the use temperature is based on an Arrhenius based temperature acceleration model:

$$AF_{Temp} = Exp\left[\frac{E_a}{k_B} * \left(\frac{1}{T_{reference}} - \frac{1}{T_{use}}\right)\right] \quad (1)$$

Where

- E_a = activation Energy in eV = 0.45 eV
- k_B = Boltzmann's constant = 8.62 x 10^{-5} eV/K
- T_{use} = use temperature in K
- $T_{reference}$ = reference temperature in K = (378K = 105°C + 273)

UT8SDMQ64M4x Bit Error Due To Aging

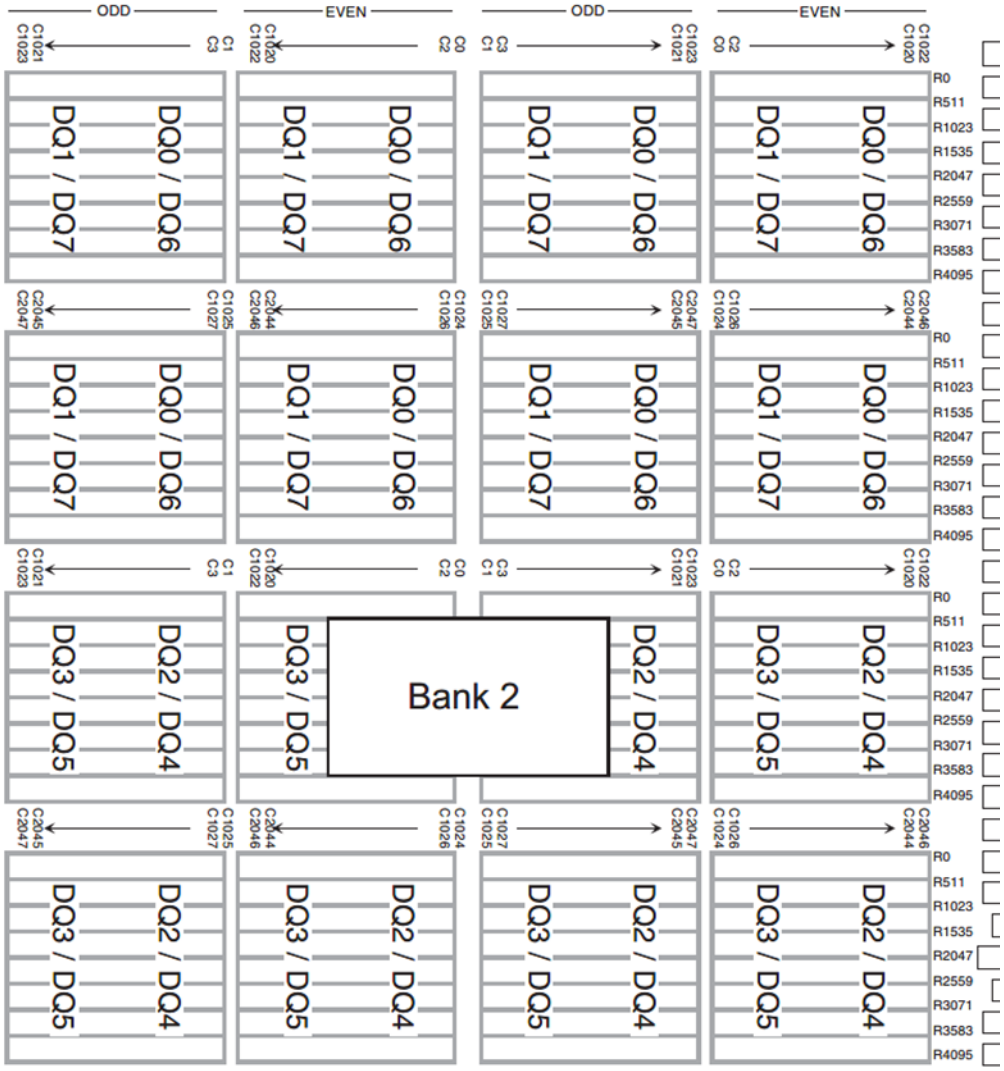


Figure 7: Illustration of DQ relationship in the memory architecture.

Using an activation energy of 0.45 eV, the device hours at 105°C were calculated and analysis performed for the bit error results for each temperature. Figure 8 shows the worst case bit error results which occurred at 105°C.

UT8SDMQ64M4x Bit Error Due To Aging

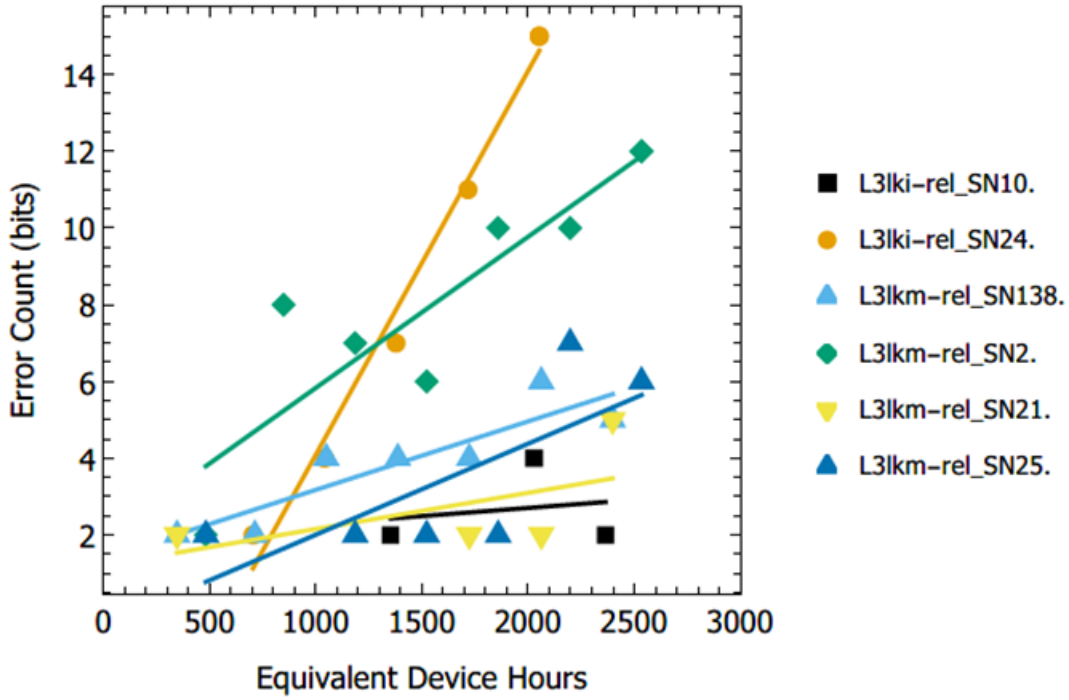


Figure 8: Plot of bit errors and regression models for the each of the devices. Data is from the 105°C bit location testing.

Based on the regression analysis, different slopes (i.e. error rates (errors/hr)) for each of the test temperatures were observed. Analysis was performed with all the data and with the Cold Mode data removed. And with the Cold Mode data removed only the -40°C error rate changed. Shown in Table 2 is the maximum error rate calculated for each temperature. And as a note, the table does include a 4x factor.

Table 2: Calculated error rates from the bit location data for test data collected at each test temperature.

	All Data			With Cold Mode Data Removed		
Temperature (°C)	Error Rate (error/hr)	Bit Error Rate[1] (error/bit-hr)	Bit Error Rate[1,2] (error/bit-day)	Error Rate (error/hr)	Bit Error Rate[1] (error/bit-hr)	Bit Error Rate[1] (error/bit-day)
-40	0.0056	1.8×10^{-12}	4.3×10^{-11}	0.0088	2.8×10^{-12}	6.7×10^{-11}
25	0.0248	7.6×10^{-12}	1.8×10^{-10}		No Change	
105	0.0420	1.3×10^{-11}	3.1×10^{-10}		No Change	

Note 1: Total number of bits per device = 3,221,225,472.
Note 2: This bit error rate includes a 4x factor to account for potentially missed errors due to the test pattern used.

Using the worst-case linear regression results (from SN24 at 105°C), the resultant model is:

$$No.\,of\ Bit\ Errors_{105°C} = -5.6 + 0.0105 * t \quad (2)$$

Where t is time in hours. As mentioned in previous sections, it was observed that there was the possibility that 75% of bit errors may not have been observed. To account for this, the linear regression model is increased by 4x resulting in:

$$No.\,of\ Bit\ Errors_{105°C} = -22.8 + 0.042 * t \quad (3)$$

UT8SDMQ64M4x Bit Error Due To Aging

As an example, assuming continuous use at 105°C and a 15 year mission life, the total bit errors is estimated as 5497 using equation (3). Whereas the following gives an example of using the AF_{Temp} to calculate the number of bit errors for a given temperature and mission life.

For example, what are the estimated number of bit errors at the end of the mission life, assuming a constant use temperature of 80C and a mission life to 5 years?

First, using equation (3), determine the number of bit errors for the mission life (this is still at the reference temperature of 105°C):

$$No.of\ Bit\ Errors_{105°C} = -22.8 + 0.042 * (5 * 365 * 24) = 1816$$

Then, using equation (1), calculate the AF_{Temp} for 80°C:

$$AF_{Temp=80°C} = Exp\left[\frac{0.45}{8.62 \times 10^{-5}} * \left(\frac{1}{(105 + 273.15)} - \frac{1}{(80 + 273.15)}\right)\right] = 0.38$$

Then multiply the bit errors at 105°C by the temperature acceleration factor to get the bit errors at the use temperature of 80°C:

$$No.of\ Bit\ Error_{80°C} = AF_{Temp=80°C} * 1816 = 0.38 * 1816 = 690$$

4.4 Bit Error Probability

For memory type devices, to estimate the probability of a bit error within a word, the binomial distribution can be used:

$$Pr(x) = \binom{n}{k} Pe^k (1 - Pe)^{n-k} \quad (4)$$

Where

- Pe = probability that a bit failed
- n = number of bits per word (= 48)
- k = number of occurrences per n

To use the binomial distribution, first the bit error probability (*Pe*) must be determined based on:

$$Pe = \frac{\#\ of\ bit\ errors}{total\ bits} \quad (5)$$

And for this experiment, due to the large percentage of bit errors associated with row 0 and row 1, the bit error probability will be determined based on two different approaches:

- Approach #1 – Single bit error probability
  - Pe = worst case bit error probability across all rows
- Approach #2 – Separate bit error probability based on row segmentation
  - $Pe_{rows0,1}$ = bit error probability using only bit errors associated with row 0 and row 1
  - $Pe_{rows>=2}$ = bit error probability using bit errors associated with rows >= 2

UT8SDMQ64M4x Bit Error Due To Aging

For each approach, the number of bit errors will be based on the linear regression equation from Section **Error! Reference source not found.**.

4.4.1 Approach #1

For this approach, using equations (3) and (5), the Pe is given by:

$$Pe = \frac{-22+0.042*t}{3{,}221{,}225{,}472} \quad (6)$$

As seen by the time dependence for the Pe, the probability of a bit failure is also time dependent. As such, the follow graphs show the probability (Pr) of failure for 1, 2, and 3 bit errors per 48-bit word as a function of time. Where the total bits used in the denominator is the total bits in the SDRAM.

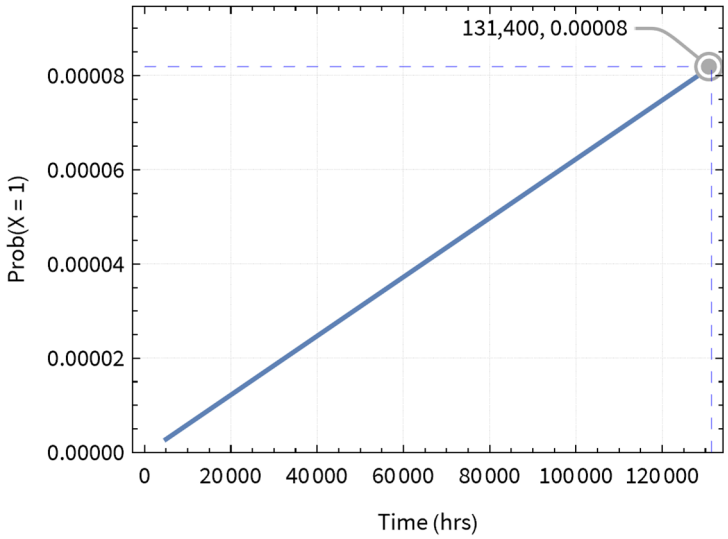


Figure 9: Plot of equation (6) showing probability of 1-bit error in a 48-bit word over time.

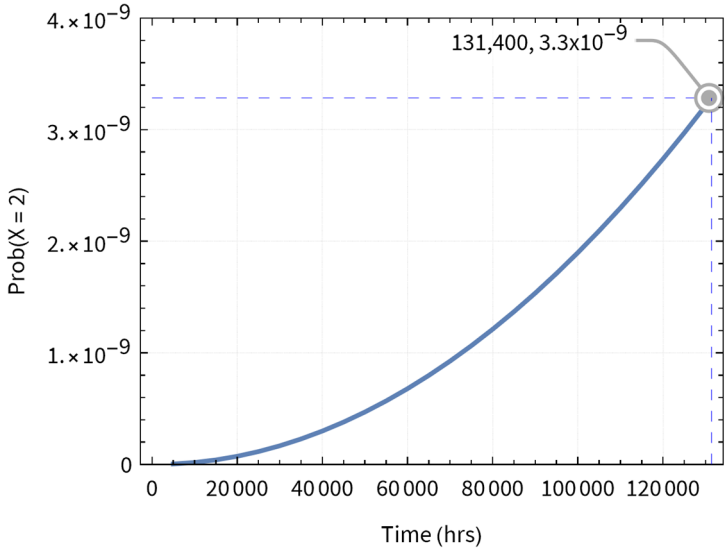


Figure 10: Plot of equation (6) showing probability of 2-bit errors in a 48-bit word over time.

UT8SDMQ64M4x Bit Error Due To Aging

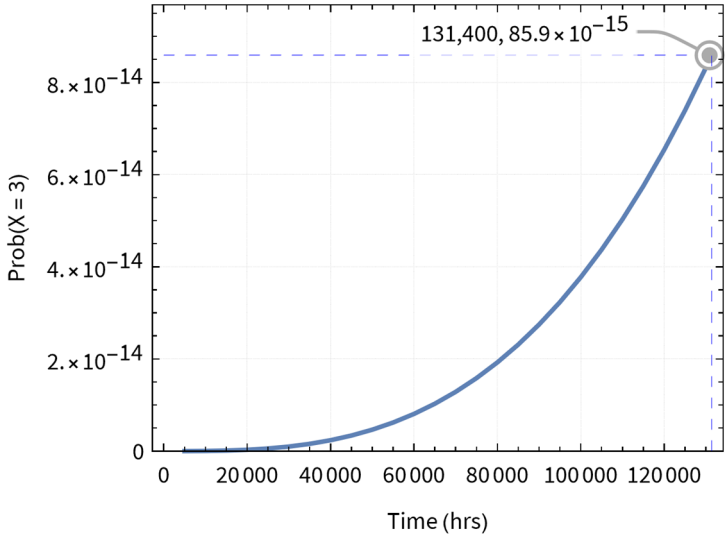


Figure 11: Plot of equation (6) showing probability of 3-bit errors in a 48-bit word over time.

4.4.2 Approach #2

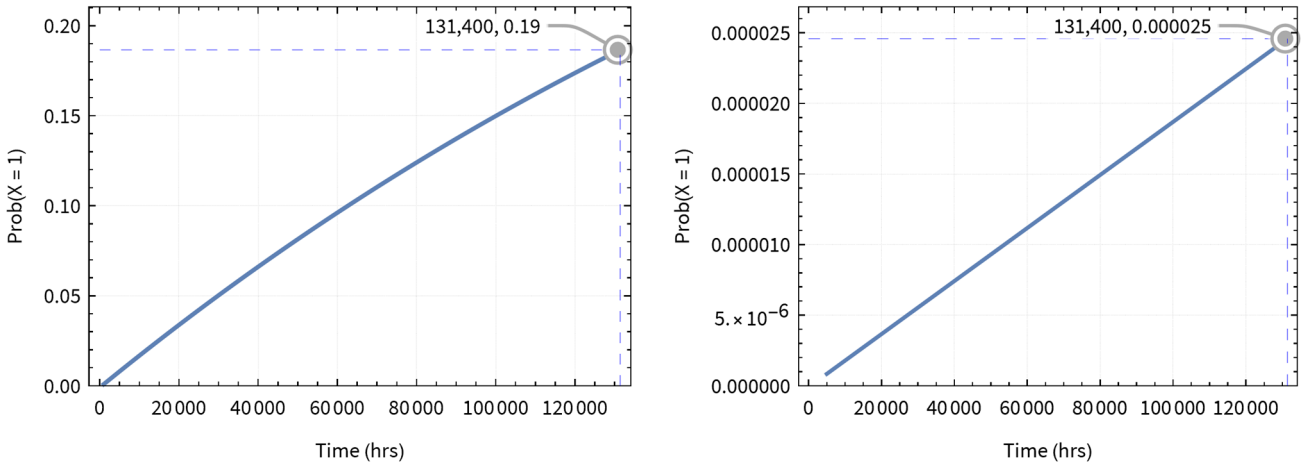
The second approach partitions the bit errors based on the observation that row 0 and row 1 had majority (70%) of the errors. As such the two different Pe values are calculated as:

$$Pe_{rows0,1} = \frac{0.7*(-22+0.042*t)}{786{,}432} \quad (7)$$

$$Pe_{rows\geq 2} = \frac{0.3*(-22+0.042*t)}{3{,}220{,}439{,}040} \quad (8)$$

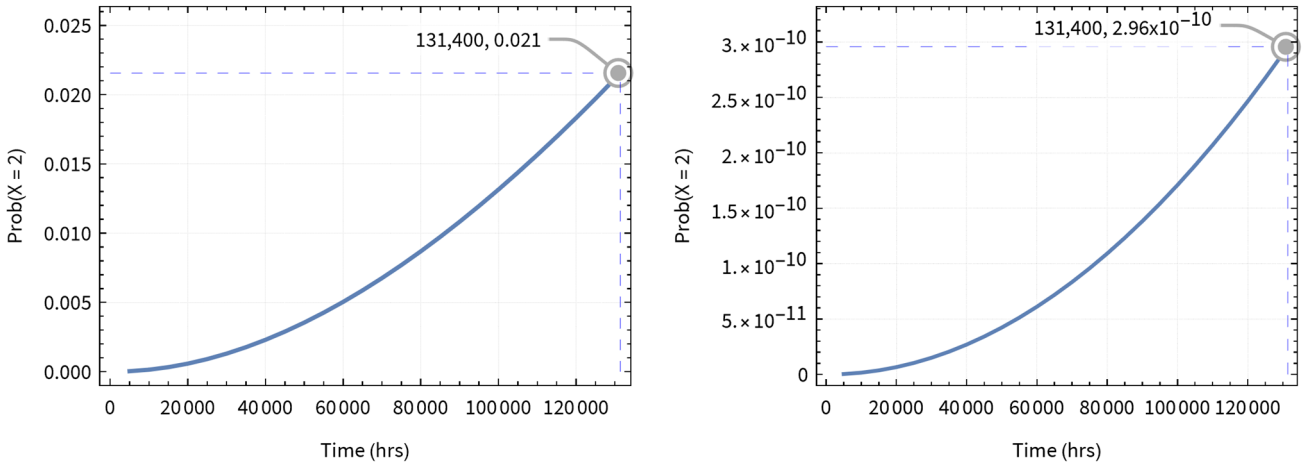
Similar to the first approach, Pe has a time dependence, therefore the probability of a bit failure is also time dependent. As such, the follow graphs show the probability (Pr) of failure for 1, 2, and 3 bit errors per 48-bit word as a function of time. Where the total bits used in Eq. (7) are based on rows 0 and 1 and for Eq. (8) the total bits are based on the remaining rows.

UT8SDMQ64M4x Bit Error Due To Aging



(a) (b)

Figure 12: Plot of probability of 1-bit error in a 48-bit word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).



(a) (b)

Figure 13: Plot of probability of 2-bit errors in a 48-bit word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).

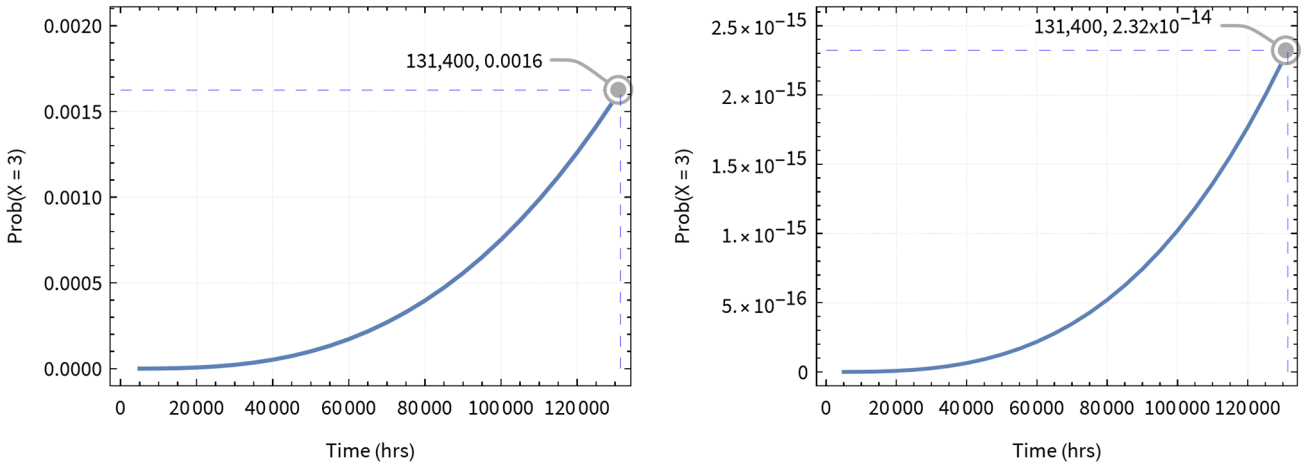


Figure 14: Plot of probability of 3-bit errors in a 48-bit word over time for (a) Rows 0 and 1 only using equation (7) and (b) all other rows using equation (8).

5 Conclusion

This technical note provides a summary of bit errors observed during a temperature accelerated stress testing of the UT8SDMQ64M48. It was observed that the bit errors continued to increase over time. From the data, a lifetime predictive model was developed. Additionally, the linear model was utilized to illustrate the change in the error probability over time. Furthermore, the linear model was using in combination with a binomial distribution to predict the probability of bit errors within a 48-bit word for 1, 2, and 3 bit errors.

6 Revision History

Date	Revision	Author	Change Description
05/17/2022	1.0	AW/NG/ML	Initial Release
05/26/2022	1.1	AW	Update Table 2 by increasing the rates by 4x to better reflect the final error rates that may be possible. Updated Figure 11 with the correct error value shown on the figure.
06/09/2022	1.2	AW	In section 4.3 changed the bit errors from 5518 to 5497. Added example for using temperature acceleration factor.
09/05/2022	1.3	AW	Updated equation 4 with the proper notation.
10/02/2022	1.4	AW	Added executive summary.

4350 Centennial Blvd. | Colorado Springs CO 80907 USA | 1-800-645-8862 | caes.com