



FRONTGRADE

PRELIMINARY DATASHEET

SimpliStor2.5T-SVPX

SpaceVPX 2.5TB Solid State Data Recorder

3/30/2026
Version #: 2.3



Introduction

The **Frontgrade SimpliStor™ 2.5T Solid-State Data Recorder (SSDR)** is a next-generation, radiation-tolerant data recorder designed specifically for modern space missions that demand high-capacity, high-throughput data storage. Built to endure the extreme conditions of space, SimpliStor provides a robust and efficient solution for data-intensive operations, such as Earth observation, scientific payload data capture, and real-time on-board analysis.

Housed in a compact 3U SpaceVPX form factor, SimpliStor delivers **2.5 terabytes of storage capacity** using **SLC-mode flash**, offering up to **33 minutes of continuous recording at 10 Gbps**. Its unique combination of performance, radiation resilience, and flexible I/O interfaces makes it ideally suited for mission profiles that cannot compromise on data availability, integrity, or speed.

Key Advantages

High Performance Storage

SimpliStor's architecture is built for speed and reliability. It supports **10 Gbps data rates** for both recording and playback, with a "store-to-full" recording policy ensuring no gaps in data continuity. With latency as low as **100 microseconds (TBC)**, SimpliStor meets the real-time demands of edge data capture and decision-making.

The drive is populated with **TLC NAND devices operating in pseudo-SLC mode**, providing enhanced endurance and data integrity. At full throughput, users can expect **up to 100 petabytes of lifetime writes** over five years, enabling continuous operation for long-duration missions.

Flexible System Integration

Network Attached Storage (NAS)

SimpliStor functions as a standalone NAS unit, using a **single-lane 10GBase-KR Ethernet interface** to provide fast access to recorded data via **User Datagram Protocol (UDP)**. This simplicity enables rapid data offload and integration with networked payloads or onboard systems.

PCIe Expansion Plane (Future Expansion with Firmware Update)

For systems requiring faster access or local processing, SimpliStor offers a **4-lane PCIe Gen 3.0 interface** on the SpaceVPX expansion plane. This feature enables tight coupling with processing modules for real-time data analytics, autonomous decision-making, or software-defined payload operations.

Applications

- High-resolution Earth imaging missions
- Scientific payload data collection
- Onboard processing for autonomous spacecraft
- Tactical surveillance from LEO/GEO satellites
- Deep space data logging
- CubeSat and SmallSat with high-data payloads

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
SSDRG12T-SVPX-OP-EDU	EDU/EM (Room Temp only)	Lab / Development Use Cases
SSDRG12T-SVPX-OP-FM4	COTS Parts Grade (-10°C to +50°C)	Target Mission Class D
SSDRG12T-SVPX-OP-FM3	Level 3 Parts Grade (-10°C to +50°C)	Target Mission Class C
SSDRG12T-SVPX-OP-FM2	Level 2 Parts Grade (-10°C to +50°C)	Target Mission Class B

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds.

Other Build Options: The standard SimpliStor build uses TE Connectivity connectors for P0, P1, and P2 and operates in the 12V-only configuration. Contact factory if you need to invoke alternative build options.

Alternative Build Options	PN Suffix Option
Standard Configuration: 12V-Only power and TE Connectivity Backplane	Blank
Configuration Option 1: 12V VS1 and 3.3V Aux and TE Connectivity Backplane	-01
Configuration Option 2: 12V-Only and Smith's KVPX Backplane	-02
Configuration Option 3: 12V VS1 and 3.3V Aux and Smith's KVPX Backplane	-03

Features

Performance

- 2.5TB SLC Capacity
 - Array populated with TLC NAND devices configured in pseudo-SLC mode
- Recording & Playback data rate: 10Gbps
 - 100µs latency (TBC)
 - "Store-to-full" recording policy
 - Full capacity recording duration 33 mins @ 10Gbps
 - Recording duration increases with lower link rates
- Full recorder erase <1 min. (TBC)

Interfaces

- 12V VS1 input Power from SpaceVPX Backplane and optional 3.3V_AUX
- Control Plane: 2x 1000Base-T ethernet
- 1x 10GbaseKR ethernet Data Plane
 - Maximum record throughput 10Gbps
- (Future Option) 4-lane PCIe 3.0 Expansion Plane
- SpaceVPX Slot Profile: SLT3-PAY-2F2T1Q-14.2.1

File System Protocols and Formats

- UDP

Radiation Performance

- TID: 30k rad(Si) to 50k rad(Si) unshielded
- SEL immune $\leq 37 \text{ MeVcm}^2/\text{mg}$
- SEFI recovery down time: <10 mins per 10 years GEO

Mass, Thermal, & Environmental Targets

- Mass: <0.65kg, standard 3U-160 VPX form factor
- -10°C to +50°C operational
- Dynamic Power: <25W Typ. / <34W Max W.C.
 - Dynamic assumes 10Gbps data recording
- Data Retention >7 years @ NAND Tj = 85°C
- Endurance: up to 40k per block
- Lifetime writes: 100 petabytes @ 10Gbps (2.5 years)
- 43 DDPD for 2.5 years
- 21.5 DDPD for 5 years
- 11 DDPD for 10 years

Block Diagram

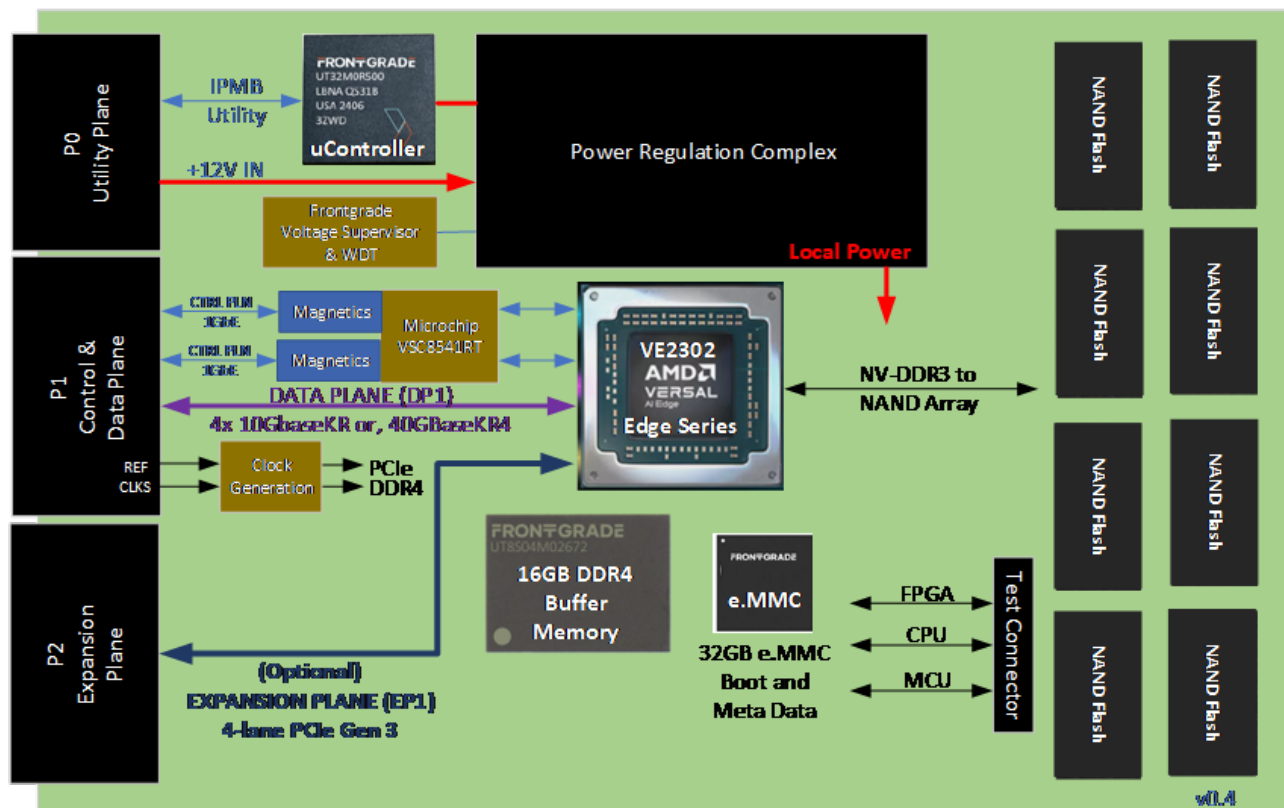


Figure 1. SimpliStor 2.5T-SVPX High Level Block Diagram

Backplane Slot Profile and Connection Tables

The SimpliStor 2.5T-SP Solid State Data Recorder is in a 3U, 160mm, SpaceVPX form factor with VITA 78.0 backplane profile SLT3-PAY-2F2T1Q-14.2.1. The P0, P1 and P2 Connector Pinouts are depicted below.

P0 Backplane Connector Signal/Pin Mapping

Connector Manufacturer: TE Connectivity (Option for Smiths Interconnect)

Manufacturer Part Number: 2102772-4 (Optional Smiths TBS)

Mates with Backplane Connector Part Number: TE Connectivity TBS (Smiths TBS)

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Figure 2. SimpliStor Module P0 Connector Pinout

Table 1. SimpliStor P0 Connection Table

P0 Connector Pin Number	P0 Connector Name	SimpliStor Signal Connection
RowG1	Vs1	+12V
RowG2	Vs1	+12V
RowG3	Vs3	N/C
RowG4	SM2	SM2_RESET_IN
RowG5	GAP*	GAP_VPX
RowG6	GA3*	GA3_VPX
RowG7	TCK	JTAG_TCK
RowG8	GND	GND
RowF1	Vs1	+12V
RowF2	Vs1	+12V
RowF3	Vs3	N/C
RowF4	SM3	SM3_STAT_OUT

P0 Connector Pin Number	P0 Connector Name	SimpliStor Signal Connection
RowF5	GA4*	GA4_VPX
RowF6	GA2*	GA2_VPX
RowF7	GND	GND
RowF8	REF_CLK-	N/C
RowE1	Vs1	+12V
RowE2	Vs1	+12V
RowE3	Vs3	N/C
RowE4	GND	GND
RowE5	GND	GND
RowE6	GND	GND
RowE7	TDO	JTAG_TDO
RowE8	REF_CLK+	N/C
RowD1	No Pad*	N/C
RowD2	No Pad*	N/C
RowD3	No Pad*	N/C
RowD4	-12V_Aux	N/C
RowD5	3.3V_Aux	3.3V
RowD6	+12V_Aux	N/C
RowD7	TDI	JTAG_TDI
RowD8	GND	GND
RowC1	Vs2	N/C
RowC2	Vs2	N/C
RowC3	Vs3	N/C
RowC4	GND	GND
RowC5	GND	GND
RowC6	GND	GND
RowC7	GND	GND
RowC8	AUX_CLK-	N/C
RowB1	Vs2	N/C
RowB2	Vs2	N/C
RowB3	Vs3	N/C
RowB4	SYSRESET*	SYSRESET#
RowB5	SM0	IPMB_SDA_IN
RowB6	GA1*	GA1_VPX
RowB7	TMS	JTAG_TMS
RowB8	AUX_CLK+	N/C
RowA1	Vs2	N/C
RowA2	Vs2	N/C

P0 Connector Pin Number	P0 Connector Name	SimpliStor Signal Connection
RowA3	Vs3	N/C
RowA4	NVMRO	N/C
RowA5	SM1	IPBM_SCL_IN
RowA6	GA0*	GA0_VPX
RowA7	TRST*	JTAG_TRST
RowA8	GND	GND

P1 Backplane Connector Signal/Pin Mapping

Connector Manufacturer: TE Connectivity (Option for Smiths Interconnect)

Manufacturer Part Number: 2102771-4 (Optional Smiths KVPX+ YGP064-001P)

Mates with Backplane Connector Part Number: TE Connectivity TBS (Smiths KVPX+ YGS064-004ANH)

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 X8	SYS_CONP*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2 X8	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		REF_CLK1-	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	REF_CLK1+	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		REF_CLK2-	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane	REF_CLK2+	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

Figure 3. SimpliStor Module P1 Connector Pinout

The SpaceVPX Control Planes of the P1 connector (Figure 3) are implemented with 1000Base-T ethernet utilizing the Microchip VSC8541RT physical transceivers which are connected to the GEM0 and GEM1 ethernet interfaces on the FPGA processor subsystem.

The Data Plane is implemented as a single 40GBase-KR4 ethernet interface or 4x 10Gbase-KR interfaces via the MRMAC on the Versal VE2302 FPGA. User defined signals on P1 are implemented with TBD LVDS pairs to the FPGA.

Table 2. SimpliStor P1 Signal Connection

P1 Connector Pin Number	P1 Connector Name	SimpliStor Signal Connection
RowG1	SYS_CONP*	N/C
RowG2	GND	GND
RowG3	VBAT	N/C
RowG4	GND	GND
RowG5	SYS_CON*	N/C
RowG6	GND	GND
RowG7	REF_CLK1-	N/C
RowG8	GND	GND
RowG9	REF_CLK1+	N/C
RowG10	GND	GND
RowG11	REF_CLK2-	CLK_VPXREF2_IN_N
RowG12	GND	GND
RowG13	REF_CLK2+	CLK_VPXREF2_IN_P
RowG14	GND	GND
RowG15	Maskable Reset*	VPX_HardReset
RowG16	GND	GND
RowF1	GND	GND
RowF2	DP01-TD1-	VPX_10GBE_TX1_N
RowF3	GND	GND
RowF4	DP01-TD3-	VPX_10GBE_TX3_N
RowF5	GND	GND
RowF6	DP02-TD1-	N/C
RowF7	GND	GND
RowF8	DP02-TD3-	N/C
RowF9	GND	GND
RowF10	UD	UC_UART_TX_N
RowF11	GND	N/C
RowF12	UD	N/C
RowF13	GND	N/C
RowF14	CPtp02-DD-	N/C
RowF15	GND	N/C
RowF16	CPtp01-DD-	VPX_1GBE_RX2_N
RowE1_Even	GND-J1	N/C
RowE2_Even	DP01-TD1+	VPX_10GBE_TX1_P
RowE3_Even	GND-J1	N/C
RowE4_Even	DP01-TD3+	VPX_10GBE_TX3_P

P1 Connector Pin Number	P1 Connector Name	SimpliStor Signal Connection
RowE5_Even	GND-J1	N/C
RowE6_Even	DP02-TD1+	N/C
RowE7_Even	GND-J1	N/C
RowE8_Even	DP02-TD3+	N/C
RowE9_Even	GND-J1	N/C
RowE10_Even	UD	UC_UART_TX_P
RowE11_Even	GND-J1	N/C
RowE12_Even	UD	N/C
RowE13_Even	GND-J4	N/C
RowE14_Even	CPtp02-DD+	N/C
RowE15_Even	GND-J4	N/C
RowE16_Even	CPtp01-DD+	VPX_1GBE_RX2_P
RowE1_Odd	DP01-TD0-	VPX_10GBE_TX0_N
RowE2_Odd	GND-J1	N/C
RowE3_Odd	DP01-TD2-	VPX_10GBE_TX2_N
RowE4_Odd	GND-J1	N/C
RowE5_Odd	DP02-TD0-	N/C
RowE6_Odd	GND-J1	N/C
RowE7_Odd	DP02-TD2-	N/C
RowE8_Odd	GND-J1	N/C
RowE9_Odd	UD	VERSAL_UART_TX_N
RowE10_Odd	GND-J1	N/C
RowE11_Odd	UD	CPU_JTAG_TDO
RowE12_Odd	GND-J1	N/C
RowE13_Odd	CPtp02-DB-	N/C
RowE14_Odd	GND-J4	N/C
RowE15_Odd	CPtp01-DB-	VPX_1GBE_RX1_N
RowE16_Odd	GND-J4	N/C
RowD1	DP01-TD0+	VPX_10GBE_TX0_P
RowD2	GND	GND
RowD3	DP01-TD2+	VPX_10GBE_TX2_P
RowD4	GND	GND
RowD5	DP02-TD0+	N/C
RowD6	GND	GND
RowD7	DP02-TD2+	N/C
RowD8	GND	GND
RowD9	UD	VERSAL_UART_TX_P
RowD10	GND	GND

P1 Connector Pin Number	P1 Connector Name	SimpliStor Signal Connection
RowD11	UD	N/C
RowD12	GND	GND
RowD13	CPTp02-DB+	N/C
RowD14	GND	GND
RowD15	CPTp01-DB+	VPX_1GBE_RX1_P
RowD16	GND	GND
RowC1	GND	GND
RowC2	DP01-RD1-	VPX_10GBE_RX1_N
RowC3	GND	GND
RowC4	DP01-RD3-	VPX_10GBE_RX3_N
RowC5	GND	GND
RowC6	DP02-RD1-	N/C
RowC7	GND	GND
RowC8	DP02-RD3-	N/C
RowC9	GND	GND
RowC10	UD	UC_UART_RX_N
RowC11	GND	GND
RowC12	UD	P1_SPARE2_IN_N
RowC13	GND	GND
RowC14	CPTp02-DC-	N/C
RowC15	GND	GND
RowC16	CPTp01-DC-	VPX_1GBE_TX2_N
RowB1_Even	GND-J1	N/C
RowB2_Even	DP01-RD1+	VPX_10GBE_RX1_P
RowB3_Even	GND-J1	N/C
RowB4_Even	DP01-RD3+	VPX_10GBE_RX3_P
RowB5_Even	GND-J1	N/C
RowB6_Even	DP02-RD1+	N/C
RowB7_Even	GND-J1	N/C
RowB8_Even	DP02-RD3+	N/C
RowB9_Even	GND-J1	N/C
RowB10_Even	UD	UC_UART_RX_P
RowB11_Even	GND-J1	N/C
RowB12_Even	UD	P1_SPARE2_IN_P
RowB13_Even	GND-J4	N/C
RowB14_Even	CPTp02-DC+	N/C
RowB15_Even	GND-J4	N/C
RowB16_Even	CPTp01-DC+	VPX_1GBE_TX2_P

P1 Connector Pin Number	P1 Connector Name	SimpliStor Signal Connection
RowB1_Odd	DP01-RD0-	VPX_10GBE_RX0_N
RowB2_Odd	GND-J1	N/C
RowB3_Odd	DP01-RD2-	VPX_10GBE_RX2_N
RowB4_Odd	GND-J1	N/C
RowB5_Odd	DP02-RD0-	N/C
RowB6_Odd	GND-J1	N/C
RowB7_Odd	DP02-RD2-	N/C
RowB8_Odd	GND-J1	N/C
RowB9_Odd	UD	VERSAL_UART_RX_N
RowB10_Odd	GND-J1	N/C
RowB11_Odd	UD	P1_SPARE1_IN_N
RowB12_Odd	GND-J1	N/C
RowB13_Odd	CPTp02-DA-	N/C
RowB14_Odd	GND-J4	N/C
RowB15_Odd	CPTp01-DA-	VPX_1GBE_TX1_N
RowB16_Odd	GND-J4	N/C
RowA1	DP01-RD0+	VPX_10GBE_RX0_P
RowA2	GND	GND
RowA3	DP01-RD2+	VPX_10GBE_RX2_P
RowA4	GND	GND
RowA5	DP02-RD0+	N/C
RowA6	GND	GND
RowA7	DP02-RD2+	N/C
RowA8	GND	GND
RowA9	UD	VERSAL_UART_RX_P
RowA10	GND	GND
RowA11	UD	P1_SPARE1_IN_P
RowA12	GND	GND
RowA13	CPTp02-DA+	N/C
RowA14	GND	GND
RowA15	CPTp01-DA+	VPX_1GBE_TX1_P
RowA16	GND	GND

P2 Backplane Connector Signal/Pin Mapping

Connector Manufacturer: TE Connectivity (Option for Smiths Interconnect)

Manufacturer Part Number: 2102771-4 (Optional Smiths KVPX+ YGP064-001P)

Mates with Backplane Connector Part Number: TE Connectivity TBS (Smiths KVPX+ YGS064-004ANH)

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Backplane J2		Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	Expansion Plane X16 using [15:0]	UD	GND	GND-J2	EP00-TD-	EP00-TD+	GND	GND-J2	EP00-RD-	EP00-RD+
2		GND	EP01-TD-	EP01-TD+	GND-J2	GND	EP01-RD-	EP01-RD+	GND-J2	GND
3		UD	GND	GND-J2	EP02-TD-	EP02-TD+	GND	GND-J2	EP02-RD-	EP02-RD+
4		GND	EP03-TD-	EP03-TD+	GND-J2	GND	EP03-RD-	EP03-RD+	GND-J2	GND
5		UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6		GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7		UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8		GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10		GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11		UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12		GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13		UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14		GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15		UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16		GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

Figure 4. SimpliStor Module P2 Connector Pinout

The P2 Expansion Plane (Figure 4) is implemented as a x4 PCI Express 3.0 interface. The link is routed to the EP00 to EP03 lanes on the backplane. The VE2302 FPGA supports Gen 4 PCIe speeds and PCB is routed to support these speeds. However, the VITA 78.0 connectors are not rated to operate at the 16Gb/s speeds necessary for Gen 4 PCIe interfaces.

Table 3. SimpliStor P2 Signal Connections

P1 Connector Pin Location	P1 Connector Name	SimpliStor Signal Connection
RowG1	UD	N/C
RowG2	GND	GND
RowG3	UD	N/C
RowG4	GND	GND
RowG5	UD	N/C
RowG6	GND	GND

P1 Connector Pin Location	P1 Connector Name	SimpliStor Signal Connection
RowG7	UD	N/C
RowG8	GND	GND
RowG9	UD	N/C
RowG10	GND	GND
RowG11	UD	N/C
RowG12	GND	GND
RowG13	UD	N/C
RowG14	GND	GND
RowG15	UD	N/C
RowG16	GND	GND
RowF1	GND	GND
RowF2	EP01-TD-	VPX_PCIE_TX1_N
RowF3	GND	GND
RowF4	EP03-TD-	VPX_PCIE_TX3_N
RowF5	GND	GND
RowF6	EP05-TD-	N/C
RowF7	GND	GND
RowF8	EP07-TD-	N/C
RowF9	GND	GND
RowF10	EP09-TD-	N/C
RowF11	GND	GND
RowF12	EP11-TD-	N/C
RowF13	GND	GND
RowF14	EP13-TD-	N/C
RowF15	GND	GND
RowF16	EP15-TD-	N/C
RowE1_Even	GND-J2	N/C
RowE2_Even	EP01-TD+	VPX_PCIE_TX1_P
RowE3_Even	GND-J2	N/C
RowE4_Even	EP03-TD+	VPX_PCIE_TX3_P
RowE5_Even	GND-J2	N/C
RowE6_Even	EP05-TD+	N/C
RowE7_Even	GND-J2	N/C
RowE8_Even	EP07-TD+	N/C
RowE9_Even	GND-J2	N/C
RowE10_Even	EP09-TD+	N/C
RowE11_Even	GND-J2	N/C
RowE12_Even	EP11-TD+	N/C

P1 Connector Pin Location	P1 Connector Name	SimpliStor Signal Connection
RowE13_Even	GND-J2	N/C
RowE14_Even	EP13-TD+	N/C
RowE15_Even	GND-J2	N/C
RowE16_Even	EP15-TD+	N/C
RowE1_Odd	EP00-TD-	VPX_PCIE_TX0_N
RowE2_Odd	GND-J2	N/C
RowE3_Odd	EP02-TD-	VPX_PCIE_TX2_N
RowE4_Odd	GND-J2	N/C
RowE5_Odd	EP04-TD-	N/C
RowE6_Odd	GND-J2	N/C
RowE7_Odd	EP06-TD-	N/C
RowE8_Odd	GND-J2	N/C
RowE9_Odd	EP08-TD-	N/C
RowE10_Odd	GND-J2	N/C
RowE11_Odd	EP10-TD-	N/C
RowE12_Odd	GND-J2	N/C
RowE13_Odd	EP12-TD-	N/C
RowE14_Odd	GND-J2	N/C
RowE15_Odd	EP14-TD-	N/C
RowE16_Odd	GND-J2	N/C
RowD1	EP00-TD+	VPX_PCIE_TX0_P
RowD2	GND	GND
RowD3	EP02-TD+	VPX_PCIE_TX2_P
RowD4	GND	GND
RowD5	EP04-TD+	N/C
RowD6	GND	GND
RowD7	EP06-TD+	N/C
RowD8	GND	GND
RowD9	EP08-TD+	N/C
RowD10	GND	GND
RowD11	EP10-TD+	N/C
RowD12	GND	GND
RowD13	EP12-TD+	N/C
RowD14	GND	GND
RowD15	EP14-TD+	N/C
RowD16	GND	GND
RowC1	GND	GND
RowC2	EP01-RD-	VPX_PCIE_RX1_N

P1 Connector Pin Location	P1 Connector Name	SimpliStor Signal Connection
RowC3	GND	GND
RowC4	EP03-RD-	VPX_PCIE_RX3_N
RowC5	GND	GND
RowC6	EP05-RD-	N/C
RowC7	GND	GND
RowC8	EP07-RD-	N/C
RowC9	GND	GND
RowC10	EP09-RD-	N/C
RowC11	GND	GND
RowC12	EP11-RD-	N/C
RowC13	GND	GND
RowC14	EP13-RD-	N/C
RowC15	GND	GND
RowC16	EP15-RD-	N/C
RowB1_Even	GND-J2	N/C
RowB2_Even	EP01-RD+	VPX_PCIE_RX1_P
RowB3_Even	GND-J2	N/C
RowB4_Even	EP03-RD+	VPX_PCIE_RX3_P
RowB5_Even	GND-J2	N/C
RowB6_Even	EP05-RD+	N/C
RowB7_Even	GND-J2	N/C
RowB8_Even	EP07-RD+	N/C
RowB9_Even	GND-J2	N/C
RowB10_Even	EP09-RD+	N/C
RowB11_Even	GND-J2	N/C
RowB12_Even	EP11-RD+	N/C
RowB13_Even	GND-J2	N/C
RowB14_Even	EP13-RD+	N/C
RowB15_Even	GND-J2	N/C
RowB16_Even	EP15-RD+	N/C
RowB1_Odd	EP00-RD-	VPX_PCIE_RX0_N
RowB2_Odd	GND-J2	N/C
RowB3_Odd	EP02-RD-	VPX_PCIE_RX2_N
RowB4_Odd	GND-J2	N/C
RowB5_Odd	EP04-RD-	N/C
RowB6_Odd	GND-J2	N/C
RowB7_Odd	EP06-RD-	N/C
RowB8_Odd	GND-J2	N/C

P1 Connector Pin Location	P1 Connector Name	SimpliStor Signal Connection
RowB9_Odd	EP08-RD-	N/C
RowB10_Odd	GND-J2	N/C
RowB11_Odd	EP10-RD-	N/C
RowB12_Odd	GND-J2	N/C
RowB13_Odd	EP12-RD-	N/C
RowB14_Odd	GND-J2	N/C
RowB15_Odd	EP14-RD-	N/C
RowB16_Odd	GND-J2	N/C
RowA1	EP00-RD+	VPX_PCIE_RX0_P
RowA2	GND	GND
RowA3	EP02-RD+	VPX_PCIE_RX2_P
RowA4	GND	GND
RowA5	EP04-RD+	N/C
RowA6	GND	GND
RowA7	EP06-RD+	N/C
RowA8	GND	GND
RowA9	EP08-RD+	N/C
RowA10	GND	GND
RowA11	EP10-RD+	N/C
RowA12	GND	GND
RowA13	EP12-RD+	N/C
RowA14	GND	GND
RowA15	EP14-RD+	N/C
RowA16	GND	GND

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input		TBS	Vdc
3.3V_AUX (Optional)	3.3V Auxiliary Input		TBS	Vdc
Storage Temp		-40	+125	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Power Dissipation			35	W
Mass			0.65	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
TID		>30k	rad (Si)
nd-SEL Immunity		≤37	MeV-cm ² /mg
Rate of SEE Recovery with External Intervention	LEO ISS Orbit LEO 1000 km / 81° Orbit MEO 10,000 km /81° Orbit GEO	TBS TBS TBS TBS	Per day

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@ 50°C / Max Vin / 100% Operation	TBS	hours
Reliability (R) ^(Note 1)	3 years / 50°C / Max Vin / 100% Operation 5 years / 50°C / Max Vin / 100% Operation 7 years / 50°C / Max Vin / 100% Operation	TBS	
Acceptance Testing (FM3 Class C and FM4 Class D)			
Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	
Qualification Testing			
Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles

Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Operational Specifications

Recommended Operating Conditions

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX (Optional)	3.3V Auxiliary Input	3	3.6	Vdc
Operating Temp	Referenced to wedge lock	-10	+50	°C

Power Dissipation

Parameter	Description/Comments	Min	Max	Units
Recording Power	10Gbps Ethernet		TBS	W
Playback Power	10Gbps Ethernet		TBS	W
Recording Power	PCIe Gen 3 (Future Opt'n)		N/A	W
Playback Power	PCIe Gen 3 (Future Opt'n)		TBS	W
Static Power	No Data Transactions		7	W

Control Plane - 1000Base-T Ethernet (IEEE 802.3ab)

Parameter	Description/Comments	Min	Max	Units
Signal Type	PAM-5			
Symbol Rate			1.25	Gbaud
Differential Output Voltage Level		-1	+1	V
VCM	Common Mode Voltage	-0.75	+0.75	V
Return Loss	TX & RX from 1MHz to 100MHz		16	dB
Insertion Loss	At 100MHz		24	dB
Differential Impedance		85	115	Ohms
Isolation Voltage		1500		Vrms

Data Plane - 10GBase-KR (USXGMII / IEEE 802.3ap Clause 72 & 73)

Parameter	Description/Comments	Min	Max	Units
Signaling Type	NRZ (PAM-2), differential			
Symbol Rate			10.3125	Gbaud
Coding	64b/66b			
Differential Voltage		600	1200	mVpp
Differential Impedance		90	110	Ohms
VCM	Common Mode Voltage		700	mV
Return Loss	4MHz to 12GHz		12	dB
Insertion Loss	At 5GHz		28	dB
Total Tx Jitter			0.28	UI
AC Coupling			100	nF

Expansion Plane – PCIe Gen 3

Parameter	Description/Comments	Min	Max	Units
Signaling Type	NRZ (PAM-2), differential			
Symbol Rate	Per Lane Rate		8	GT/s
Coding	128b/130b			
Differential Voltage		600	1200	mVpp
Differential Impedance		72.25	97.75	Ohms
VCM	Common Mode Voltage		700	mV
Return Loss	At 4GHz		10	dB
Insertion Loss	At 4GHz		28	dB
Skew	Between Lanes		20	ns
Total Tx Jitter			0.3	UI
AC Coupling			100	nF

Functional Description

To Be Added

Mechanical Drawing

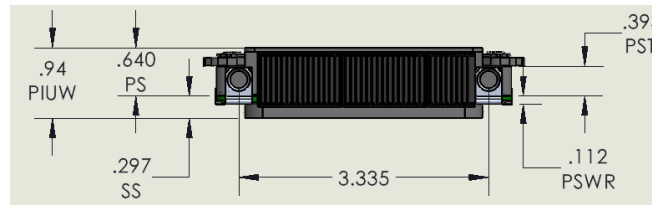
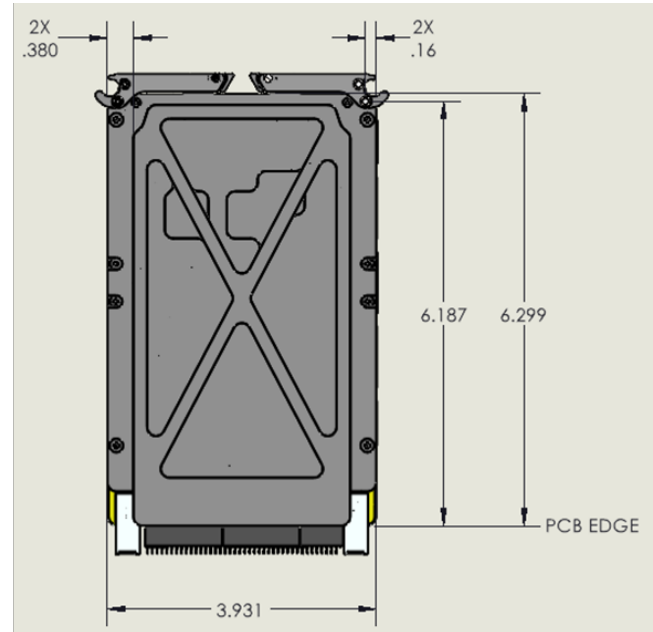
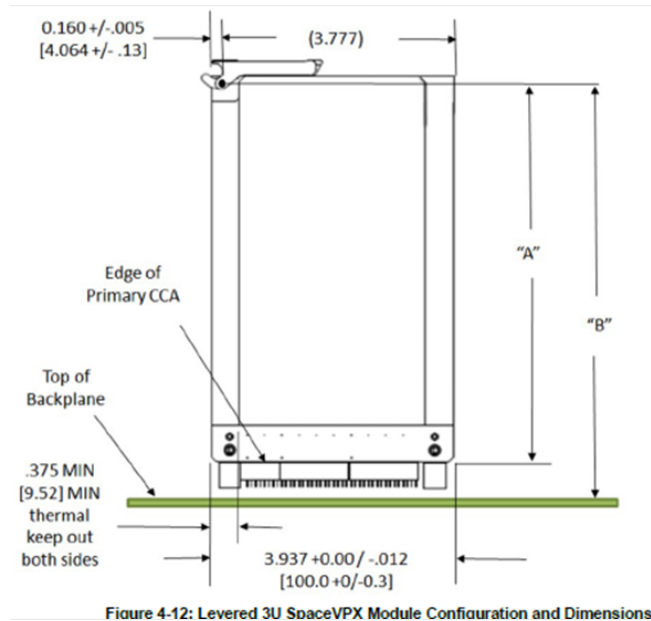


Table 4.5.1-3: SpaceVPX Variable Table for Plug-In Units – Secondary Side Retainer

Variable	0.80-inch Pitch	1.00-inch Pitch	1.20-inch Pitch	1.40-inch Pitch	1.60-inch Pitch - A
PSTI: 3U primary side of PCB to thermal interface	0.393 ± 0.005 [9.98 ± 0.13]	0.393 ± 0.005 [9.98 ± 0.13]	0.393 ± 0.005 [9.98 ± 0.13]	0.393 ± 0.005 [9.98 ± 0.13]	0.393 ± 0.005 [9.98 ± 0.13]
PSTI: 6U primary side of PCB to thermal interface	0.513 ± 0.005 [13.03 ± 0.13]	0.513 ± 0.005 [13.03 ± 0.13]	0.513 ± 0.005 [13.03 ± 0.13]	0.513 ± 0.005 [13.03 ± 0.13]	0.513 ± 0.005 [13.03 ± 0.13]
PSRW: 3U primary side of PCB to outer edge of relaxed retainer	0.102 ± 0.010 [2.59 ± 0.25]	0.102 ± 0.010 [2.59 ± 0.25]	0.102 ± 0.010 [2.59 ± 0.25]	0.102 ± 0.010 [2.59 ± 0.25]	0.102 ± 0.010 [2.59 ± 0.25]
PSRW: 6U primary side of PCB to outer edge of relaxed retainer	0.092 ± 0.010 [2.34 ± 0.25]	0.092 ± 0.010 [2.34 ± 0.25]	0.092 ± 0.010 [2.34 ± 0.25]	0.092 ± 0.010 [2.34 ± 0.25]	0.092 ± 0.010 [2.34 ± 0.25]
PIUW: plug-in unit width	0.760 MAX [19.30 MAX]	0.960 MAX [24.38 MAX]	1.160 MAX [29.46 MAX]	1.360 MAX [34.54 MAX]	1.560 MAX [39.62 MAX]
PS: primary side of PCB to front of plug-in unit	0.570 MAX [14.48 MAX]	0.650 MAX [16.51 MAX]	0.650 MAX [16.51 MAX]	0.800 MAX [20.32 MAX]	1.000 MAX [25.4 MAX]
SS: primary side of PCB to back of plug-in unit	0.190 MAX [4.83 MAX]	0.310 MAX [7.87 MAX]	0.510 MAX [12.95 MAX]	0.560 MAX [14.22 MAX]	0.560 MAX [14.22 MAX]

Revision History

Date	Rev	Author	Change Description	Page #
08/06/25	1.0	TLM	Initial DRAFT	All
08/06/25	1.1	TLM	Edits made from CDR • Removed NAND Power Switching from Block Diagram	4
10/30/25	1.2	TLM	Updated ordering information and block diagram	3 & 4
11/30/2025`	2.0	TLM	Up-leveled document to Preliminary level. Adjusted orderable PN to reflect official PNs. Added DWPD features Updated Acceptance Test criteria for flight modules Updated Mechanical Dimensions	All, 3 3 7 12
12/11/2025	2.1	TLM	Added Backplane eICD Connection Tables and added TE Connectivity as default connector; making Smiths as alternative option	5-16
3/13/2025	2.2	DPA	Updated Operational Temperature and added FM4 ordering information	All
3/30/3036	2.3	TLM	Updated Radiation Performance and Reliability & Quality tables	17

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
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