AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

FRONTGRADE

PRODUCT INFORMATION NOTICE

1. TITLE UT8ER1/2/4M32 32-128Mb SRAM Internal EDAC Operation Clarification		**2. DOCUMENT NUMBER** SPO-2025-PIN-0002	
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4. MANUFACTURER NAME AND ADDRESS FRONTGRADE TECHNOLOGIES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486		**5. MANUFACTURER POINT OF CONTACT NAME** Mike Leslie	
		6. MANUFACTURER POINT OF CONTACT TELEPHONE 719-594-8148	
		7. MANUFACTURER POINT OF CONTACT EMAIL mike.leslie@frontgrade.com	
8. CAGE CODE 65342	**9. BLANK**	**10. PRODUCT IDENTIFICATION CODE** QS09-12, QS16,17	**11. BASE PART** UT81/2/4ERM32
12. BLANK		**13. SMD NUMBER** 5962-10202,10203, 10204	**14. DEVICE TYPE DESIGNATOR** all
		15. RHA LEVELS all	**16. QML LEVEL** all
		17. NON QML LEVEL all	**18. GIDEP NUMBER** **GB4-PC-2025-0002**

It has come to the attention of Frontgrade that a statement in the manufacturer's datasheet may lead to a misunderstanding of the internal EDAC correction of data and memory. Therefore, the below statement has been revised to clarify that core memory errors are only rewritten during internal scrub cycles, and it is important to perform periodic scrubbing to prevent the accumulation of errors.

In the current datasheet "UT8ER1M32, UT8ER2M32, UT8ER4M32 32, 64, 128 Megabit SRAM MCM" version 1.0.0 dated 7/1/2021, page 12

Data is not only corrected during the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after t_{AVAV} is satisfied, the MBE signal will be asserted. (Note: Reading un-initialized memory locations may result in un-intended MBE assertions.)

Newly released datasheet "UT8ER1M32, UT8ER2M32, UT8ER4M32 32, 64, 128 Megabit SRAM MCM" version 1.0.0 dated 7/1/2021, page 14

The EDAC circuitry corrects single bit errors during read cycles for the purposes of presenting correct data to the DQ[31:0] data bus pins. If a double bit error is encounter, no correction is performed, and the MBE will assert after t_{AVAV} or t_{ETQV} are satisfied. While single bit errors are corrected during read cycles to the DQ[31:0] output pins, the corrected data is not rewritten to the core memory. Single bit errors (bit upsets) in the core memory are only corrected (rewritten) during internal scrub cycles. The address location of the scrub cycle is controlled by an internal address counter which is reset to 0x00000h at power up. The address counter increments sequentially for each subsequent scrub cycle. The scrub address counter has no correlation to previous read cycles or what may be present on the address pins when a scrub cycle initiates. If a double bit error is encountered during any scrub cycle, no correction or MBE flag will be asserted until that uncorrectable location is encountered during a read cycle. For this reason, it is important to perform periodic scrub cycles to avoid the accumulation of upsets to the core memory. (Note: Reading un-initialized memory locations may result in un-intended MBE assertions).

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