FRONTGRADE

ADV DATASHEET

SBC2A72-SVPX

Dual-Core ARM Cortex-A72 with GPU SpaceVPX Single Board Computer

3/12/2026

Version #: 1.3

Introduction

The Frontgrade™ SBC2A72-SVPX Single Board Computer provides a compelling mix of high-performance processing and interface capability, in low power SWaP optimized design. Implemented a 3U-160mm SpaceVPX form factor, the SBC is ideal for on-board computing, payload computing, and graphics processing applications. This compact 3U design is small, lightweight, and power efficient while offering a strong combination of compute and graphics processing performance along with a strong mix of interfaces.

The Frontgrade SBC2A72-SVPX features the power efficient and radiation tolerant Vorago VA7230 Dual ARM® Cortex®-A72 processor with integrated Graphics Processing Unit (GPU) capable of 10.4 GFLOPs performance that is ideal for image processing and AI acceleration. Adding to the processing capabilities of the VA7230, the SBC provides a strong complement of communications and interface protocols to support high-throughput networking, graphics, command, control, and telemetry in conjunction with extensive memory facilities.

Moreover, to address the wide mix of I/O interfaces required by different applications, the SBC2A72-SVPX integrates a companion CertusPro-NX-RT FPGA and XMC+ I/O expansion mezzanine interface. Leveraging the local FPGA and XMC+ interface, applications can implement additional I/O solutions optimized for their unique requirements without customizing the main SBC hardware. The FPGA currently implements a PCIe to SpaceFibre interface.

Finally, the SBC2A72-SVPX includes a radiation hardened MCU (VA41630, ARM Cortex-M4) which provides, among other things, system management between plug-in modules integrated into a larger system as well as local monitoring and power management to elements local to the SBC. Additionally, the MCU expands the interfaces to the system backplane in the form of UARTs, SpaceWire, and GPIO.

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
SBC2A72-SVPX-OP-EDU	E = EDU/EM (Room Temp only)	Lab / Development Use Cases
SBC2A72-SVPX-OP-FM4	COTS Parts Grade (-25°C to +65°C)	Target Mission Class D
SBC2A72-SVPX-OP-FM3	Level 3 Parts Grade (-25°C to +65°C)	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds.

Features

Processing Performance

- Based on Vorago VA7230 Processor (NXP LS1028A) with GPU Acceleration
  - — Two 32/64-bit ARM® Cortex®-A72 cores with the following capabilities:
    - ~15K DMIPS performance at1.5 GHz operation
    - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache
    - Single cluster of two cores sharing 1MB L2 cache
  - — Graphics processing unit
    - Supports Geometry rate 100 Mtri/sec
    - Pixel rate 650 Mpixel/sec
    - 10.4 GFLOPS (32-bit high precision)
    - Supports OpenGL ES 3.0, 2.0, 1.1
    - Supports OpenCL 1.1, 1.2

User Memory

- 8GB + ECC DDR4 (x36 bus width)
  - — 1600 MT/s
- Apps and Storage
  - — 32GB e.MMC 5.1
    - Supports enhanced secure digital host controller (eSHDC)
  - — Optional: 1Gb-8Gb DQSPI MRAM

Mass & Thermal

- Mass: <0.65 kg
- 3U Form Factor: 160mm x 100mm / 1.0” Pitch
- -25°C to +65°C operational case temperature
- Power consumption: <15W Typical / 30W Max
- TID: 30-50krad (Si)
- SEL Immune <= 37MeV

Debug Interfaces

- MCU JTAG, Debug UART, Reset and 2 GPIO
- CPU JTAG, Debug UART, Reset and 2 GPIO
- FPGA JTAG, Debug UART, Programming, and LEDs
- CPU Debug Reset

Security Features

- Secure boot
- Security Engine
- Arm TrustZone™

Backplane Interfaces

(VITA 78.0 Profile: SLT3-PAY-2F2T1Q-14.2.1)

- — 4x GbE ports
  - 2x TSN 1GbE (SGMII)
  - 2x 1000Base-X (with magnetics)
- — 1x PCIe 3.0 x1 port
- — 1x USB 3.0 Interface
- — 1x DisplayPort Out
  - DisplayPort 1.3 and eDP 1.4
- — 6x GPIO + 2x GPIO/I2C, from CPU
- — 4x GPIO, from FPGA
- — 1x PPS Input
- 1x UART
- 1x SpW

Backplane Utility Segment

- 5x GA + 1x GA Parity
- SYSRESET*
- 1x I2C + SM_STAT* & SM_RESET*
- 1x LVDS REFCLK Input (100MHz)
- 1x LVDS AUXCLK, PPS
- 12V VS1
- 3.3V_AUX

Software

The SBC2A72-SVPX is supported by a SDK/BSP which offers Linux based off the NXP LS1028A layerscape distribution, NXP Layerscape Software.

The NXP Middleware and additional 3rd Party Solutions are available. Please contact your local Frontgrade sales representative for additional information.

Block Diagram

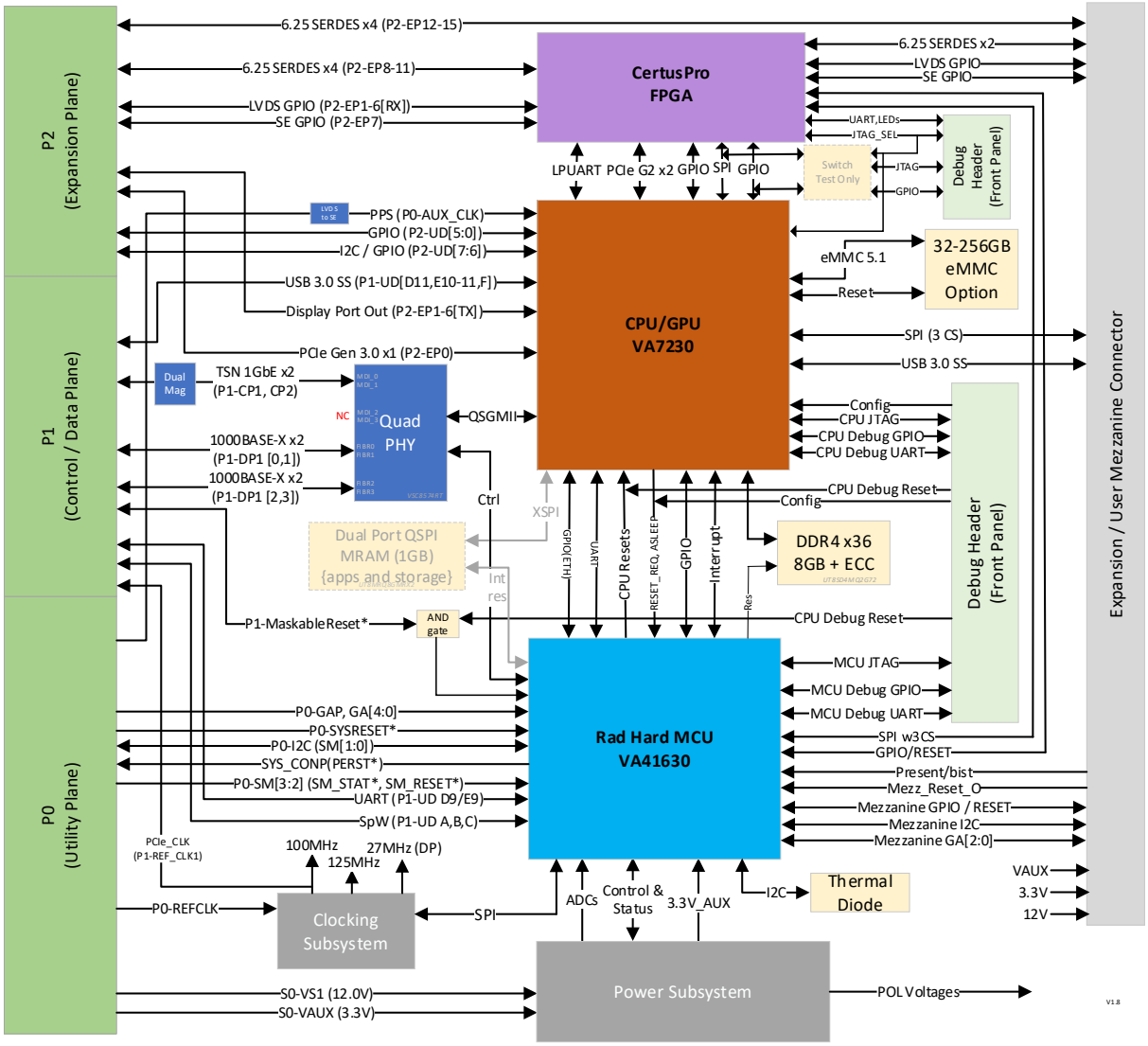

Figure 1. SBC2A72-SVPX High Level Block Diagram

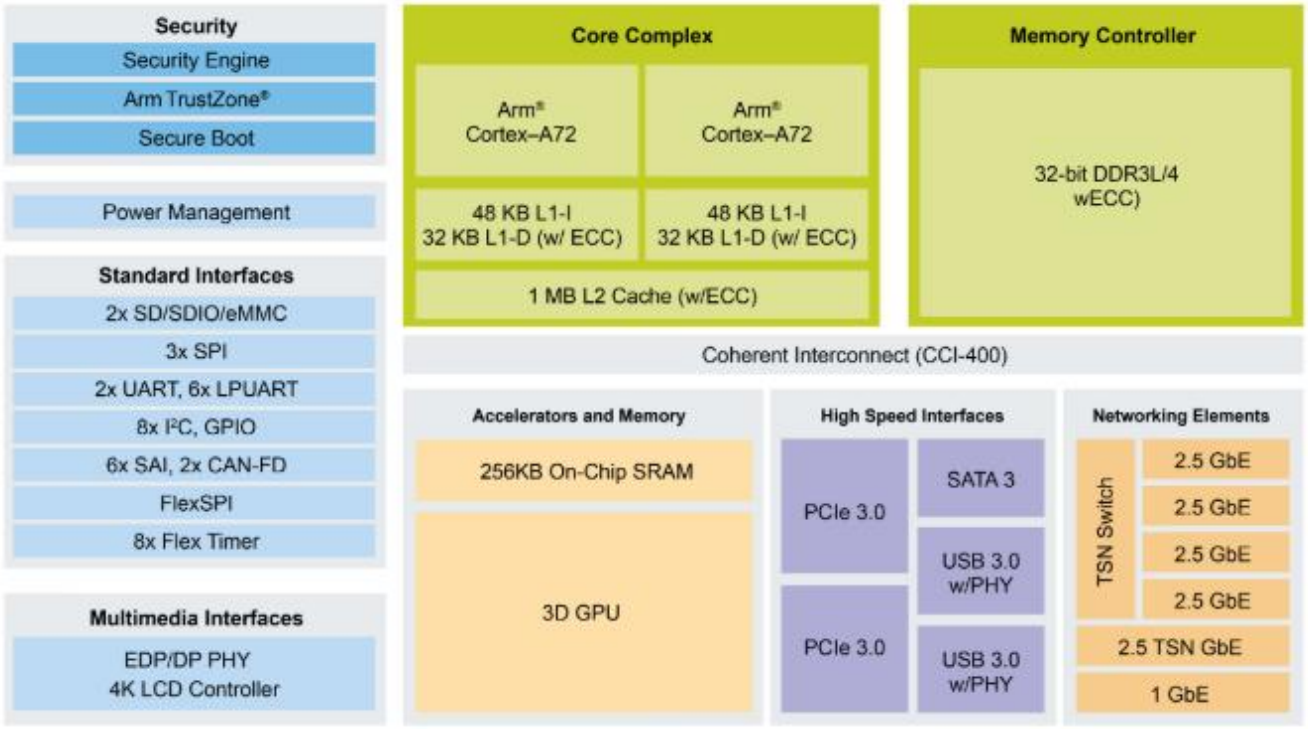

Figure 2. VA7230 Processor High Level Block Diagram

Debug Connector Interfaces

The SBC2A72-SPVX provides a two Debug Interfaces to the front side of the plug-in module. The main debug interface is for the VA7230 CPU and VA41630 MCU.

The other Debug Interface is for the CertusPro FPGA which is described in table 2.

The debug interfaces are only intended for ground/lab level testing and pre-flight configuration of the SBC software.

J1: 40-pin Front Panel Debug Connector

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	MCU_JTAG_TRSTN	2	SE Input	CPU_JTAG_TRSTN
3	SE Input	MCU_JTAG_TCK	4	SE Input	CPU_JTAG_TCK
5	SE Input	MCU_JTAG_TMS	6	SE Input	CPU_JTAG_TMS
7	SE Input	MCU_JTAG_TDI	8	SE Input	CPU_JTAG_TDI
9	SE Output	MCU_JTAG_TDO	10	SE Output	CPU_JTAG_TDO
11	PWR	GND	12	PWR	GND
13	SE Input	MCU_RESET	14	SE Input	CPU_RESET
15	SE Input	MCU_UART_RX	16	SE Input	CPU_UART_RX
17	SE Input	MCU_UART_TX	18	SE Input	CPU_UART_TX
19	SE Input	MCU_GPIO_LED0	20	SE Input	CPU_GPIO_LED0
21	SE Output	MCU_GPIO_LED1	22	SE Output	CPU_GPIO_LED1
23	PWR	GND	24	PWR	GND
25	SE In/Out	SDHC2_DAT0	26	SE In/Out	SDHC2_DAT2
27	SE In/Out	SDHC2_DAT1	28	SE In/Out	SDHC2_DAT3
29	SE Input	SDHC2_CMD	30	SE Input	MCU_CPU_ASLEEP
31	SE Input	SDHC2_CLK	32	SE Input	MCU_CPU_UART_RX
33	PWR	GND	34	PWR	GND
35	NC	NC	36	SE Output	CPU_CLK_OUT
37	PWR	1.8V	38	SE Output	CPU_TA_PROG
39	PWR	GND	40		GND

Table 1. J1 Debug Connector Pin list

J2: 20-pin Front Panel Debug Connector

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	FPGA_JTAG_TCK	2	SE Input	FPGA_RESET
3	SE Input	FPGA_JTAG_TMS	4	SE Input	FPGA_UART_RX
5	SE Input	FPGA_JTAG_TDI	6	SE Output	FPGA_UART_TX
7	SE Output	FPGA_JTAG_TDO	8	SE Input	JTAG_SELECT
9	PWR	GND	10	PWR	GND
11	PWR	1.8V	12	PWR	1.8V
13	SE Input	FPGA_PROG	14	SE Output	FPGA_LED0
15	SE Input	FPGA_INT	14	SE Output	FPGA_LED1
17	SE Input	FPGA_DONE	14	NC	NC
19	PWR	GND	14	PWR	GND

Table 2. J2 FPGA Debug Connector Pin list

Backplane Slot Profile and Connection Tables

The SBC2A72-SVPX is a 3U VPX card that measures 100 mm x 160mm and is based off the VITA 78.0 standard. The backplane interface is based on the VITA 78.0 Payload Slot Profile: SLT3-PAY-2F2T1Q-14.2.1.

For reference, the slot profile for VITA 78.0 is shown below.

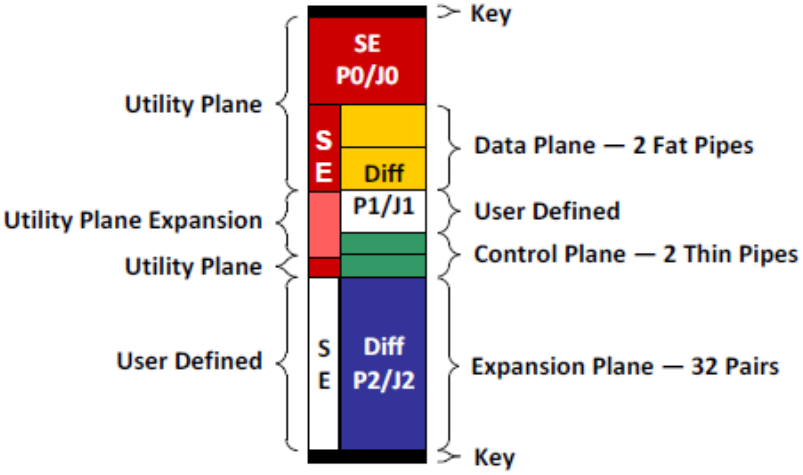

Figure 4. Backplane Slot Profile, SLT3-PAY-2F2T1Q-14.2.1

The table below provides a brief description of each one of the different plans defined in the SLT3-PAY-2F2T1Q-14.2.1 payload slot profile.

Plane	Description
Data Plane	High-speed payload and mission data transfer between processing modules.
Control Plane	Command, control, and health/status communications.
Utility Plane	Power distribution, timing, clocks, reset, discretes, housekeeping.
Expansion Plane	Local or optional I/O expansion between modules (e.g., co-processors or sensors).

Table 2. VITA 78.0 Plane Definitions

Backplane Slot Profile and Connection Tables

The SBC2A72-SVPX Single Board Computer is in a 3U, 160mm, SpaceVPX form factor with VITA 78.0 backplane profile SLT3-PAY-2F2T1Q-14.2.1. The P1 and P2 Connector Pinouts are depicted below.

P1 Backplane Connector Signal/Pin Mapping

Connector Manufacturer: Smiths Interconnect

Manufacturer Part Number: KVPX+ YGP064-001P

Mates with Backplane Connector Part Number: KVPX+ YGS064-004ANH

Plug-In Module P1				Row G	Row F	Row E		Row D	Row C	Row B		Row A
						Even	Odd			Even	Odd	
Bplane J1				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Date Plane Port 1	x8	x4/2x2/4x1	SYS_CONP*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2				GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3				VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD1-	DP01-RD2+
4				GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2			SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6				GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7				REF_CLK1-	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8				GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined			REF_CLK1+	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11				REF_CLK2-	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane			REF_CLK2+	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14				GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15				Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16				GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

Table 1. SBC2A72-SVPX Module P1 Connector Pinout

The SpaceVPX Control Plane is implemented with a SpaceWire (SpW) and UART interface which is connected to the VA41630 Processor.

The Data Plane is implemented with 4 Gigabit Ethernet Ports which include 2x TSN 1GbE and 2x 1000Base-X interfaces.

P2 Backplane

Connector Signal/Pin Mapping

Connector Manufacturer: Smiths Interconnect

Manufacturer Part Number: KVPX+ YGP064-001P (Same as P1 Connector)

Mates with Backplane Connector Part Number: KVPX+ YGS064-004ANH

Plug-In Module P2				Row G	Row F	Row E		Row D	Row C	Row B		Row A
						Even	Odd			Even	Odd	
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Expansion Plane x16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-TD-	EP00-TD+	GND	GND-J2	EP00-RD-	EP00-RD+
2				GND	EP01-TD-	EP01-TD+	GND-J2	GND	EP01-RD-	EP01-RD+	GND-J2	GND
3				UD	GND	GND-J2	EP02-TD-	EP02-TD+	GND	GND-J2	EP02-RD-	EP02-RD+
4				GND	EP03-TD-	EP03-TD+	GND-J2	GND	EP03-RD-	EP03-RD+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using [15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using [15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

Table 4. SBC2A72-SVPX Module P2 Connector Pinout

The Expansion Plane contains the following I/O:

- VA7230 CPU
  - PCIe Gen 3.0 x 1
  - DisplayPort 1.3 and eDP 1.4
  - 8 SE GPIO
- CertusPro FGPA
  - 6.25 SERDES x 4
  - 6 LVDS GPIO pairs
  - 4 SE GPIO

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX	3.3V Auxiliary Input	3	3.6	Vdc
Storage Temp		-40	+125	°C
Operating Temp	Measured at wedge lock	-25	+65	°C
Mass			0.65 TBC	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID		>30k	rad (Si)
nd-SEL Immunity		37	MeV-cm^2/mg
d-SEL Immunity		60	MeV-cm^2/mg
Total Single Event Rate Requiring External or Ground Intervention	LEO ISS Orbit 420km / 51.6° LEO 1000 km / 81° MEO 8000 km / 85° GEO 35,786km / 0°	4.08e-04 2.28e-03 4.33e-03 6.31e-03	per year

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@ 55 C	@ 40 °C (TBC) @ 55 °C (TBC) @ 65 °C (TBC	hours
Operating Life	@ 65°C	3 Years (TBC) 5 Years (TBC) 7 Years (TBC) 12 Years (TBC)	years
Random Vibration	3 Axis 60Hz to 800 Hz	14.6	Grms
~~Shock (duration)~~	~~100G to 4000G (100Hz to 10kHz)~~	~~20~~	~~ms~~
Thermal Vac (?)	-25°C to +75°C	1-2	Cycles

Electrical Specifications

To Be Added

Functional Description

To Be Added

Software Ecosystem

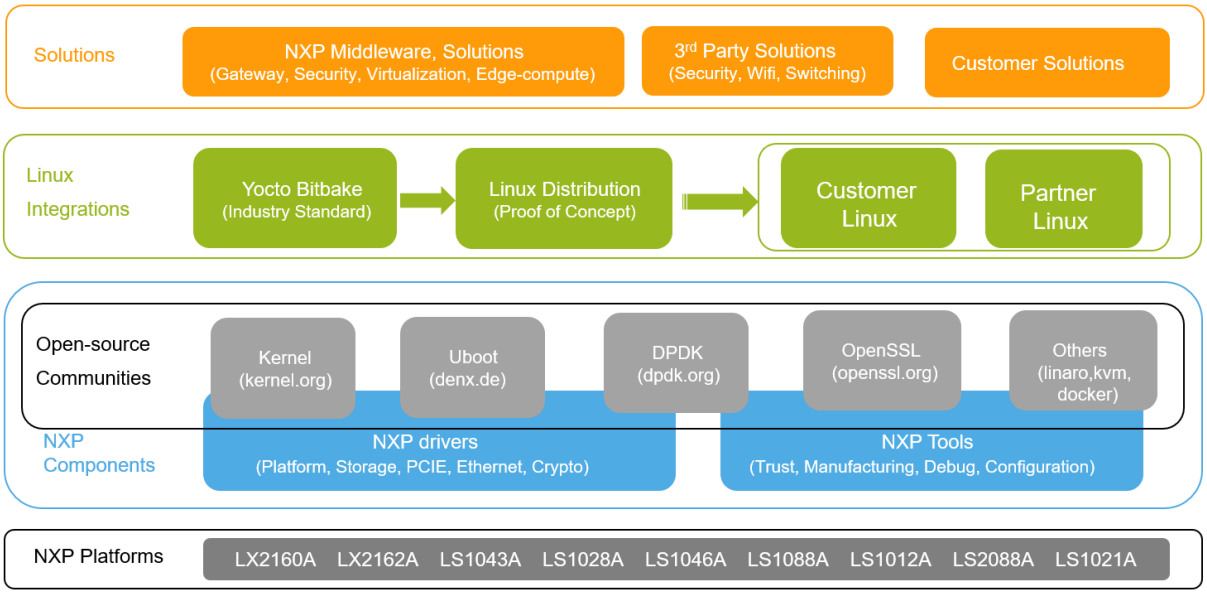

Figure 5. NXP Layerscape Software

Features

Layerscape LDP Components

- Freely available
  - Download from public repositories (e.g. github.com)
  - No need to download a large ISO and extract
- Modularized
  - Boot-loaders, Kernels, User-space libraries, Tools, Configuration
  - Pick and choose ones you need
- Clean layering, separation
  - Separate patches on top of open source
  - Patches identified by platform/IP
- Easy updates via Git
  - Periodic releases and interim updates
  - Support for two recent LTS kernels

Layerscape LDP

- Easy boot mechanisms
  - Boot from multiple sources
  - Simple, quick updates from any mass-storage
  - Brick-proof mechanism* - easy recovery via SD
- Easy runtime upgrades
  - Rich LDP user-land and repositories
  - On-the-fly install with apt-get
  - Build/install from source on target
- Latest and greatest
  - Latest Layerscape platforms
  - Latest drivers and features

- Layerscape specific tools, drivers

What's New In L6.1.1-1.0.0-LLDP

- NXP Layerscape LDP userland:
  - NXP Layerscape LDP, including Linux distro main packages and NXP packages
- Toolchain: gcc-11.2, glibc-2.36,binutils-2.38, gdb-12.1
- Linux kernel core and virtualization:
  - LTS kernel 6.1.1 update
- Linux kernel drivers:
  - Data Plane Development Kit (DPDK):
  - Virtualization - OVS-DPDK
- U-Boot bootloader:
  - U-Boot v2022.04 update
  - AQR113C on TWR-LS1021A, LS1088ARDB, and LX2162AQDS
- Other tools and utilities:
  - AQR113C firmware
  - Yocto bitbake

Mechanical Drawing

Placeholder (needs updated with latest information)

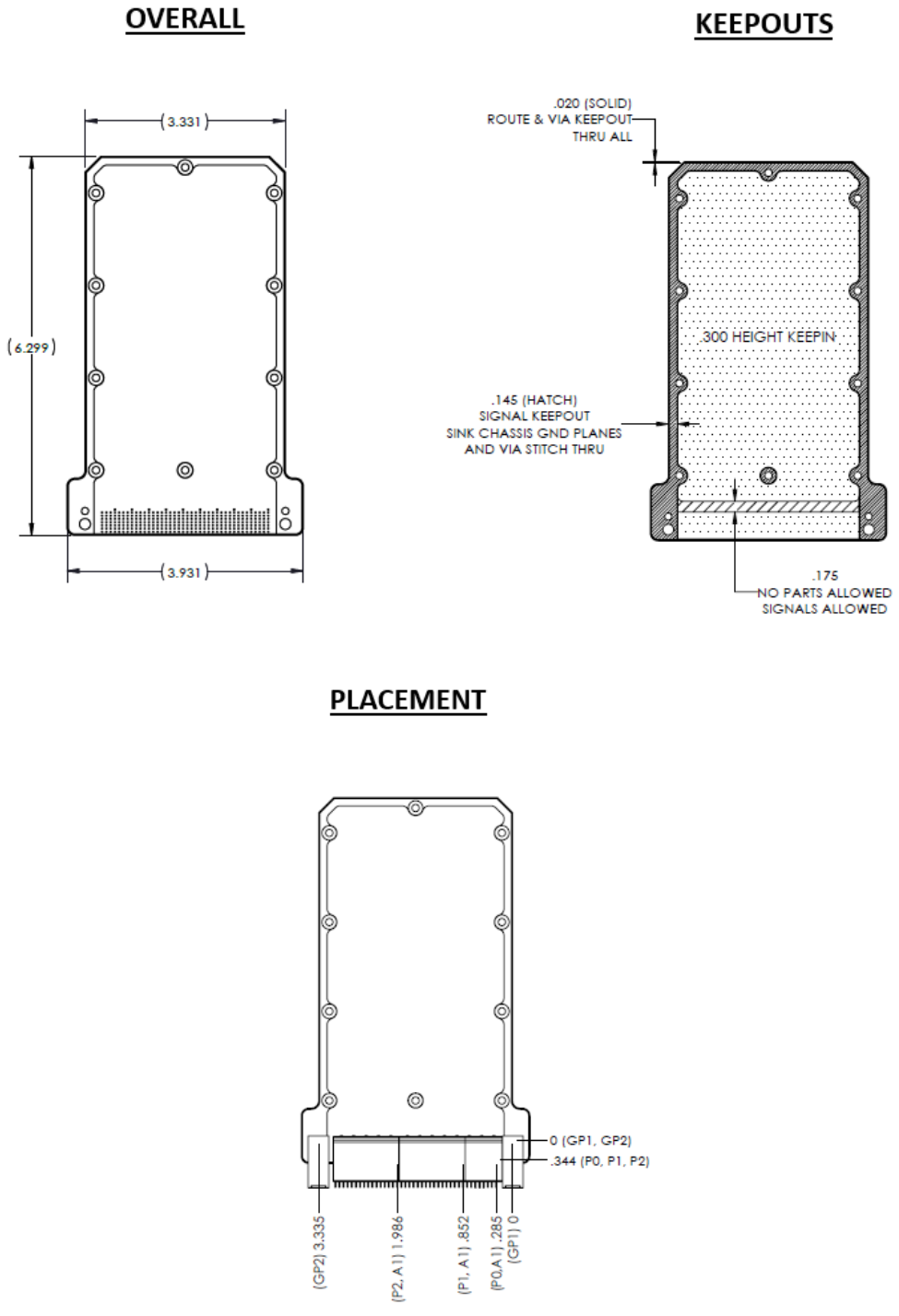

Figure 6. SBC2A72-SVPX Mechanical Information

Revision History

Date	Rev	Author	Change Description	Page #
06/10/25	1.0	TLM	Initial DRAFT	All
11/12/25	1.1	DPA	Revised DRAFT	All
12/04/25	1.2	TLM	Update ordering table and removed old ordering encoder	1, 18

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.