



FRONTGRADE

PRELIMINARY DATASHEET

SBC16A72-SVPX

Sixteen-Core ARM Cortex-A72
SpaceVPX Single Board Computer

6/1/2026
Version #: 1.0



Introduction

The **Frontgrade SBC16A72-SVPX** is a high-performance **3U SpaceVPX single board computer** designed to deliver scalable mission computing, secure networking, and deterministic I/O in size-, weight-, and power-constrained environments. Powered by the **NXP LX2160 processor**, the SBC16A72-SVPX provides a balanced combination of multicore compute performance, advanced security, and high-speed connectivity for space and defense applications.

At its core, the SBC16A72-SVPX integrates a **16-core Arm® Cortex-A72 processor operating up to 2.2 GHz**, enabling demanding workloads such as mission management, data handling, onboard networking, and edge analytics. The processor architecture supports software-defined payloads and distributed computing frameworks commonly deployed in modern SpaceVPX systems.

Security is a foundational design element of the SBC16A72-SVPX. The LX2160 incorporates a hardware **Security Engine**, **secure boot**, and **Arm TrustZone™**, providing a hardware-rooted chain of trust, cryptographic acceleration, and isolation between trusted and non-trusted execution environments. These features enable protection of mission software, secure command and telemetry processing, and resilience against cyber threats.

Based on **VITA 78.0 Profile SLT3-PAY-2F2T1Q-14.2.1**, the SBC16A72-SVPX offers extensive backplane connectivity. High-speed interfaces include **two 1000Base-T Ethernet ports**, up to **eight USXGMII or SGMII Ethernet lanes**, and **four PCIe Gen3 x4 ports** for high-bandwidth connections to payloads, accelerators, storage, and network fabrics. Additional interfaces include GPIO, I2C, RS-422 UART, SpaceWire, and a precision **PPS input** for time-synchronized systems. A fully featured utility plane supports system management, SpaceVPX addressing, clocks, resets, and smart in-board power management. Onboard memory includes **2x 16GB of ECC-protected DDR4 (72-bit) at 2400 MT/s** and **32 GB eMMC 5.1** for applications and storage, with optional configurations supporting **up to 1 GB of Dual-QSPI MRAM** for radiation-tolerant non-volatile memory.

The SBC16A72-SVPX is supported by the **NXP Layerscape Linux Distribution SDK**, providing a mature software ecosystem with BSPs, drivers, security tools, and integration with open-source frameworks such as U-Boot, Yocto/BitBake, and Linux middleware.

Key Applications

- Space-based mission and payload processing
- Secure command, telemetry, and networking gateways
- Distributed modular computing architectures
- Onboard data handling and edge analytics
- Software-defined spacecraft avionics
- Ethernet Switch Applications
- 5G NTN Regenerative On-Board Computing

Why it Matters

The **SBC16A72-SVPX** delivers **server-class multicore performance**, **hardware-rooted security**, and **rich high-speed I/O** in a **low-power, space-ready 3U SpaceVPX form factor**. It enables spacecraft designers to consolidate mission functions, increase onboard autonomy, and deploy secure, scalable computing architectures while meeting stringent SWaP and environmental constraints.

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
SBC16A72-SVPX-OP-EDU	EDU = EDU/EM (Room Temp only)	Lab / Development Use Cases
SBC16A72-SVPX-OP-FM4	COTS Parts Grade (-10°C to +50°C)	Target Mission Class D
SBC16A72-SVPX-OP-FM3	Level 3 Parts Grade (-10°C to +50°C)	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where optimal parts grades are not achievable/practical for standard hardware builds.

Features

Processing Performance

Based on NXP Layerscape® LX2160 Processor

- Sixteen (16) Arm Cortex®-A72 cores:
 - Up to 2.2 GHz
 - Single-threaded cores with 48KB L1 instruction cache and 32 KB L1 data cache
 - 8 MB L2 cache with ECC
 - Cache Coherent Interconnect Fabric up to 1.5 GHz
 - 8 MB Level 3 cache with ECC and On-Chip Memory Mode (OCM)

Security Features

- Security Engine
- Secure boot
- Arm TrustZone™

User Memory

- 2x 16GB + ECC DDR4 (x72 bus width)
 - 2400 MT/s
- Apps and Storage
 - 32GB e.MMC 5.1
 - Optional build with up to 1GB Dual-QSPI MRAM
- Supports enhanced secure digital host controller

Software Driven Power Saving Features

- CPU Idle/Sleep (Wait for Interrupt - WFI)
- CPU core hot plug
- Clock Gating
- Internal Power Gating
- Dynamic Frequency Scaling (DFS)
- Network Block Disable
- Peripheral Shutdown

Mass & Thermal

- Mass: <0.65 kg
- Form Factor: 160mm x 100mm / 1" Pitch
- -10°C to +50°C operational case temperature
- Power consumption: <20W Typical / 40W Max
- TID: Up to 30 krad (Si)
- nd-SEL Immune ≤ 37MeV

Backplane Interfaces

(VITA 78.0 Profile: SLT3-PAY-2F2T1Q-14.2.1)

- (CP1 & 2) 2x 1000Base-T Ethernet Ports
- (DP1 & 2) 8x USXGMII or SGMII Ethernet Ports
 - Four lanes capable of 40Gbase-KR4
- (P1 UD4:7) 2x I2C
- (P1 UD8:15) 1x SpW
- (EP0:7) 1x PCIe Gen 3 x8 (or 2x PCIe Gen 3 x4)
- (EP8:11) 1x PCIe Gen 3 x4
- (EP12:15) 1x PCIe Gen 3 x4
- (P2 UD) RS-422 UART

Backplane Utility Segment

- 5x GA + 1x GA Parity
- SYSRESET* & GDISCRETE
- 1x I2C + SM_STAT* & SM_RESET*
- 1x LVDS 100MHz Input (REFCLK)
- 1x LVDS 1PPS Input (AUX_CLK)
- 12V VS1
- 3.3V_AUX (Ordering Option)

Software

The SBC is supported by the NXP Layerscape Linux Distribution POC.

- <https://www.nxp.com/design/design-center/software/embedded-software/linux-software-and-development-tools/layerescape-linux-distribution-poc:LAYERSCAPE-SDK>

The Layerscape SDK includes a BSP and Drivers for the Layerscape appropriate for peripherals native to the processor along with toolsets including Trust, Manufacturing, Debug, and Configuration.

The SDK integrates into a software stack from Open-source Communities (e.g. Uboot) into Linux Integrations like Yocto Bitbake, and up through application support packages like NXP Middleware and 3rd Party Solutions.

Block Diagram

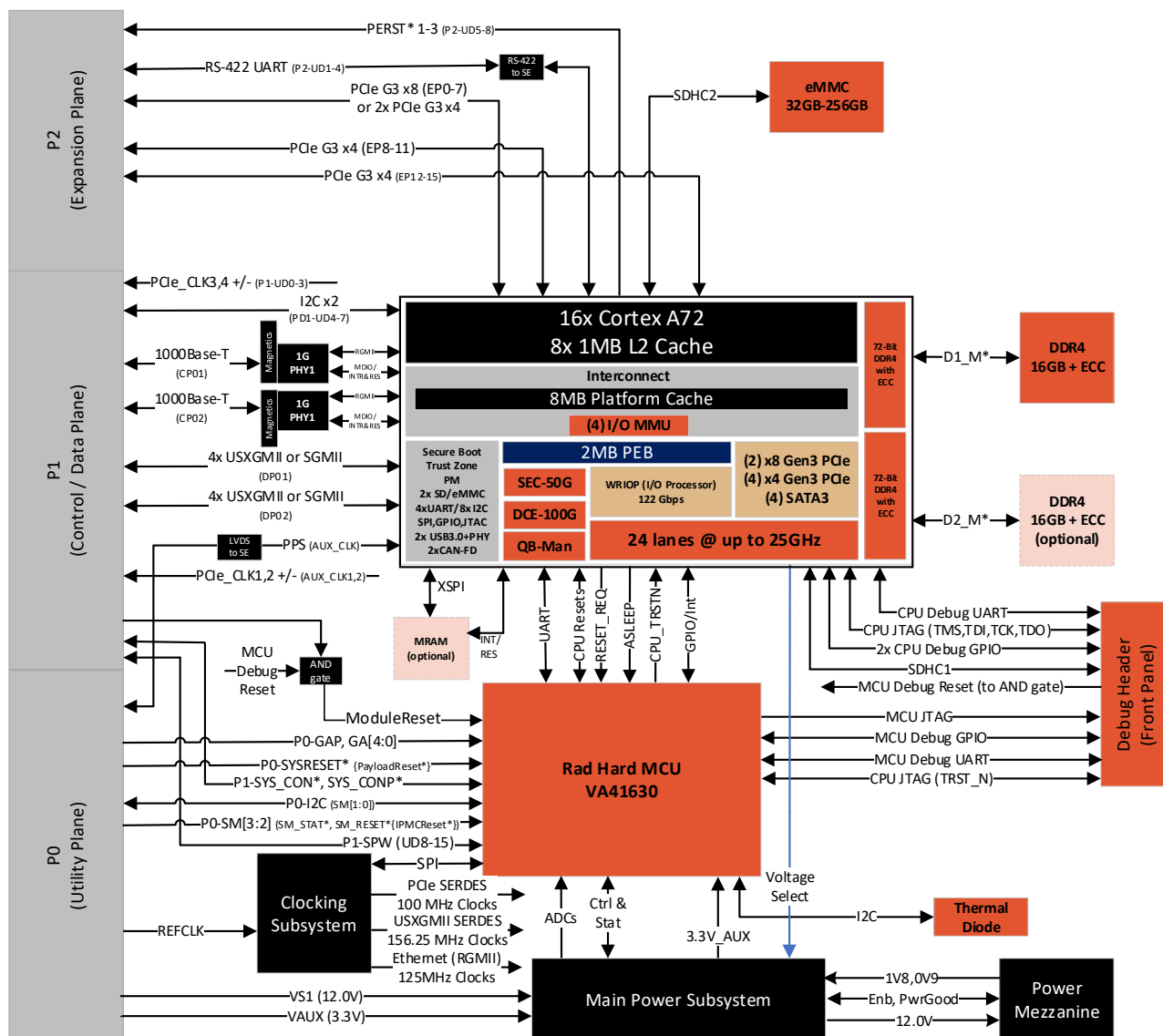


Figure 1. SBC16A72-SVPX High Level Block Diagram

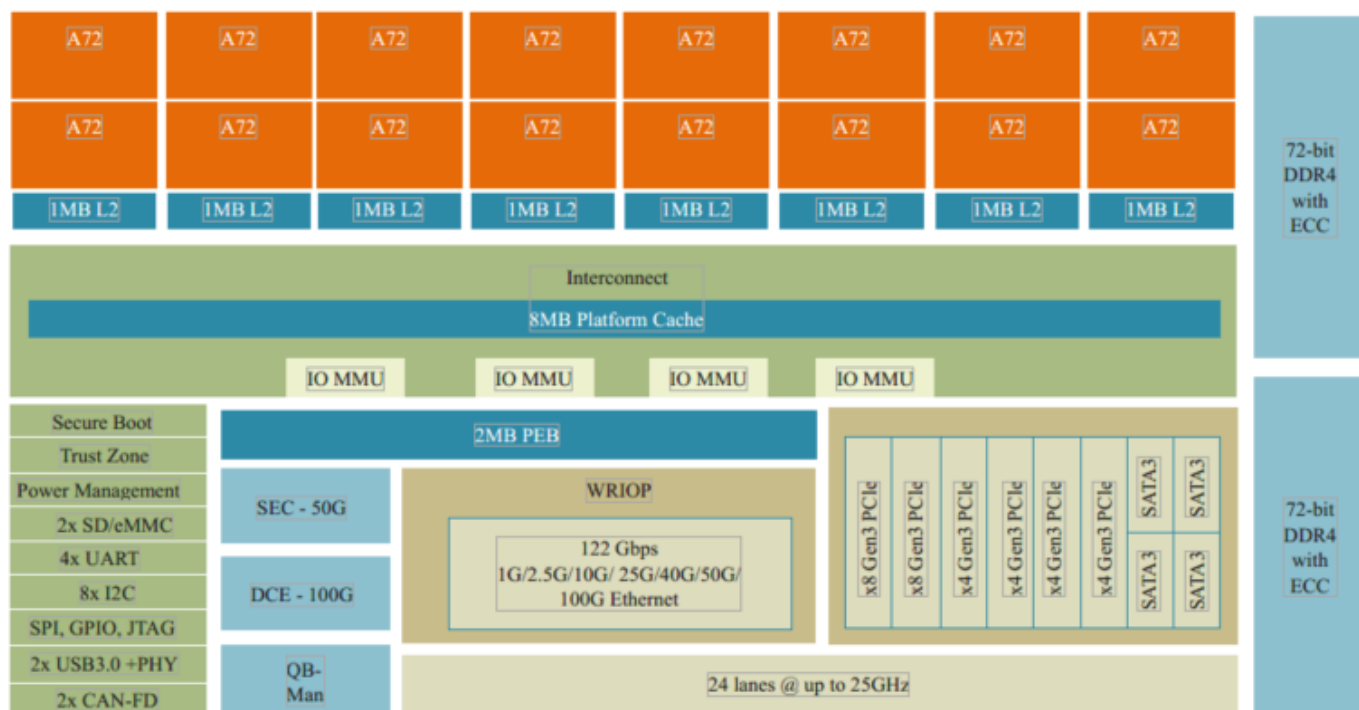


Figure 2. LX2160A Processor High Level Block Diagram

Debug Connector Interfaces

The SBC16A72-SPVX provides a Debug Interface to the front side of the plug-in module for the purpose of debugging the LX2160 CPU and the VA4130 MCU.

The debug interfaces are only intended for ground/lab level testing and pre-flight configuration of the SBC software. The debug connectors will be covered for flight.

J1: 40-pin Front Panel Debug Connector

Table 1. J1 Debug Connector Part Number

Connector	Position	Part Number	Vendor
J1 Debug Connector	J1	LSHM-120-01-F-DH-A-S-K-TR	Samtec

Table 2. J1 Debug Connector Pin list

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	MCU_JTAG_TRSTN	2	SE Input	CPU_JTAG_TRSTN
3	SE Input	MCU_JTAG_TCK	4	SE Input	CPU_JTAG_TCK
5	SE Input	MCU_JTAG_TMS	6	SE Input	CPU_JTAG_TMS
7	SE Input	MCU_JTAG_TDI	8	SE Input	CPU_JTAG_TDI
9	SE Output	MCU_JTAG_TDO	10	SE Output	CPU_JTAG_TDO
11	PWR	GND	12	PWR	GND
13	SE Input	MCU_RESET	14	SE Input	CPU_RESET
15	SE Input	MCU_UART_RX	16	SE Input	CPU_UART_RX
17	SE Input	MCU_UART_TX	18	SE Input	CPU_UART_TX
19	SE Input	MCU_GPIO_LED0	20	SE Input	CPU_GPIO_LED0
21	SE Output	MCU_GPIO_LED1	22	SE Output	CPU_GPIO_LED1
23	PWR	GND	24	PWR	GND
25	SE In/Out	SDHC2_DAT0	26	SE In/Out	SDHC2_DAT2
27	SE In/Out	SDHC2_DAT1	28	SE In/Out	SDHC2_DAT3
29	SE Input	SDHC2_CMD	30	SE Input	SDHC2_DS
31	SE Input	SDHC2_CLK	32	SE Input	SDHC2_CDB
33	PWR	GND	34	PWR	GND
35	SE In/Out	MCU_Spare0	36	SE In/Out	CPU_Spare0
37	SE In/Out	MCU_Spare1	38	SE In/Out	CPU_Spare1
39	PWR	GND	40	PWR	GND

Backplane Slot Profile and Connection Tables

The SBC16A72-SVPX is a 3U VPX card that measures 100 mm x 160mm and is based off the VITA 78.0 standard. The backplane interface is based on the VITA 78.0 Payload Slot Profile: SLT3-PAY-2F2T1Q-14.2.1. For reference, the slot profile for VITA 78.0 is shown below.

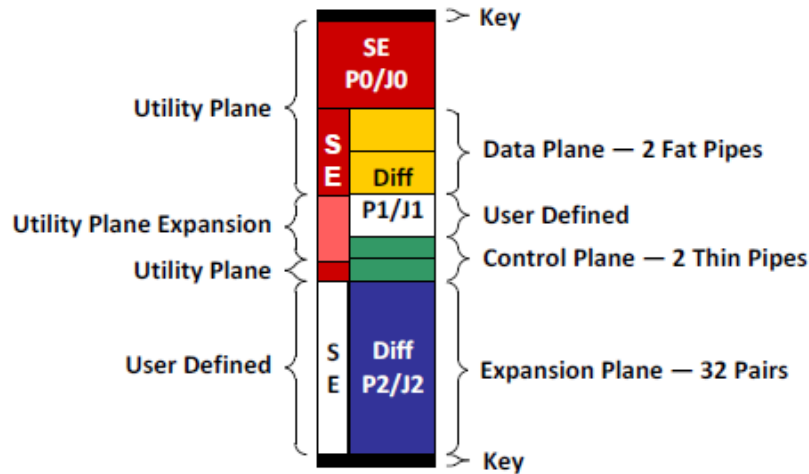


Figure 3. Backplane Slot Profile, SLT3-PAY-2F2T1Q-14.2.1

The table below provides a brief description of each one of the different plans defined in the SLT3-PAY-2F2T1Q-14.2.1 payload slot profile.

Table 3. VITA 78.0 Plane Definitions

Plane	Description
Data Plane	High-speed payload and mission data transfer between processing modules.
Control Plane	Command, control, and health/status communications.
Utility Plane	Power distribution, timing, clocks, reset, discretes, housekeeping.
Expansion Plane	Local or optional I/O expansion between modules (e.g., co-processors or sensors).

Table 4. SBC16A72-SVPX P0, P1, and P2 Connector Part Number and Manufacturer

Connector	Position	Part Number	Vendor
Backplane P0 (Module)	P0	RVPX-P08VM2	Amphenol
Backplane P1 (Module)	P1	RVPX-PE216DM2	Amphenol
Backplane P2 (Module)	P2	RVPX-PE216DM2	Amphenol

Table 5. Backplane J0, J1, and J2 Connector Part Number and Manufacturer

Connector	Position	Part Number	Vendor
Backplane J0 (Backplane)	J0	RVPX-J08EM1	Amphenol
Backplane J1 (Backplane)	J1	RVPX-JE216EM2	Amphenol
Backplane J2 (Backplane)	J2	RVPX-JE216EM2	Amphenol

Backplane Slot Profile and Connection Tables

The SBC16A72-SVPX Single Board Computer is in a 3U, 160mm, SpaceVPX form factor with VITA 78.0 backplane profile SLT3-PAY-2F2T1Q-14.2.1. The P0 through P2 Connector Pinouts are depicted below.

P0 Backplane Connector Signal/Pin Mapping

Figure 4. SBC16A72-SBC Module P0 Backplane Connector Pinout

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Table 6. SBC16A72-SVPX Utility Plane Signal on P0 and SBC16A72-SVPX Signal Name

P0 Connector Pin Location	P0 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowG1	Vs1	12V VS1	
RowG2	Vs1	12V VS1	
RowG3	Vs3	VS3 (N/C)	
RowG4	SM2	SMSTAT*	
RowG5	GAP*	GAP*	
RowG6	GA3*	GA3*	
RowG7	TCK	TCK	
RowG8	GND	GND	
RowF1	Vs1	VS1	
RowF2	Vs1	VS1	
RowF3	Vs3	VS3	
RowF4	SM3	SMRESET*	
RowF5	GA4*	GA4*	
RowF6	GA2*	GA2*	
RowF7	GND	GND	
RowF8	REF_CLK-	BP_REF_CLK_N	
RowE1	Vs1	12V VS1	
RowE2	Vs1	12V VS1	
RowE3	Vs3	VS3 (N/C)	
RowE4	GND	GND	

P0 Connector Pin Location	P0 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowE5	GND	GND	
RowE6	GND	GND	
RowE7	TDO	TDO	
RowE8	REF_CLK+	BP_REF_CLK_P	
RowD1	No Pad*	No Pad	
RowD2	No Pad*	No Pad	
RowD3	No Pad*	No Pad	
RowD4	-12V_Aux	-12V AUX (N/C)	
RowD5	3.3V_Aux	3.3V AUX	
RowD6	+12V_Aux	+12V AUX (N/C)	
RowD7	TDI	TDI	
RowD8	GND	GND	
RowC1	Vs2	VS2 (N/C)	
RowC2	Vs2	VS2 (N/C)	
RowC3	Vs3	VS3 (N/C)	
RowC4	GND	GND	
RowC5	GND	GND	
RowC6	GND	GND	
RowC7	GND	GND	
RowC8	AUX_CLK-	BP_AUX_CLK_N	
RowB1	Vs2	VS2 (N/C)	
RowB2	Vs2	VS2 (N/C)	
RowB3	Vs3	VS3 (N/C)	
RowB4	SYSRESET*	SYSRESET*	
RowB5	SM0	SM_SCL	
RowB6	GA1*	GA1*	
RowB7	TMS	TMS	
RowB8	AUX_CLK+	BP_AUX_CLK_P	
RowA1	Vs2	VS2 (N/C)	
RowA2	Vs2	VS2 (N/C)	
RowA3	Vs3	VS3 (N/C)	
RowA4	NVMRO	NVMRO	
RowA5	SM1	SMSDA	
RowA6	GA0*	GA0*	
RowA7	TRST*	TRST*	
RowA8	GND	GND	

P1 Backplane Connector Signal/Pin Mapping

Table 7. SBC16A72-SVPX Module P1 Connector Pinout

Plug-In Module P1				Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Date Plane Port 1	x8	x4/2x2/4x1	SYS_CONP*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
				GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
				VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD1-	DP01-RD2+
				GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	x8	x4/2x2/4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
				GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
				REF_CLK1-	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
				GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	x8	x4/2x2/4x1	REF_CLK1+	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
				REF_CLK2-	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane	x8	x4/2x2/4x1	REF_CLK2+	GND	GND-J4	CPTp02-DB-	CPTp02-DB+	GND	GND-J4	CPTp02-DA-	CPTp02-DA+
				GND	CPTp02-DD-	CPTp02-DD+	GND-J4	GND	CPTp02-DC-	CPTp02-DC+	GND-J4	GND
				Maskable Reset*	GND	GND-J4	CPTp01-DB-	CPTp01-DB+	GND	GND-J4	CPTp01-DA-	CPTp01-DA+
				GND	CPTp01-DD-	CPTp01-DD+	GND-J4	GND	CPTp01-DC-	CPTp01-DC+	GND-J4	GND

Table 8. SBC16A72-SVPX Module P1 Connector Pinout

P1 Connector Pin Location	P1 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowG1	SYS_CONP*	MCU_BP_PERST*	
RowG2	GND	GND	
RowG3	VBAT	VBAT	
RowG4	GND	GND	
RowG5	SYS_CON*	SYS_CON*	
RowG6	GND	GND	
RowG7	REF_CLK1-	BP_PCI_REFCLK1_N	
RowG8	GND	GND	
RowG9	REF_CLK1+	BP_PCI_REFCLK1_P	
RowG10	GND	GND	
RowG11	REF_CLK2-	BP_PCI_REFCLK2_N	
RowG12	GND	GND	
RowG13	REF_CLK2+	BP_PCI_REFCLK2_P	
RowG14	GND	GND	
RowG15	Maskable Reset*	Maskable Reset*	
RowG16	GND	GND	

P1 Connector Pin Location	P1 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowF1	GND	GND	
RowF2	DP01-TD1-	EPHYA_10G_TX1_N	
RowF3	GND	GND	
RowF4	DP01-TD3-	EPHYA_10G_TX3_N	
RowF5	GND	GND	
RowF6	DP02-TD1-	EPHYB_10G_TX1_N	
RowF7	GND	GND	
RowF8	DP02-TD3-	EPHYB_10G_TX3_N	
RowF9	GND	GND	
RowF10	UD	ETHA_MDIO_SCL	
RowF11	GND	GND	
RowF12	UD	MCU_SW_STXS_N	
RowF13	GND	GND	
RowF14	CPtp02-DD-	Ethernet2_DD_N	
RowF15	GND	GND	
RowF16	CPtp01-DD-	Ethernet1_DD_N	
RowE1_Even	GND-J1	GND-J1	
RowE2_Even	DP01-TD1+	EPHYA_10G_TX1_P	
RowE3_Even	GND-J1	GND-J1	
RowE4_Even	DP01-TD3+	EPHYA_10G_TX3_P	
RowE5_Even	GND-J1	GND-J1	
RowE6_Even	DP02-TD1+	EPHYB_10G_TX1_P	
RowE7_Even	GND-J1	GND-J1	
RowE8_Even	DP02-TD3+	EPHYB_10G_TX3_P	
RowE9_Even	GND-J1	GND-J2	
RowE10_Even	UD	ETHA_MDIO_SDA	
RowE11_Even	GND-J1	GND-J2	
RowE12_Even	UD	MCU_SW_STXS_P	
RowE13_Even	GND-J4	GND-J1	
RowE14_Even	CPtp02-DD+	Ethernet2_DD_P	
RowE15_Even	GND-J4	GND-J1	
RowE16_Even	CPtp01-DD+	Ethernet1_DD_P	
RowE1_Odd	DP01-TD0-	EPHYA_10G_TX0_N	
RowE2_Odd	GND-J1	GND-J1	
RowE3_Odd	DP01-TD2-	EPHYA_10G_TX2_N	
RowE4_Odd	GND-J1	GND-J1	
RowE5_Odd	DP02-TD0-	EPHYB_10G_TX0_N	
RowE6_Odd	GND-J1	GND-J1	
RowE7_Odd	DP02-TD2-	EPHYB_10G_TX2_N	

P1 Connector Pin Location	P1 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowE8_Odd	GND-J1	GND-J1	
RowE9_Odd	UD	BP_PCI_REFCLK4_N	
RowE10_Odd	GND-J1	GND-J2	
RowE11_Odd	UD	MCU_SW_STX_N	
RowE12_Odd	GND-J1	GND-J2	
RowE13_Odd	CPtp02-DB-	Ethernet2_DB_N	
RowE14_Odd	GND-J4	GND-J1	
RowE15_Odd	CPtp01-DB-	Ethernet1_DB_N	
RowE16_Odd	GND-J4	GND-J1	
RowD1	DP01-TD0+	EPHYA_10G_TX0_P	
RowD2	GND	GND	
RowD3	DP01-TD2+	EPHYA_10G_TX2_P	
RowD4	GND	GND	
RowD5	DP02-TD0+	EPHYB_10G_TX0_P	
RowD6	GND	GND	
RowD7	DP02-TD2+	EPHYB_10G_TX2_P	
RowD8	GND	GND	
RowD9	UD	BP_PCI_REFCLK4_P	
RowD10	GND	GND	
RowD11	UD	MCU_SW_STX_P	
RowD12	GND	GND	
RowD13	CPtp02-DB+	Ethernet2_DB_P	
RowD14	GND	GND	
RowD15	CPtp01-DB+	Ethernet1_DB_P	
RowD16	GND	GND	
RowC1	GND	GND	
RowC2	DP01-RD1-	EPHYA_10G_RX1_N	
RowC3	GND	GND	
RowC4	DP01-RD3-	EPHYA_10G_RX3_N	
RowC5	GND	GND	
RowC6	DP02-RD1-	EPHYB_10G_RX1_N	
RowC7	GND	GND	
RowC8	DP02-RD3-	EPHYB_10G_RX3_N	
RowC9	GND	GND	
RowC10	UD	ETHB_MDIO_SCL	
RowC11	GND	GND	
RowC12	UD	MCU_SW_SRXS_N	
RowC13	GND	GND	
RowC14	CPtp02-DC-	Ethernet2_DC_N	

P1 Connector Pin Location	P1 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowC15	GND	GND	
RowC16	CPTp01-DC-	Ethernet1_DC_N	
RowB1_Even	GND-J1	GND-J1	
RowB2_Even	DP01-RD1+	EPHYA_10G_RX1_P	
RowB3_Even	GND-J1	GND-J1	
RowB4_Even	DP01-RD3+	EPHYA_10G_RX3_P	
RowB5_Even	GND-J1	GND-J1	
RowB6_Even	DP02-RD1+	EPHYB_10G_RX1_P	
RowB7_Even	GND-J1	GND-J1	
RowB8_Even	DP02-RD3+	EPHYB_10G_RX3_P	
RowB9_Even	GND-J1	GND-J2	
RowB10_Even	UD	ETHB_MDIO_SDA	
RowB11_Even	GND-J1	GND-J2	
RowB12_Even	UD	MCU_SW_SRXS_P	
RowB13_Even	GND-J4	GND-J1	
RowB14_Even	CPTp02-DC+	Ethernet2_DC_P	
RowB15_Even	GND-J4	GND-J1	
RowB16_Even	CPTp01-DC+	Ethernet1_DC_P	
RowB1_Odd	DP01-RD0-	EPHYA_10G_RX0_N	
RowB2_Odd	GND-J1	GND-J1	
RowB3_Odd	DP01-RD2-	EPHYA_10G_RX2_N	
RowB4_Odd	GND-J1	GND-J1	
RowB5_Odd	DP02-RD0-	EPHYB_10G_RX0_N	
RowB6_Odd	GND-J1	GND-J1	
RowB7_Odd	DP02-RD2-	EPHYB_10G_RX2_N	
RowB8_Odd	GND-J1	GND-J1	
RowB9_Odd	UD	BP_PCI_REFCLK3_N	
RowB10_Odd	GND-J1	GND-J2	
RowB11_Odd	UD	MCU_SW_SRX_N	
RowB12_Odd	GND-J1	GND-J2	
RowB13_Odd	CPTp02-DA-	Ethernet2_DA_N	
RowB14_Odd	GND-J4	GND-J1	
RowB15_Odd	CPTp01-DA-	Ethernet1_DA_N	
RowB16_Odd	GND-J4	GND-J1	
RowA1	DP01-RD0+	EPHYA_10G_RX0_P	
RowA2	GND	GND	
RowA3	DP01-RD2+	EPHYA_40G_RX2_P	
RowA4	GND	GND	
RowA5	DP02-RD0+	EPHYB_10G_RX0_P	

P1 Connector Pin Location	P1 Connector Name	SBC16A72-SVPX Signal Name	Signal Type
RowA6	GND	GND	
RowA7	DP02-RD2+	EPHYB_10G_RX0_P	
RowA8	GND	GND	
RowA9	UD	BP_PCI_REFCLK3_P	
RowA10	GND	GND	
RowA11	UD	MCU_SW_SRX_P	
RowA12	GND	GND	
RowA13	CPtp02-DA+	Ethernet2_DA_P	
RowA14	GND	GND	
RowA15	CPtp01-DA+	Ethernet1_DA_P	
RowA16	GND	GND	

P2 Backplane Connector Signal/Pin Mapping

Table 9. SBC16A72-SVPX Module P2 Connector Pinout

Plug-In Module P2			Row G	Row F	Row E		Row D	Row C	Row B		Row A	
					Even	Odd			Even	Odd		
Backplane J2			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a	
1	Expansion Plane x16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-TD-	EP00-TD+	GND	GND-J2	EP00-RD-	EP00-RD+
2				GND	EP01-TD-	EP01-TD+	GND-J2	GND	EP01-RD-	EP01-RD+	GND-J2	GND
3				UD	GND	GND-J2	EP02-TD-	EP02-TD+	GND	GND-J2	EP02-RD-	EP02-RD+
4				GND	EP03-TD-	EP03-TD+	GND-J2	GND	EP03-RD-	EP03-RD+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using [15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using [15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

Table 10. SBC16A72-SVPX Module P2 Connector Pinout and SBC16A72-SVPX Signal Name

P2 Connector Pin Location	P2 Connector Name	SBC16A72-SVPX Name	Signal Type
RowG1	UD	RS_422_TX_N	
RowG2	GND	GND	
RowG3	UD	RS_422_TX_P	
RowG4	GND	GND	
RowG5	UD	RS_422_RX_N	
RowG6	GND	GND	
RowG7	UD	RS_422_RX_P	
RowG8	GND	GND	
RowG9	UD	BP_PERST1*	
RowG10	GND	GND	
RowG11	UD	BP_PERST2*	
RowG12	GND	GND	
RowG13	UD	BP_PERST3*	
RowG14	GND	GND	
RowG15	UD	BP_PERST4*	
RowG16	GND	GND	

P2 Connector Pin Location	P2 Connector Name	SBC16A72-SVPX Name	Signal Type
RowF1	GND	GND	
RowF2	EP01-TD-	SD3_PCl_e_TX1_N	
RowF3	GND	GND	
RowF4	EP03-TD-	SD3_PCl_e_TX3_N	
RowF5	GND	GND	
RowF6	EP05-TD-	SD3_PCl_e_TX5_N	
RowF7	GND	GND	
RowF8	EP07-TD-	SD3_PCl_e_TX7_N	
RowF9	GND	GND	
RowF10	EP09-TD-	SD2_PCl_e_TX1_N	
RowF11	GND	GND	
RowF12	EP11-TD-	SD2_PCl_e_TX3_N	
RowF13	GND	GND	
RowF14	EP13-TD-	SD2_PCl_e_TX5_N	
RowF15	GND	GND	
RowF16	EP15-TD-	SD2_PCl_e_TX7_N	
RowE1_Even	GND-J2	GND-J2	
RowE2_Even	EP01-TD+	SD3_PCl_e_TX1_P	
RowE3_Even	GND-J2	GND-J2	
RowE4_Even	EP03-TD+	SD3_PCl_e_TX3_P	
RowE5_Even	GND-J2	GND-J2	
RowE6_Even	EP05-TD+	SD3_PCl_e_TX5_P	
RowE7_Even	GND-J2	GND-J2	
RowE8_Even	EP07-TD+	SD3_PCl_e_TX7_P	
RowE9_Even	GND-J2	GND-J2	
RowE10_Even	EP09-TD+	SD2_PCl_e_TX1_P	
RowE11_Even	GND-J2	GND-J2	
RowE12_Even	EP11-TD+	SD2_PCl_e_TX3_P	
RowE13_Even	GND-J2	GND-J2	
RowE14_Even	EP13-TD+	SD2_PCl_e_TX5_P	
RowE15_Even	GND-J2	GND-J2	
RowE16_Even	EP15-TD+	SD2_PCl_e_TX7_P	
RowE1_Odd	EP00-TD-	SD3_PCl_e_TX0_N	
RowE2_Odd	GND-J2	GND-J2	
RowE3_Odd	EP02-TD-	SD3_PCl_e_TX2_N	
RowE4_Odd	GND-J2	GND	
RowE5_Odd	EP04-TD-	SD3_PCl_e_TX4_N	
RowE6_Odd	GND-J2	GND	
RowE7_Odd	EP06-TD-	SD3_PCl_e_TX6_N	

P2 Connector Pin Location	P2 Connector Name	SBC16A72-SVPX Name	Signal Type
RowE8_Odd	GND-J2	GND-J2	
RowE9_Odd	EP08-TD-	SD2_PCl_e_TX0_N	
RowE10_Odd	GND-J2	GND-J2	
RowE11_Odd	EP10-TD-	SD2_PCl_e_TX2_N	
RowE12_Odd	GND-J2	GND-J2	
RowE13_Odd	EP12-TD-	SD2_PCl_e_TX4_N	
RowE14_Odd	GND-J2	GND-J2	
RowE15_Odd	EP14-TD-	SD2_PCl_e_TX6_N	
RowE16_Odd	GND-J2	GND-J2	
RowD1	EP00-TD+	SD3_PCl_e_TX0_P	
RowD2	GND	GND	
RowD3	EP02-TD+	SD3_PCl_e_TX2_P	
RowD4	GND	GND-J2	
RowD5	EP04-TD+	SD3_PCl_e_TX4_P	
RowD6	GND	GND-J2	
RowD7	EP06-TD+	SD3_PCl_e_TX6_P	
RowD8	GND	GND	
RowD9	EP08-TD+	SD2_PCl_e_TX0_P	
RowD10	GND	GND	
RowD11	EP10-TD+	SD2_PCl_e_TX2_P	
RowD12	GND	GND	
RowD13	EP12-TD+	SD2_PCl_e_TX4_P	
RowD14	GND	GND	
RowD15	EP14-TD+	SD2_PCl_e_TX6_P	
RowD16	GND	GND	
RowC1	GND	GND	
RowC2	EP01-RD-	SD3_PCl_e_RX1_N	
RowC3	GND	GND	
RowC4	EP03-RD-	SD3_PCl_e_RX3_N	
RowC5	GND	GND	
RowC6	EP05-RD-	SD3_PCl_e_RX5_N	
RowC7	GND	GND	
RowC8	EP07-RD-	SD3_PCl_e_RX7_N	
RowC9	GND	GND	
RowC10	EP09-RD-	SD2_PCl_e_RX1_N	
RowC11	GND	GND	
RowC12	EP11-RD-	SD2_PCl_e_RX3_N	
RowC13	GND	GND	
RowC14	EP13-RD-	SD2_PCl_e_RX5_N	

P2 Connector Pin Location	P2 Connector Name	SBC16A72-SVPX Name	Signal Type
RowC15	GND	GND	
RowC16	EP15-RD-	SD2_PCl_e_RX7_N	
RowB1_Even	GND-J2	GND-J2	
RowB2_Even	EP01-RD+	SD3_PCl_e_RX1_P	
RowB3_Even	GND-J2	GND-J2	
RowB4_Even	EP03-RD+	SD3_PCl_e_RX3_P	
RowB5_Even	GND-J2	GND-J2	
RowB6_Even	EP05-RD+	SD3_PCl_e_RX5_P	
RowB7_Even	GND-J2	GND-J2	
RowB8_Even	EP07-RD+	SD3_PCl_e_RX7_P	
RowB9_Even	GND-J2	GND-J2	
RowB10_Even	EP09-RD+	SD2_PCl_e_RX1_P	
RowB11_Even	GND-J2	GND-J2	
RowB12_Even	EP11-RD+	SD2_PCl_e_RX3_P	
RowB13_Even	GND-J2	GND-J2	
RowB14_Even	EP13-RD+	SD2_PCl_e_RX5_P	
RowB15_Even	GND-J2	GND-J2	
RowB16_Even	EP15-RD+	SD2_PCl_e_RX7_P	
RowB1_Odd	EP00-RD-	SD3_PCl_e_RX0_N	
RowB2_Odd	GND-J2	GND-J2	
RowB3_Odd	EP02-RD-	SD3_PCl_e_RX2_N	
RowB4_Odd	GND-J2	GND	
RowB5_Odd	EP04-RD-	SD3_PCl_e_RX4_N	
RowB6_Odd	GND-J2	GND	
RowB7_Odd	EP06-RD-	SD3_PCl_e_RX6_N	
RowB8_Odd	GND-J2	GND-J2	
RowB9_Odd	EP08-RD-	SD2_PCl_e_RX0_N	
RowB10_Odd	GND-J2	GND-J2	
RowB11_Odd	EP10-RD-	SD2_PCl_e_RX2_N	
RowB12_Odd	GND-J2	GND-J2	
RowB13_Odd	EP12-RD-	SD2_PCl_e_RX4_N	
RowB14_Odd	GND-J2	GND-J2	
RowB15_Odd	EP14-RD-	SD2_PCl_e_RX6_N	
RowB16_Odd	GND-J2	GND-J2	
RowA1	EP00-RD+	SD3_PCl_e_RX0_P	
RowA2	GND	GND	
RowA3	EP02-RD+	SD3_PCl_e_RX2_P	
RowA4	GND	GND-J2	
RowA5	EP04-RD+	SD3_PCl_e_RX4_P	

P2 Connector Pin Location	P2 Connector Name	SBC16A72-SVPX Name	Signal Type
RowA6	GND	GND-J2	
RowA7	EP06-RD+	SD3_PCl_e_RX6_P	
RowA8	GND	GND	
RowA9	EP08-RD+	SD2_PCl_e_RX0_P	
RowA10	GND	GND	
RowA11	EP10-RD+	SD2_PCl_e_RX2_P	
RowA12	GND	GND	
RowA13	EP12-RD+	SD2_PCl_e_RX4_P	
RowA14	GND	GND	
RowA15	EP14-RD+	SD2_PCl_e_RX6_P	
RowA16	GND	GND	

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX	3.3V Auxiliary Input	3	3.6	Vdc
Pd	Max Power Dissipation		40	W
Storage Temp		-40	+105	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Mass			0.65 (TBC)	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID	RDM 1x	30k	rad (Si)
nd-SEL Immunity		37	MeV-cm ² /mg
Destructive/Non-Recoverable SEE Rate	LEO ISS Orbit 415km / 51.6° MEO GPS 20,200 km / 55° GEO 35,786km / 0°	1.50e-10 4.61e-09 5.24e-09	per day
External or Ground Intervention SEE Rate	LEO ISS Orbit 415km / 51.6° MEO GPS 20,200 km / 55° GEO 35,786km / 0°	1.69e-06 2.93e-05 3.76e-05	per day

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@Ta = 30 °C @Ta = 50 °C @Ta = 60 °C	749,511 TBD TBD	hours
Reliability (R) @ 30°C / 100% Active	3 Years 5 Years 7 Years 12 Years	TBD 0.943 0.921 0.869	
Electrical Testing	Functional and Performance	Pass/Fail	

Acceptance Testing (FM3 Class C and FM4 Class D)

Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	

Qualification Testing

Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles
Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Functional Description

The Frontgrade SBC16A72-SVPX is a 3U SpaceVPX single board computer (SBC) engineered to provide high-performance embedded processing, secure networking, and deterministic system control for platforms operating in size-, weight-, and power-constrained environments. Built around the NXP LX2160 multicore processor, the board enables scalable mission computing architectures capable of supporting payload management, onboard data processing, networking, and distributed edge computing applications.

At the center of the SBC16A72-SVPX is a 16-core Arm® Cortex®-A72 processor operating at frequencies up to 2.2 GHz. The processor delivers high compute density and parallel processing capability suitable for mission applications requiring real-time decision making, sensor fusion, software-defined functionality, and high-throughput data movement. The multicore architecture supports virtualization, containerized applications, and distributed processing frameworks commonly deployed in modern SpaceVPX systems.

The board provides extensive high-speed interconnect capability through its SpaceVPX backplane interfaces. Four PCI Express® Gen3 x4 interfaces enable high-bandwidth connectivity to payload processors, FPGA accelerators, storage devices, and networking modules. Ethernet connectivity includes dual 1000Base-T interfaces and up to eight USXGMII/SGMII ports to support network switching, command and telemetry routing, and distributed payload communication. These interfaces allow the SBC16A72-SVPX to function as a central mission processor, network controller, or distributed compute node within larger modular architectures.

The SBC16A72-SVPX supports deterministic and time-synchronized operation through integrated utility and control interfaces. SpaceWire connectivity, RS-422 UARTs, GPIO, I2C, and precision PPS input enable integration with avionics subsystems, timing networks, and control electronics. The utility implementation supports SpaceVPX system management functions including geographic addressing, clocks, resets, health monitoring, and intelligent power management.

Security features are integrated throughout the platform architecture. The NXP LX2160 Security Engine provides hardware-accelerated cryptographic processing, secure key storage, and authentication services. Secure boot and Arm TrustZone™ technology establish a hardware-rooted chain of trust that protects mission software and isolates trusted execution environments from non-secure applications. These capabilities support secure command processing, protected data handling, and cyber-resilient system operation.

Memory resources include ECC-protected DDR4 SDRAM configured as 2 × 16 GB 72-bit memory channels operating at 2400 MT/s, supporting reliable operation in mission-critical environments. Non-volatile storage includes 32 GB eMMC 5.1 for operating systems, applications, and persistent mission data. Optional Dual-QSPI MRAM provides radiation-tolerant non-volatile memory for critical storage requirements and mission assurance applications.

The SBC16A72-SVPX is aligned with VITA 78.0 SpaceVPX standards and conforms to Profile SLT3-PAY-2F2T1Q-14.2.1, enabling interoperability with standardized SpaceVPX backplanes and payload infrastructures. The platform is supported by the NXP Layerscape Linux Distribution SDK, including board support packages, drivers, bootloaders, security tools, and Yocto/BitBake integration to accelerate software development and deployment.

Designed for high-reliability embedded environments, the SBC16A72-SVPX provides a flexible and scalable processing solution for mission computing, secure networking, autonomous systems, payload control, and edge analytics applications.

Software Ecosystem

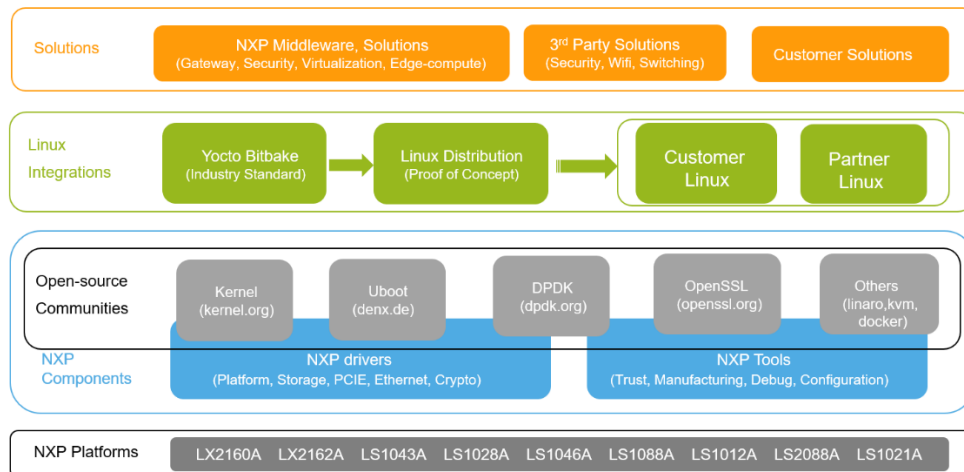


Figure 5. NXP Layerscape Software

Features

Layerscape LDP Components

- Freely available
 - Download from public repositories (e.g. github.com)
 - No need to download a large ISO and extract
- Modularized
 - Boot-loaders, Kernels, User-space libraries, Tools, Configuration
 - Pick and choose ones you need
- Clean layering, separation
 - Separate patches on top of open source
 - Patches identified by platform/IP
- Easy updates via Git
 - Periodic releases and interim updates
 - Support for two recent LTS kernels

Layerscape LDP

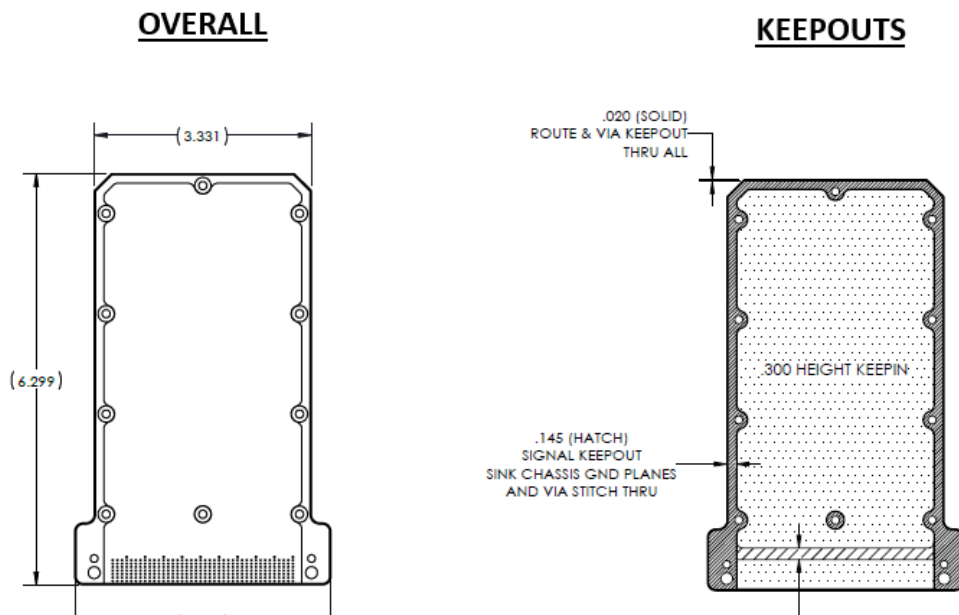
- Easy boot mechanisms
 - Boot from multiple sources
 - Simple, quick updates from any mass-storage
 - Brick-proof mechanism* - easy recovery via SD
- Easy runtime upgrades
 - Rich LDP user-land and repositories
 - On-the-fly install with apt-get
 - Build/install from source on target
- Latest and greatest
 - Latest Layerscape platforms
 - Latest drivers and features
 - Layerscape specific tools, drivers

What's New In L6.1.1-1.0.0-LLDP

- NXP Layerscape LDP userland:
 - NXP Layerscape LDP, including Linux distro main packages and NXP packages
- Toolchain: gcc-11.2, glibc-2.36, binutils-2.38, gdb-12.1
- Linux kernel core and virtualization:
 - LTS kernel 6.1.1 update
- Linux kernel drivers:
 - Data Plane Development Kit (DPDK):
 - Virtualization - OVS-DPDK
- U-Boot bootloader:
 - U-Boot v2022.04 update
- Other tools and utilities:
 - Yocto bitbake

Mechanical Drawing

Placeholder (needs updated with latest information)



Need Proper Mechanical outline drawings for finished module

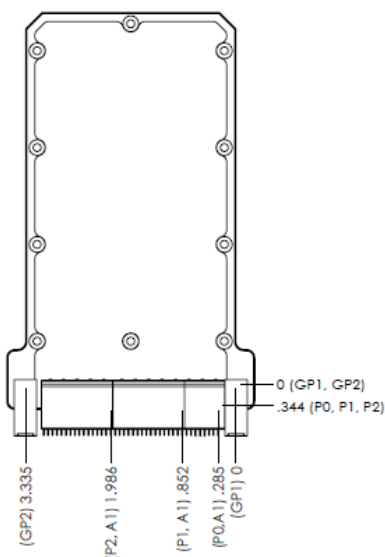


Figure 6. SBC16A72-SVPX Mechanical Outline Drawing

Revision History

Date	Rev	Author	Change Description	Page #
6/1/2026	1.0	DPA	Initial Preliminary Datasheet	All

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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