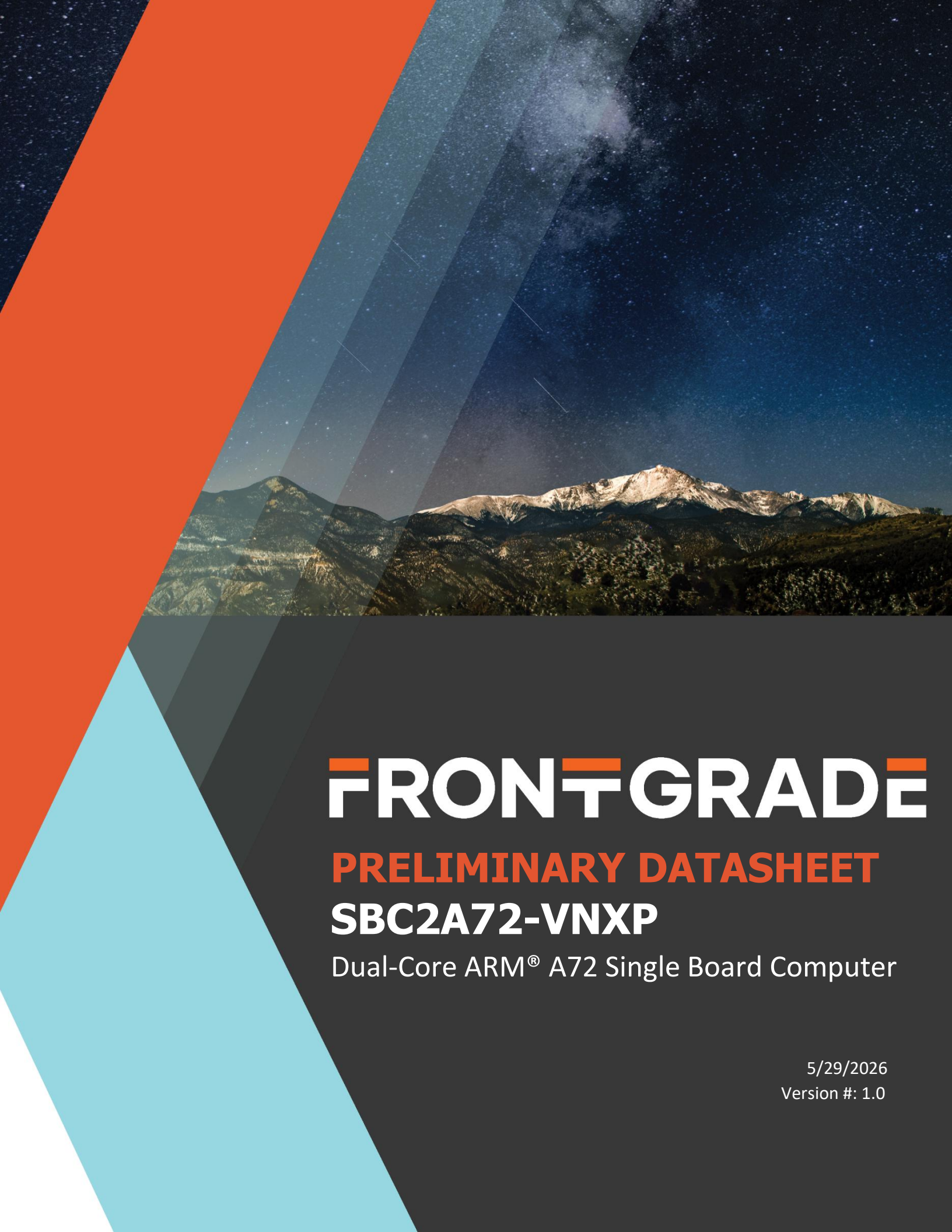




FRONTGRADE

PRELIMINARY DATASHEET

SBC2A72-VNXP

Dual-Core ARM® A72 Single Board Computer

5/29/2026
Version #: 1.0



Introduction

The Frontgrade™ SBC2A72-VNXP Single Board Computer provides a compelling mix of high-performance processing and interface capability, in low power SWaP optimized design. Implemented as a 19mm VITA 90.0 VNX+ plug-in module, the SBC2A72-VNXP is ideal for edge and small form-factor compute and graphics processing applications. This compact VNX+ design is small, lightweight, and power efficient while offering a strong combination of compute and graphics processing power along with a strong mix of interfaces.

The Frontgrade SBC2A72-VNXP features the power efficient and radiation tolerant VA7230 (NXP LS1028A) Dual ARM® Cortex®-A72 processor with integrated Graphics Processing Unit capable of 10.4 GFLOPs performance. Adding to the processing capabilities of the VA7230, the SBC provides a strong complement of communications and interface protocols to support high-throughput networking, graphics, command, control, and telemetry in conjunction with extensive memory facilities heretofore unattainable in a small form factor solution.

Moreover, in keeping with the system integration goals of VNX+ solution where front-panel interfaces are discouraged, all application and operational signals are connected through the backplane interface. The only front-panel connector signals are used for debug purposes and ultimately left unconnected (and covered) after integration for flight.

This Single Board Computer includes a radiation hardened MCU which provides, among other things, system management between plug-in modules integrated into a larger system as well as local monitoring and power management to elements local to the SBC. Additionally, the MCU expands the interfaces to the system backplane in the form of UARTs, SpaceWire, and GPIO.

Applications

- Command and Data Handling (C&DH)
- Lunar Terrain Vehicles
- Onboard payload processing
- Networking and Communications

Why it Matters

The Frontgrade™ SBC2A72-VNXP matters because it brings powerful processing, graphics, and networking capabilities to space-constrained applications in a compact, low-power VNX+ form factor. Its radiation-tolerant architecture enables reliable edge computing, payload processing, and mission management in harsh environments. With extensive backplane connectivity and onboard system management, it simplifies integration while supporting advanced autonomy and high-throughput data handling. This combination of performance, resilience, and SWaP efficiency makes it an ideal computing foundation for next-generation systems.

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
SBC2A72-VNXP-OP-EDU	EDU= EDU/EM (Room Temp only)	Lab / Development Use Cases
SBC2A72-VNXP-OP-FM4	COTS Parts Grade (-10°C to +50°C)	Target Mission Class D
SBC2A72-VNXP-OP-FM3	Level 3 Parts Grade (-10°C to +50°C)	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds.

Features

Processing Performance

- Based on Vorago VA7230 Processor (NXP LS1028A) with GPU Acceleration
 - Two 32/64-bit ARM® Cortex®-A72 cores with the following capabilities:
 - ~15K DMIPS performance at 1.5 GHz operation
 - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache
 - Single cluster of two cores sharing 1MB L2 cache
 - Graphics processing unit
 - Supports Geometry rate 100 Mtri/sec
 - Pixel rate 650 Mpixel/sec
 - 10.4 GFLOPS (32-bit high precision)
 - Supports OpenGL ES 3.0, 2.0, 1.1
 - Supports OpenCL 1.1, 1.2

User Memory

- 8GB + ECC DDR4 (x36 bus width)
 - 1600 MT/s
- Apps and Storage
 - 32GB e.MMC 5.1
 - Supports enhanced secure digital host controller (eSDHC)

Mass & Thermal

- Mass: <0.35 kg
- 19mm VNX+ form factor
- -10°C to +50°C operational case temperature
- Power consumption: <15W Typical / 30W Max
- TID: Up to 30K rad (Si)
- SEL Immune ≤ 37 MeV-cm²/mg

Debug Interfaces

- MCU JTAG, MCU Debug UART, and 2x Debug GPIO
- CPU JTAG, CPU Debug UART, and 3x Debug GPIO
- CPU Debug Reset
- SDCARD

Security Features

- Security Engine
- Secure boot
- Arm TrustZone™

Backplane Interfaces

(VITA 90.1 Profile: VNX.PL-1-19.400-7.2.1.1-SBC)

- 4x GbE ports
 - 2x TSN 1GbE
 - 2x 1000Base-X
- 3x PCIe 3.0 Lanes (x2 port and x1 port)
- 2x USB 3.0 Interfaces
- 1x DisplayPort Out (
 - DisplayPort 1.3 and eDP 1.4
- 6x GPIO + 2x GPIO/I2C
- 1x PPS Input

Backplane Utility Segment

- 5x GA + 1x GA Parity
- SYSRESET* & GDISCRETE
- 2x GPIO
- 1x I2C + SM_STAT* & SM_RESET*
- 1x UART
- 1x SpW
- 1x LVDS REFCLK Input (100MHz)
- 1x LVDS PCIe_CLK Output (100MHz)
- 12V VS1
- 3.3V_AUX

Software

The SBC2A72-VNXP is supported by the NXP Layerscape Linux Distribution POC.

- <https://www.nxp.com/design/design-center/software/embedded-software/linux-software-and-development-tools/layercape-linux-distribution-poc:LAYERSCAPE-SDK>

The Layerscape SDK includes a BSP and Drivers for the LS1028A (VA7230) appropriate for peripherals native to the processor along with toolsets including Trust, Manufacturing, Debug, and Configuration.

The SDK integrates into a software stack from Open-source Communities (e.g. Uboot) into Linux Integrations like Yocto Bitbake, and up through application support packages like NXP Middleware and 3rd Party Solutions

Block Diagram

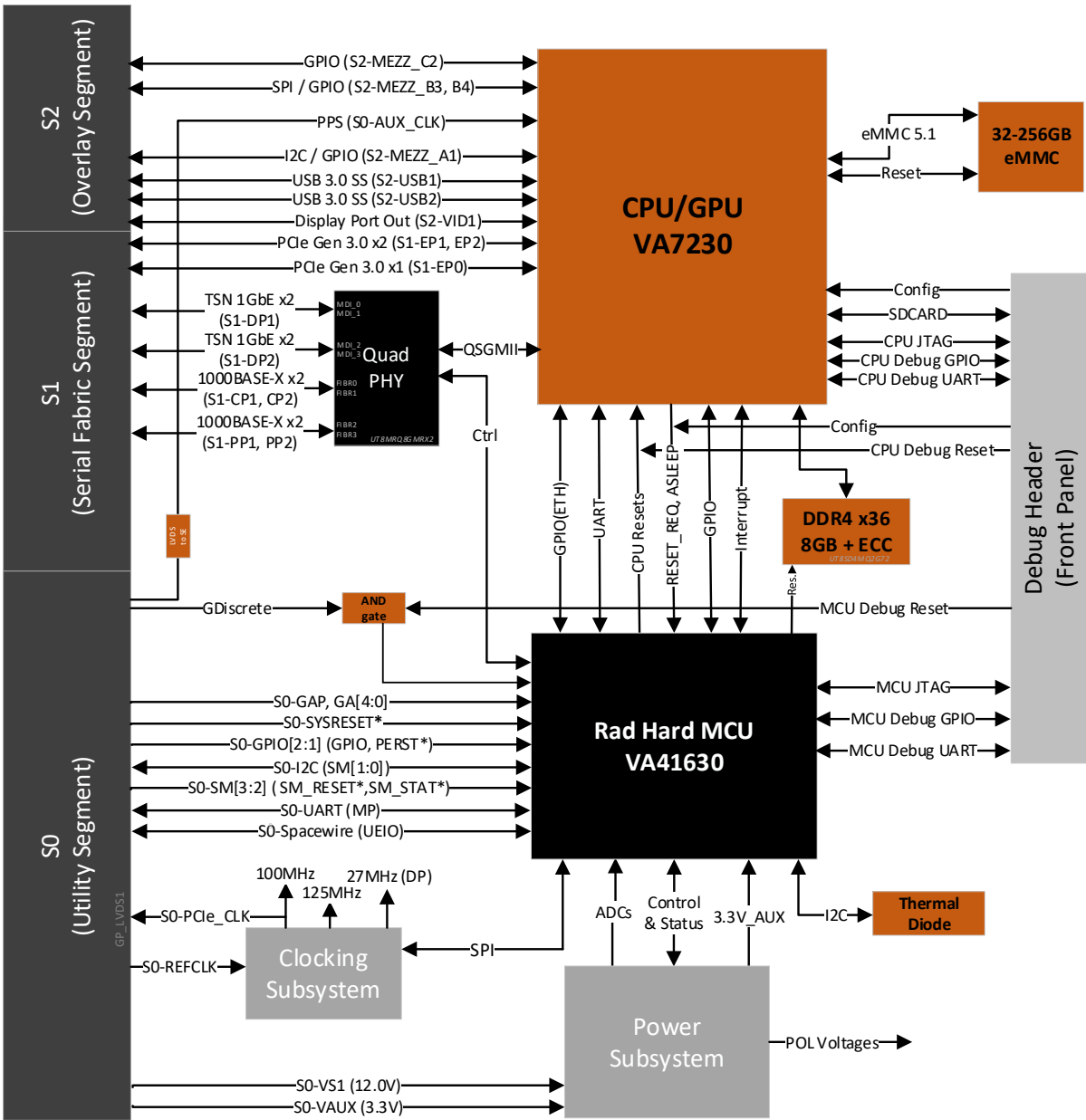


Figure 1. SBC2A72-VNXP High Level Block Diagram

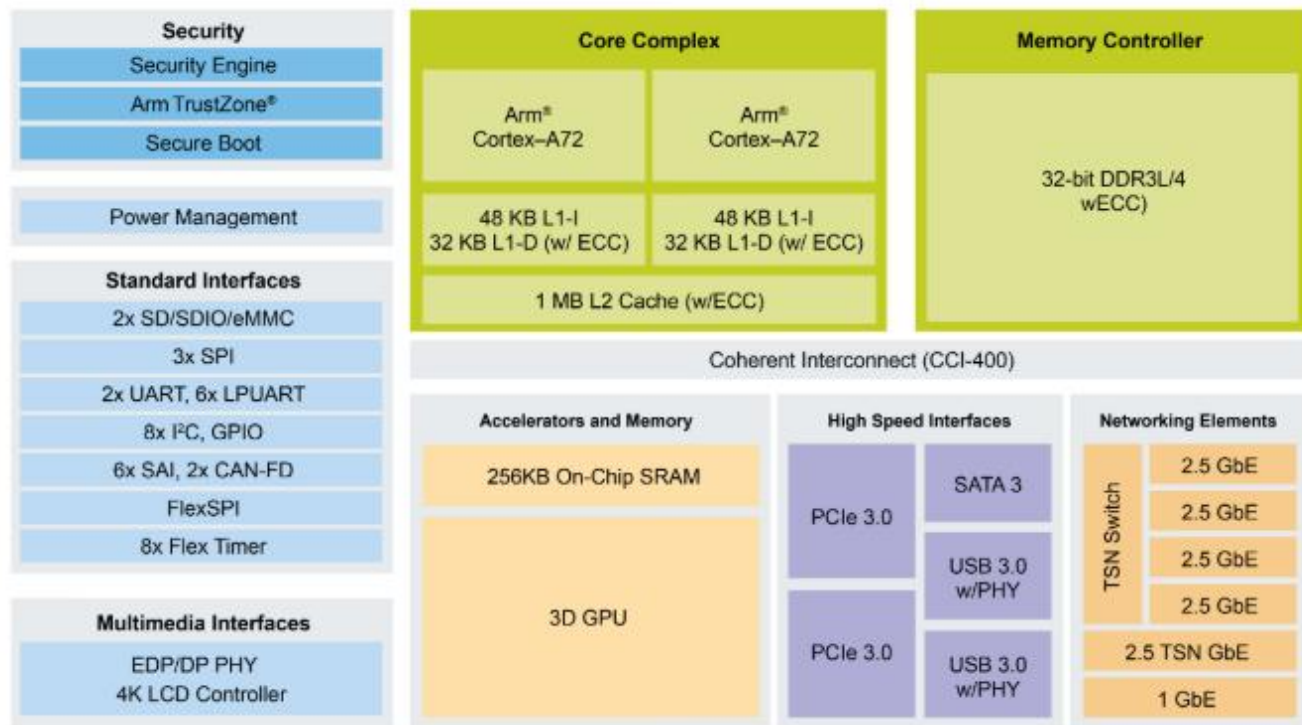


Figure 2. VA7230 Processor High Level Block Diagram

Debug Connector Interface

The SBC2A72-VNXP provides a single Debug Interface to the front side of the plug-in module. The debug interface is only intended for ground/lab level testing and pre-flight configuration of the SBC software.

J2: 40-pin Front Panel Debug Connector

Table 1. J2 Debug Connector Pin list

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	MCU_JTAG_TRSTN	2	SE Input	CPU_JTAG_TRSTN
3	SE Input	MCU_JTAG_TCK	4	SE Input	CPU_JTAG_TCK
5	SE Input	MCU_JTAG_TMS	6	SE Input	CPU_JTAG_TMS
7	SE Input	MCU_JTAG_TDI	8	SE Input	CPU_JTAG_TDI
9	SE Output	MCU_JTAG_TDO	10	SE Output	CPU_JTAG_TDO
11	PWR	GND	12	PWR	GND
13	SE Input	MCU_RESET	14	SE Input	CPU_RESET
15	SE Input	MCU_UART_RX	16	SE Input	CPU_UART_RX
17	SE Input	MCU_UART_TX	18	SE Input	CPU_UART_TX
19	SE Input	MCU_GPIO_LED0	20	SE Input	CPU_GPIO_LED0
21	SE Output	MCU_GPIO_LED1	22	SE Output	CPU_GPIO_LED1
23	PWR	GND	24	PWR	GND
25	SE In/Out	SDHC2_DAT0	26	SE In/Out	SDHC2_DAT2
27	SE In/Out	SDHC2_DAT1	28	SE In/Out	SDHC2_DAT3
29	SE Input	SDHC2_CMD	30	SE Input	MCU_CPU_ASLEEP
31	SE Input	SDHC2_CLK	32	SE Input	MCU_CPU_UART_RX
33	PWR	GND	34	PWR	GND
35	NC	NC	36	SE Output	CPU_CLK_OUT
37	PWR	1.8V	38	SE Output	CPU_TA_PROG
39	PWR	GND	40		GND

Table 2. J2 Connector Part Number and Manufacturer (Module)

Connector	Position	Part Number	Vendor
40-Pin Debug Connector	J2	LSHM-120-01-F-DH-A-S-K-TR	Samtec

Backplane Slot Profile and Connection Tables

The SBC2A72-VNXP is a 19mm pitch VNX+ plug-in module (PIM). As such, the backplane interface is a single 400-pin connector based on Profile: VNX.PL-1-19.400-7.2.1.1-SBC

For reference, the connector pinout segments taken from VITA 90.0 are shown below.

Table 3. Plug-In Module S0, S1, and S2 Segments

Segment Name	Description
S0 - Utility Segment	Pin region containing power and other utility signals common to all Payload Templates and slot profiles.
S1 - Communications Segment	Pin region containing communications ports based on industry-standard fabrics and interfaces.
S2 - Overlay Segment	Copper and/or coaxial/optical Connector Module regions for functional or application-specific pin/signal definitions.

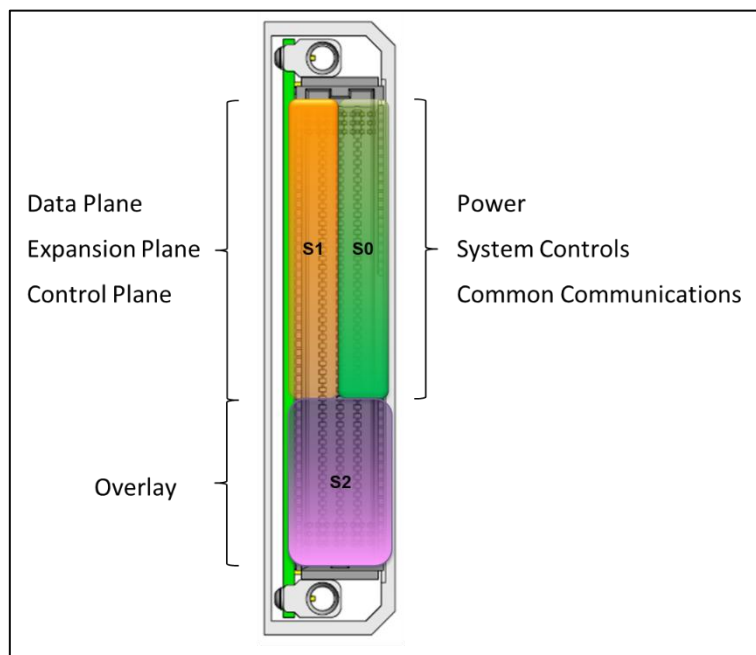


Figure 3. 400-Pin 19mm PIM Segment Diagram

As the diagram suggests, S0 is focused on Power and Utility Plane Signals. Segment S1 focusses on Control Plane (CP), Data Plane (DP), and Expansion Plane (EP). The final segment S2 is called an Overlay which allocates pins for application specific signal choices or allocate space for optical and coax apertures.

P1 Backplane Connector Signal/Pin Mapping

Table 5. P1 400-pin Backplane Connector Pinout

SBC2A72-VNXP Backplane Interface			Revision: 1.1		Title: 400-Pin HSDC Without CM Payload Module Pin Map		VITA 90.1 Slot Profile: VITA 90 400-Pin IO Intensive Compute Profile																		
			Date: 1/8/2025		Use: Compute Module, Single Video, Mezz I/O																				
400-Pin VNX+ HSDC Without CM Pin Assignments																									
Row A			Row B			Row C			Row D			Row E			Row F			Row G			Row H				
Col	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Col
1	Expansion	A1	PCIE1_LN0_RX_P	Expansion	B1	GND	Expansion	C1	EP1_RX3_P	Expansion	D1	GND	Expansion	E1	EP1_RX6_P	Expansion	F1	GND	Expansion	G1	VS1	Expansion	H1	VS1	1
2		A2	PCIE1_LN0_RX_N		B2	GND		C2	EP1_RX3_N		D2	GND		E2	EP1_RX6_N		F2	GND		G2			H2		2
3		A3	GND		B3	PCIE2_LN1_RX_P		C3	GND		D3	EP1_RX5_P		E3	GND		F3	GBE1_MDIO_P		G3			H3		3
4		A4	GND		B4	PCIE2_LN1_RX_P		C4	GND		D4	EP1_RX5_N		E4	GND		F4	GBE1_MDIO_N		G4			H4		4
5		A5	PCIE2_LN0_RX_P		B5	GND		C5	EP1_RX4_P		D5	GND		E5	EP1_RX7_P		F5	GND		G5			H5		5
6		A6	PCIE2_LN0_RX_N		B6	GND		C6	EP1_RX4_N		D6	GND		E6	EP1_RX7_N		F6	GND		G6			H6		6
7	Data	A7	GND	Data	B7	Ethernet1_DB_P	Data	C7	GND	Data	D7	Ethernet3_DA_P	Data	E7	GND	Data	F7	GBE1_MDIO1_P	Data	G7	VS2	Data	H7	VS2	7
8		A8	GND		B8	Ethernet1_DB_N		C8	GND		D8	Ethernet3_DA_N		E8	GND		F8	GBE1_MDIO1_N		G8			H8		8
9		A9	Ethernet1_DA_P		B9	GND		C9	Ethernet1_DD_P		D9	GND		E9	Ethernet3_DC_P		F9	GND		G9			H9		9
10		A10	Ethernet1_DA_N		B10	GND		C10	Ethernet1_DD_N		D10	GND		E10	Ethernet3_DC_N		F10	GND		G10			H10		10
11		A11	GND		B11	Ethernet1_DC_P		C11	GND		D11	Ethernet3_DB_P		E11	GND		F11	GBE1_MDIO2_P		G11			H11		11
12		A12	GND		B12	Ethernet1_DC_N		C12	GND		D12	Ethernet3_DB_N		E12	GND		F12	GBE1_MDIO2_N		G12			H12		12
13	Control	A13	1000BASEX-RX1_P	Utility	B13	GND	Utility	C13	SMB_SCL	Utility	D13	GND	Utility	E13	Ethernet3_DD_P	Utility	F13	GND	Utility	G13	VS4	Utility	H13	VHEATER	13
14		A14	1000BASEX-RX1_N		B14	GND		C14	SMB_SDA		D14	GND		E14	Ethernet3_DD_N		F14	GND		G14			H14		14
15		A15	GND		B15	SMA_SCL		C15	GND		D15	SO_UART_RX		E15	GND		F15	GBE1_MDIO3_P		G15			H15		15
16		A16	GND		B16	SMA_SDA		C16	GND		D16	SO_UART_TX		E16	GND		F16	GBE1_MDIO3_N		G16			H16		16
17		A17	1000BASEX-TX1_P		B17	GND		C17	EP1_TX3_P		D17	GND		E17	REFCLK_P		F17	GND		G17			H17		17
18		A18	1000BASEX-TX1_N		B18	GND		C18	EP1_TX3_N		D18	GND		E18	REFCLK_N		F18	GND		G18			H18		18
19	Expansion	A19	GND	Expansion	B19	PCIE2_LN0_TX_P	Expansion	C19	GND	Expansion	D19	EP1_TX5_P	Expansion	E19	GND	Expansion	F19	AUXCLK_P	Expansion	G19	GND	Expansion	H19	SER1_RX_P	19
20		A20	GND		B20	PCIE2_LN0_TX_N		C20	GND		D20	EP1_TX5_N		E20	GND		F20	AUXCLK_N		G20	H20		20		
21		A21	PCIE1_LN0_TX_P		B21	GND		C21	EP1_TX4_P		D21	GND		E21	EP1_TX7_P		F21	GND		G21	H21		21		
22		A22	PCIE1_LN0_TX_N		B22	GND		C22	EP1_TX4_N		D22	GND		E22	EP1_TX7_N		F22	GND		G22	H22		22		
23		A23	GND		B23	PCIE2_LN1_TX_P		C23	GND		D23	EP1_TX6_P		E23	GND		F23	USB1_D_P		G23	H23		23		
24		A24	GND		B24	PCIE2_LN1_TX_N		C24	GND		D24	EP1_TX6_N		E24	GND		F24	USB1_D_N		G24	H24		24		
25	Data	A25	Ethernet2_DA_P	Data	B25	GND	Data	C25	Ethernet2_DD_P	Data	D25	GND	Data	E25	Ethernet4_DC_P	Data	F25	GND	Data	G25	SpaceWire	Data	H25	GA1*	25
26		A26	Ethernet2_DA_N		B26	GND		C26	Ethernet2_DD_N		D26	GND		E26	Ethernet4_DC_N		F26	GND		G26	H26		26		
27		A27	GND		B27	Ethernet2_DC_P		C27	GND		D27	Ethernet4_DB_P		E27	GND		F27	SD-PCIE_CLK_P		G27	H27		27		
28		A28	GND		B28	Ethernet2_DC_N		C28	GND		D28	Ethernet4_DB_N		E28	GND		F28	SD-PCIE_CLK_N		G28	H28		28		
29		A29	Ethernet1_DB_P		B29	GND		C29	Ethernet4_DA_P		D29	GND		E29	Ethernet4_DD_P		F29	GND		G29	H29		29		
30		A30	Ethernet1_DB_N		B30	GND		C30	Ethernet4_DA_N		D30	GND		E30	Ethernet4_DD_N		F30	GND		G30	H30		30		
31	Control	A31	GND	Control	B31	DP_LANE1_P	Control	C31	GND	Control	D31	1000BASEX-TX4_P	Control	E31	GND	Control	F31	MEZZ_F1_P	Control	G31	GND	Control	H31	DP_REFCLK_P	31
32		A32	GND		B32	DP_LANE1_N		C32	GND		D32	1000BASEX-TX4_N		E32	GND		F32	MEZZ_F2_N		G32	H32		32		
33		A33	1000BASEX-TX2_P		B33	GND		C33	1000BASEX-TX3_P		D33	GND		E33	USB2SS_TX_P		F33	GND		G33	H33		33		
34		A34	1000BASEX-TX2_N		B34	GND		C34	1000BASEX-TX3_N		D34	GND		E34	USB2SS_TX_N		F34	GND		G34	H34		34		
35		A35	GND		B35	DP_LANE2_P		C35	GND		D35	1000BASEX-RX4_P		E35	GND		F35	MEZZ_F2_P		G35	H35		35		
36		A36	GND		B36	DP_LANE2_N		C36	GND		D36	1000BASEX-RX4_N		E36	GND		F36	MEZZ_F2_N		G36	H36		36		
37	Overlay	A37	VA7230_I2C_SDA	Overlay	B37	GND	Overlay	C37	1000BASEX-RX3_P	Overlay	D37	GND	Overlay	E37	USB2SS_RX_P	Overlay	F37	GND	Overlay	G37	MEZZ_G2_P	Overlay	H37	GND	37
38		A38	VA7230_I2C_SCL		B38	GND		C38	1000BASEX-RX3_N		D38	GND		E38	USB2SS_RX_N		F38	GND		G38	H38		38		
39		A39	GND		B39	DP_LANE3_P		C39	GND		D39	DP_LANE0_P		E39	GND		F39	USB2_D_P		G39	H39		39		
40		A40	GND		B40	DP_LANE3_N		C40	GND		D40	DP_LANE0_N		E40	GND		F40	USB2_D_N		G40	H40		40		
41		A41	USB1SS_TX_P		B41	GND		C41	VA7230_GPIO4		D41	GND		E41	MEZZ_E2_P		F41	GND		G41	H41		41		
42		A42	USB1SS_TX_N		B42	GND		C42	VA7230_GPIO5		D42	GND		E42	MEZZ_E2_N		F42	GND		G42	H42		42		
43	Control	A43	GND	Control	B43	VA7230_GPIO0	Control	C43	GND	Control	D43	MEZZ_D3_P	Control	E43	GND	Control	F43	MEZZ_F3_P	Control	G43	MEZZ_G3_P	Control	H43	MEZZ_H3_P	43
44		A44	GND		B44	VA7230_GPIO1		C44	GND		D44	MEZZ_D3_N		E44	GND		F44	MEZZ_F3_N		G44	H44		44		
45		A45	USB1SS_RX_P		B45	GND		C45	MEZZ_C3_P		D45	GND		E45	MEZZ_E3_P		F45	GND		G45	H45		45		
46		A46	USB1SS_RX_N		B46	GND		C46	MEZZ_C3_N		D46	GND		E46	MEZZ_E3_N		F46	GND		G46	H46		46		
47		A47	GND		B47	VA7230_GPIO2		C47	GND		D47	MEZZ_D4_P		E47	GND		F47	GPLVDS2_P		G47	H47		47		
48		A48	GND		B48	VA7230_GPIO3		C48	GND		D48	MEZZ_D4_N		E48	GND		F48	GPLVDS2_N		G48	H48		48		
49	Control	A49	1000BASEX-RX2_P	Control	B49	GND	Control	C49	MEZZ_C4_P	Control	D49	GND	Control	E49	MEZZ_E4_P	Utility	F49	GND	Utility	G49	MEZZ_G5_P	Utility	H49	GND	49
50		A50	1000BASEX-RX2_N		B50	GND		C50	MEZZ_C4_N		D50	GND		E50	MEZZ_E4_N		F50	GND		G50	H50		50		

Color Key	
Discretetes	
Ethernet	
PCIE	
LVDS	
USB	
Open	
Power	

Table 6. P1 Connector Part Number and Manufacturer (Module)

Connector	Position	Part Number	Vendor
Backplane P1 (Module)	P1	ASP-232975-01	Samtec

Table 7. J1 Connector Part Number and Manufacturer (Backplane)

Connector	Position	Part Number	Vendor
Backplane J1(Backplane)	J1	ASP-232974-01	Samtec

Backplane Pin list / Cross Reference

Table 8. P1 400-pin Backplane Connector, ROW A

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW A	Expansion	A1	EP1_RX0_P	PCIE1_LN0_RX_P
2	ROW A	Expansion	A2	EP1_RX0_N	PCIE1_LN0_RX_N
3	ROW A	Expansion	A3	GND	GND
4	ROW A	Expansion	A4	GND	
5	ROW A	Expansion	A5	EP1_RX1_P	PCIE2_LN0_RX_P
6	ROW A	Expansion	A6	EP1_RX1_N	PCIE2_LN0_RX_N
7	ROW A	Data	A7	GND	GND
8	ROW A	Data	A8	GND	
9	ROW A	Data	A9	DP1_RX0_P	Ethernet1_DA_P
10	ROW A	Data	A10	DP1_RX0_N	Ethernet1_DA_N
11	ROW A	Data	A11	GND	GND
12	ROW A	Data	A12	GND	GND
13	ROW A	Control	A13	CP1_RX0_P	1000BASEX-RX1_P
14	ROW A	Control	A14	CP1_RX0_N	1000BASEX-RX1_N
15	ROW A	Control	A15	GND	GND
16	ROW A	Control	A16	GND	GND
17	ROW A	Control	A17	CP1_TX0_P	1000BASEX-TX1_P
18	ROW A	Control	A18	CP1_TX0_N	1000BASEX-TX1_N
19	ROW A	Expansion	A19	GND	GND
20	ROW A	Expansion	A20	GND	GND
21	ROW A	Expansion	A21	EP1_TX0_P	PCIE1_LN0_TX_P
22	ROW A	Expansion	A22	EP1_TX0_N	PCIE1_LN0_TX_N
23	ROW A	Expansion	A23	GND	GND
24	ROW A	Expansion	A24	GND	GND
25	ROW A	Data	A25	DP1_TX0_P	Ethernet2_DA_P
26	ROW A	Data	A26	DP1_TX0_N	Ethernet2_DA_N
27	ROW A	Data	A27	GND	GND
28	ROW A	Data	A28	GND	GND
29	ROW A	Data	A29	DP1_TX1_P	Ethernet1_DB_P
30	ROW A	Data	A30	DP1_TX1_N	Ethernet1_DB_N
31	ROW A	Control	A31	GND	GND
32	ROW A	Control	A32	GND	GND
33	ROW A	Control	A33	CP2_TX0_P	1000BASEX-TX2_P
34	ROW A	Control	A34	CP2_TX0_N	1000BASEX-TX2_N

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
35	ROW A	Overlay	A35	GND	GND
36	ROW A	Overlay	A36	GND	GND
37	ROW A	Overlay	A37	MEZZ_A1_P	VA7230_I2C_SDA
38	ROW A	Overlay	A38	MEZZ_A1_N	VA7230_I2C_SCL
39	ROW A	Overlay	A39	GND	GND
40	ROW A	Overlay	A40	GND	GND
41	ROW A	Overlay	A41	USB1SS_TX_P	USB1SS_TX_P
42	ROW A	Overlay	A42	USB1SS_TX_N	USB1SS_TX_N
43	ROW A	Overlay	A43	GND	GND
44	ROW A	Overlay	A44	GND	GND
45	ROW A	Overlay	A45	USB1SS_RX_P	USB1SS_RX_P
46	ROW A	Overlay	A46	USB1SS_RX_N	USB1SS_RX_N
47	ROW A	Control	A47	GND	GND
48	ROW A	Control	A48	GND	GND
49	ROW A	Control	A49	CP2_RX0_P	1000BASEX-RX2_P
50	ROW A	Control	A50	CP2_RX0_N	1000BASEX-RX2_N

Table 9. P1 400-pin Backplane Connector, ROW B

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW B	Expansion	B1	GND	GND
2	ROW B	Expansion	B2	GND	GND
3	ROW B	Expansion	B3	EP1_RX2_P	PCIE2_LN1_RX_P
4	ROW B	Expansion	B4	EP1_RX2_N	PCIE2_LN1_RX_P
5	ROW B	Expansion	B5	GND	GND
6	ROW B	Expansion	B6	GND	GND
7	ROW B	Data	B7	DP1_RX1_P	Ethernet1_DB_P
8	ROW B	Data	B8	DP1_RX1_N	Ethernet1_DB_N
9	ROW B	Data	B9	GND	GND
10	ROW B	Data	B10	GND	GND
11	ROW B	Data	B11	DP1_RX2_P	Ethernet1_DC_P
12	ROW B	Data	B12	DP1_RX2_N	Ethernet1_DC_N
13	ROW B	Utility	B13	GND	GND
14	ROW B	Utility	B14	GND	GND
15	ROW B	Utility	B15	SMA_SCL	SMA_SCL
16	ROW B	Utility	B16	SMA_SDA	SMA_SDA
17	ROW B	Expansion	B17	GND	GND
18	ROW B	Expansion	B18	GND	GND
19	ROW B	Expansion	B19	EP1_TX1_P	PCIE2_LN0_TX_P
20	ROW B	Expansion	B20	EP1_TX1_N	PCIE2_LN0_TX_N
21	ROW B	Expansion	B21	GND	GND
22	ROW B	Expansion	B22	GND	GND
23	ROW B	Expansion	B23	EP1_TX2_P	PCIE2_LN1_TX_P
24	ROW B	Expansion	B24	EP1_TX2_N	PCIE2_LN1_TX_N
25	ROW B	Data	B25	GND	GND
26	ROW B	Data	B26	GND	GND
27	ROW B	Data	B27	DP1_TX2_P	Ethernet2_DC_P
28	ROW B	Data	B28	DP1_TX2_N	Ethernet2_DC_N
29	ROW B	Data	B29	GND	GND
30	ROW B	Data	B30	GND	GND
31	ROW B	Overlay	B31	VID1_D1_P	DP_LANE0_P
32	ROW B	Overlay	B32	VID1_D1_N	DP_LANE0_N
33	ROW B	Overlay	B33	GND	GND
34	ROW B	Overlay	B34	GND	GND
35	ROW B	Overlay	B35	VID1_D2_P	DP_LANE1_P
36	ROW B	Overlay	B36	VID1_D2_N	DP_LANE1_N

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
37	ROW B	Overlay	B37	GND	GND
38	ROW B	Overlay	B38	GND	GND
39	ROW B	Overlay	B39	VID1_D3_P	DP_LANE3_P
40	ROW B	Overlay	B40	VID1_D3_N	DP_LANE4_N
41	ROW B	Overlay	B41	GND	GND
42	ROW B	Overlay	B42	GND	GND
43	ROW B	Overlay	B43	MEZZ_B3_P	VA7230_GPIO0
44	ROW B	Overlay	B44	MEZZ_B3_N	VA7230_GPIO1
45	ROW B	Overlay	B45	GND	GND
46	ROW B	Overlay	B46	GND	GND
47	ROW B	Overlay	B47	MEZZ_B4_P	VA7230_GPIO2
48	ROW B	Overlay	B48	MEZZ_B4_N	VA7230_GPIO3
49	ROW B	Overlay	B49	GND	GND
50	ROW B	Overlay	B50	GND	GND

Table 10. P1 400-pin Backplane Connector, ROW C

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW C	Expansion	C1	EP1_RX3_P	EP1_RX3_P (N/C)
2	ROW C	Expansion	C2	EP1_RX3_N	EP1_RX3_N (N/C)
3	ROW C	Expansion	C3	GND	GND
4	ROW C	Expansion	C4	GND	GND
5	ROW C	Expansion	C5	EP1_RX4_P	EP1_RX4_P (N/C)
6	ROW C	Expansion	C6	EP1_RX4_N	EP1_RX4_N (N/C)
7	ROW C	Data	C7	GND	GND
8	ROW C	Data	C8	GND	GND
9	ROW C	Data	C9	DP1_RX3_P	Ethernet1_DD_P
10	ROW C	Data	C10	DP1_RX3_N	Ethernet1_DD_N
11	ROW C	Data	C11	GND	GND
12	ROW C	Data	C12	GND	GND
13	ROW C	Utility	C13	SMB_SCL	SMB_SCL
14	ROW C	Utility	C14	SMB_SDA	SMB_SDA
15	ROW C	Utility	C15	GND	GND
16	ROW C	Utility	C16	GND	GND
17	ROW C	Expansion	C17	EP1_TX3_P	EP1_TX3_P (N/C)
18	ROW C	Expansion	C18	EP1_TX3_N	EP1_TX3_N (N/C)
19	ROW C	Expansion	C19	GND	GND
20	ROW C	Expansion	C20	GND	GND
21	ROW C	Expansion	C21	EP1_TX4_P	EP1_TX4_P (N/C)
22	ROW C	Expansion	C22	EP1_TX4_N	EP1_TX4_N (N/C)
23	ROW C	Expansion	C23	GND	GND
24	ROW C	Expansion	C24	GND	GND
25	ROW C	Data	C25	DP1_TX3_P	Ethernet2_DD_P
26	ROW C	Data	C26	DP1_TX3_N	Ethernet2_DD_N
27	ROW C	Data	C27	GND	GND
28	ROW C	Data	C28	GND	GND
29	ROW C	Data	C29	DP2_TX0_P	Ethernet4_DA_P
30	ROW C	Data	C30	DP2_TX0_N	Ethernet4_DA_N
31	ROW C	Overlay	C31	GND	GND
32	ROW C	Overlay	C32	GND	GND
33	ROW C	Overlay	C33	PP1_TX1_P	1000BASEX-TX3_P
34	ROW C	Overlay	C34	PP1_TX1_N	1000BASEX-TX3_N
35	ROW C	Overlay	C35	GND	GND
36	ROW C	Overlay	C36	GND	GND

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
37	ROW C	Overlay	C37	PP1_RX1_P	1000BASEX-RX3_P
38	ROW C	Overlay	C38	PP1_RX1_N	1000BASEX-RX3_N
39	ROW C	Overlay	C39	GND	GND
40	ROW C	Overlay	C40	GND	GND
41	ROW C	Overlay	C41	MEZZ_C2_P	VA7230_GPIO4
42	ROW C	Overlay	C42	MEZZ_C2_N	VA7230_GPIO5
43	ROW C	Overlay	C43	GND	GND
44	ROW C	Overlay	C44	GND	GND
45	ROW C	Overlay	C45	MEZZ_C3_P	MEZZ_C3_P (N/C)
46	ROW C	Overlay	C46	MEZZ_C3_N	MEZZ_C3_N (N/C)
47	ROW C	Overlay	C47	GND	GND
48	ROW C	Overlay	C48	GND	GND
49	ROW C	Overlay	C49	MEZZ_C4_P	MEZZ_C4_P (N/C)
50	ROW C	Overlay	C50	MEZZ_C4_N	MEZZ_C4_N (N/C)

Table 11. P1 400-pin Backplane Connector, ROW D

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBCA72-VNXP Name
1	ROW D	Expansion	D1	GND	GND
2	ROW D	Expansion	D2	GND	GND
3	ROW D	Expansion	D3	EP1_RX5_P	EP1_RX5_P (N/C)
4	ROW D	Expansion	D4	EP1_RX5_N	EP1_RX5_N (N/C)
5	ROW D	Expansion	D5	GND	GND
6	ROW D	Expansion	D6	GND	GND
7	ROW D	Data	D7	DP2_RX0_P	Ethernet3_DA_P
8	ROW D	Data	D8	DP2_RX0_N	Ethernet3_DA_N
9	ROW D	Data	D9	GND	GND
10	ROW D	Data	D10	GND	GND
11	ROW D	Data	D11	DP2_RX1_P	Ethernet3_DB_P
12	ROW D	Data	D12	DP2_RX1_N	Ethernet3_DB_N
13	ROW D	Utility	D13	GND	GND
14	ROW D	Utility	D14	GND	GND
15	ROW D	Utility	D15	MP1_RXD	S0_UART_RX
16	ROW D	Utility	D16	MP1_TXD	S0_UART_TX
17	ROW D	Expansion	D17	GND	GND
18	ROW D	Expansion	D18	GND	GND
19	ROW D	Expansion	D19	EP1_TX5_P	EP1_TX5_P (N/C)
20	ROW D	Expansion	D20	EP1_TX5_N	EP1_TX5_N (N/C)
21	ROW D	Expansion	D21	GND	GND
22	ROW D	Expansion	D22	GND	GND
23	ROW D	Expansion	D23	EP1_TX6_P	EP1_TX6_P (N/C)
24	ROW D	Expansion	D24	EP1_TX6_N	EP1_TX6_N (N/C)
25	ROW D	Data	D25	GND	GND
26	ROW D	Data	D26	GND	GND
27	ROW D	Data	D27	DP2_TX1_P	Ethernet4_DB_P
28	ROW D	Data	D28	DP2_TX1_N	Ethernet4_DB_N
29	ROW D	Data	D29	GND	GND
30	ROW D	Data	D30	GND	GND
31	ROW D	Overlay	D31	PP1_TX2_P	1000BASEX-TX4_P
32	ROW D	Overlay	D32	PP1_TX2_N	1000BASEX-TX4_N
33	ROW D	Overlay	D33	GND	GND
34	ROW D	Overlay	D34	GND	GND
35	ROW D	Overlay	D35	PP1_RX2_P	1000BASEX-RX4_P
36	ROW D	Overlay	D36	PP1_RX2_N	1000BASEX-RX4_N

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBCA72-VNXP Name
37	ROW D	Overlay	D37	GND	GND
38	ROW D	Overlay	D38	GND	GND
39	ROW D	Overlay	D39	VID1_D0_P	DP_LANE0_P
40	ROW D	Overlay	D40	VID1_D0_N	DP_LANE0_N
41	ROW D	Overlay	D41	GND	GND
42	ROW D	Overlay	D42	GND	GND
43	ROW D	Overlay	D43	MEZZ_D3_P	MEZZ_D3_P (N/C)
44	ROW D	Overlay	D44	MEZZ_D3_N	MEZZ_D3_N (N/C)
45	ROW D	Overlay	D45	GND	GND
46	ROW D	Overlay	D46	GND	GND
47	ROW D	Overlay	D47	MEZZ_D4_P	MEZZ_D4_P (N/C)
48	ROW D	Overlay	D48	MEZZ_D4_N	MEZZ_D4_N (N/C)
49	ROW D	Overlay	D49	GND	GND
50	ROW D	Overlay	D50	GND	GND

Table 12. 400-pin Connector, ROW E

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBCA72-VNXP Name
1	ROW E	Expansion	E1	EP1_RX6_P	EP1_RX6_P (N/C)
2	ROW E	Expansion	E2	EP1_RX6_N	EP1_RX6_N (N/C)
3	ROW E	Expansion	E3	GND	GND
4	ROW E	Expansion	E4	GND	GND
5	ROW E	Expansion	E5	EP1_RX7_P	EP1_RX7_P (N/C)
6	ROW E	Expansion	E6	EP1_RX7_N	EP1_RX7_N (N/C)
7	ROW E	Data	E7	GND	GND
8	ROW E	Data	E8	GND	GND
9	ROW E	Data	E9	DP2_RX2_P	Ethernet3_DC_P
10	ROW E	Data	E10	DP2_RX2_N	Ethernet3_DC_N
11	ROW E	Data	E11	GND	GND
12	ROW E	Data	E12	GND	GND
13	ROW E	Data	E13	DP2_RX3_P	Ethernet3_DD_P
14	ROW E	Data	E14	DP2_RX3_N	Ethernet3_DD_N
15	ROW E	Utility	E15	GND	GND
16	ROW E	Utility	E16	GND	GND
17	ROW E	Utility	E17	REFCLK_P	REFCLK_P
18	ROW E	Utility	E18	REFCLK_N	REFCLK_N
19	ROW E	Expansion	E19	GND	GND
20	ROW E	Expansion	E20	GND	GND
21	ROW E	Expansion	E21	EP1_TX7_P	EP1_TX7_P (N/C)
22	ROW E	Expansion	E22	EP1_TX7_N	EP1_TX7_N (N/C)
23	ROW E	Expansion	E23	GND	GND
24	ROW E	Expansion	E24	GND	GND
25	ROW E	Data	E25	GND	Ethernet4_DC_P
26	ROW E	Data	E26	GND	Ethernet4_DC_N
27	ROW E	Data	E27	DP2_TX1_P	GND
28	ROW E	Data	E28	DP2_TX1_N	GND
29	ROW E	Data	E29	GND	Ethernet4_DD_P
30	ROW E	Data	E30	GND	Ethernet4_DD_N
31	ROW E	Overlay	E31	GND	GND
32	ROW E	Overlay	E32	GND	GND
33	ROW E	Overlay	E33	USB2SS_TX_P	USB2SS_TX_P
34	ROW E	Overlay	E34	USB2SS_TX_N	USB2SS_TX_N
35	ROW E	Overlay	E35	GND	GND
36	ROW E	Overlay	E36	GND	GND

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBCA72-VNXP Name
37	ROW E	Overlay	E37	USB2SS_RX_P	USB2SS_RX_P
38	ROW E	Overlay	E38	USB2SS_RX_N	USB2SS_RX_N
39	ROW E	Overlay	E39	GND	GND
40	ROW E	Overlay	E40	GND	GND
41	ROW E	Overlay	E41	MEZZ_E2_P	MEZZ_E2_P (N/C)
42	ROW E	Overlay	E42	MEZZ_E2_N	MEZZ_E2_N (N/C)
43	ROW E	Overlay	E43	GND	GND
44	ROW E	Overlay	E44	GND	GND
45	ROW E	Overlay	E45	MEZZ_E3_P	MEZZ_E3_P (N/C)
46	ROW E	Overlay	E46	MEZZ_E3_N	MEZZ_E3_N (N/C)
47	ROW E	Overlay	E47	GND	GND
48	ROW E	Overlay	E48	GND	GND
49	ROW E	Overlay	E49	MEZZ_E4_P	MEZZ_E4_P (N/C)
50	ROW E	Overlay	E50	MEZZ_E4_N	MEZZ_E4_N (N/C)

Table 13. P1 400-pin Backplane Connector, ROW F

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW F	Utility	F1	EP1_RX6_P	GND
2	ROW F	Utility	F2	EP1_RX6_N	GND
3	ROW F	Utility	F3	GND	GBE1_MDI0_P (N/C)
4	ROW F	Utility	F4	GND	GBE1_MDI0_N (N/C)
5	ROW F	Utility	F5	EP1_RX7_P	GND
6	ROW F	Utility	F6	EP1_RX7_N	GND
7	ROW F	Utility	F7	GND	GBE1_MDI1_P (N/C)
8	ROW F	Utility	F8	GND	GBE1_MDI1_N (N/C)
9	ROW F	Utility	F9	DP2_RX2_P	GND
10	ROW F	Utility	F10	DP2_RX2_N	GND
11	ROW F	Utility	F11	GND	GBE1_MDI2_P (N/C)
12	ROW F	Utility	F12	GND	GBE1_MDI2_N (N/C)
13	ROW F	Utility	F13	DP2_RX3_P	GND
14	ROW F	Utility	F14	DP2_RX3_N	GND
15	ROW F	Utility	F15	GND	GBE1_MDI3_P (N/C)
16	ROW F	Utility	F16	GND	GBE1_MDI3_N (N/C)
17	ROW F	Utility	F17	REFCLK_P	GND
18	ROW F	Utility	F18	REFCLK_N	GND
19	ROW F	Utility	F19	GND	AUXCLK_P
20	ROW F	Utility	F20	GND	AUXCLK_N
21	ROW F	Utility	F21	EP1_TX7_P	GND
22	ROW F	Utility	F22	EP1_TX7_N	GND
23	ROW F	Utility	F23	GND	USB1_D_P
24	ROW F	Utility	F24	GND	USB1_D_N
25	ROW F	Utility	F25	GND	GND
26	ROW F	Utility	F26	GND	GND
27	ROW F	Utility	F27	DP2_TX1_P	S0-PCIe_CLK_P
28	ROW F	Utility	F28	DP2_TX1_N	S0-PCIe_CLK_N
29	ROW F	Utility	F29	GND	GND
30	ROW F	Utility	F30	GND	GND
31	ROW F	Overlay	F31	GND	MEZZ_F1_P (N/C)
32	ROW F	Overlay	F32	GND	MEZZ_F2_N (N/C)
33	ROW F	Overlay	F33	USB2SS_TX_P	GND
34	ROW F	Overlay	F34	USB2SS_TX_N	GND
35	ROW F	Overlay	F35	GND	MEZZ_F2_P (N/C)
36	ROW F	Overlay	F36	GND	MEZZ_F2_N (N/C)

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
37	ROW F	Overlay	F37	USB2SS_RX_P	GND
38	ROW F	Overlay	F38	USB2SS_RX_N	GND
39	ROW F	Overlay	F39	GND	USB2_D_P
40	ROW F	Overlay	F40	GND	USB2_D_N
41	ROW F	Overlay	F41	MEZZ_E2_P	GND
42	ROW F	Overlay	F42	MEZZ_E2_N	GND
43	ROW F	Overlay	F43	GND	MEZZ_F3_P (N/C)
44	ROW F	Overlay	F44	GND	MEZZ_F3_N (N/C)
45	ROW F	Overlay	F45	MEZZ_E3_P	GND
46	ROW F	Overlay	F46	MEZZ_E3_N	GND
47	ROW F	Utility	F47	GND	GPLVDS2_P (N/C)
48	ROW F	Utility	F48	GND	GPLVDS2_N (N/C)
49	ROW F	Utility	F49	MEZZ_E4_P	GND
50	ROW F	Utility	F50	MEZZ_E4_N	GND

Table 14. P1 400-pin Backplane Connector, ROW G

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW G	Utility	G1	VS1	VS1 (12V)
2	ROW G	Utility	G2	VS1	VS1 (12V)
3	ROW G	Utility	G3	VS1	VS1 (12V)
4	ROW G	Utility	G4	VS1	VS1 (12V)
5	ROW G	Utility	G5	GND	GND
6	ROW G	Utility	G6	VS2	VS2 (N/C)
7	ROW G	Utility	G7	VS2	VS2 (N/C)
8	ROW G	Utility	G8	VS2	VS2 (N/C)
9	ROW G	Utility	G9	VS2	VS2 (N/C)
10	ROW G	Utility	G10	GND	GND
11	ROW G	Utility	G11	VS3	VS3 (N/C)
12	ROW G	Utility	G12	VS3	VS3 (N/C)
13	ROW G	Utility	G13	VS4	VS4 (N/C)
14	ROW G	Utility	G14	VAUX	3.3 VAUX
15	ROW G	Utility	G15	GND	GND
16	ROW G	Utility	G16	UEIO0	SpaceWire
17	ROW G	Utility	G17	UEIO1	SpaceWire
18	ROW G	Utility	G18	UEIO2	SpaceWire
19	ROW G	Utility	G19	GND	GND
20	ROW G	Utility	G20	UEIO3	SpaceWire
21	ROW G	Utility	G21	UEIO4	SpaceWire
22	ROW G	Utility	G22	UEIO5	SpaceWire
23	ROW G	Utility	G23	GND	GND
24	ROW G	Utility	G24	UEIO6	SpaceWire
25	ROW G	Utility	G25	UEIO7	SpaceWire
26	ROW G	Utility	G26	USB1_VBUS	USB1_VBUS
27	ROW G	Utility	G27	GND	GND
28	ROW G	Utility	G28	GDISCRETE1	GDISCRETE1
29	ROW G	Utility	G29	GPIO1	GPIO1
30	ROW G	Utility	G30	GPIO2	GPIO2
31	ROW G	Overlay	G31	GND	GND
32	ROW G	Overlay	G32	GND	GND
33	ROW G	Overlay	G33	MEZZ_G1_P	MEZZ_G1_P (N/C)
34	ROW G	Overlay	G34	MEZZ_G1_N	MEZZ_G2_N (N/C)
35	ROW G	Overlay	G35	GND	GND
36	ROW G	Overlay	G36	GND	GND

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
37	ROW G	Overlay	G37	MEZZ_G2_P	MEZZ_G2_P (N/C)
38	ROW G	Overlay	G38	MEZZ_G2_N	MEZZ_G2_N (N/C)
39	ROW G	Overlay	G39	GND	GND
40	ROW G	Overlay	G40	GND	GND
41	ROW G	Overlay	G41	MEZZ_G3_P	MEZZ_G3_P (N/C)
42	ROW G	Overlay	G42	MEZZ_G3_N	MEZZ_G3_N (N/C)
43	ROW G	Overlay	G43	GND	GND
44	ROW G	Overlay	G44	GND	GND
45	ROW G	Overlay	G45	MEZZ_G4_P	MEZZ_G4_P (N/C)
46	ROW G	Overlay	G46	MEZZ_G4_N	MEZZ_G4_N (N/C)
47	ROW G	Overlay	G47	GND	GND
48	ROW G	Overlay	G48	GND	GND
49	ROW G	Overlay	G49	MEZZ_G5_P	MEZZ_G5_P (N/C)
50	ROW G	Overlay	G50	MEZZ_G5_N	MEZZ_G5_N (N/C)

Table 15. P1 400-pin Backplane Connector, ROW H

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
1	ROW H	Utility	H1	VS1	VS1 (12V)
2	ROW H	Utility	H2	VS1	VS1 (12V)
3	ROW H	Utility	H3	VS1	VS1 (12V)
4	ROW H	Utility	H4	VS1	VS1 (12V)
5	ROW H	Utility	H5	GND	GND
6	ROW H	Utility	H6	VS2	VS2 (N/C)
7	ROW H	Utility	H7	VS2	VS2 (N/C)
8	ROW H	Utility	H8	VS2	VS2 (N/C)
9	ROW H	Utility	H9	VS2	VS2 (N/C)
10	ROW H	Utility	H10	GND	GND
11	ROW H	Utility	H11	VS3	VS3 (N/C)
12	ROW H	Utility	H12	VS3	VS3 (N/C)
13	ROW H	Utility	H13	VHEATER	VHEATER (N/C)
14	ROW H	Utility	H14	VBAT_3V	VBAT_3V (N/C)
15	ROW H	Utility	H15	GND	GND
16	ROW H	Utility	H16	NVMRO	NVMRO (N/C)
17	ROW H	Utility	H17	SYSRESET*	SYSRESET*
18	ROW H	Utility	H18	GND	GND
19	ROW H	Utility	H19	SER1_RX_P	SER1_RX_P
20	ROW H	Utility	H20	SER1_RX_N	SER1_RX_N
21	ROW H	Utility	H21	SER1_TX_P	SER1_TX_P
22	ROW H	Utility	H22	SER1_TX_N	SER1_TX_N
23	ROW H	Utility	H23	GND	GND
24	ROW H	Utility	H24	GA0*	GA0*
25	ROW H	Utility	H25	GA1*	GA1*
26	ROW H	Utility	H26	GA2*	GA2*
27	ROW H	Utility	H27	GA3*	GA3*
28	ROW H	Utility	H28	GA4*	GA4*
29	ROW H	Utility	H29	GAP*	GAP*
30	ROW H	Utility	H30	GND	GND
31	ROW H	Overlay	H31	VID1_D4_P	CPU_DP_AUX_P
32	ROW H	Overlay	H32	VID1_D4_N	CPU_DP_AUX_P
33	ROW H	Overlay	H33	GND	GND
34	ROW H	Overlay	H34	GND	GND
35	ROW H	Overlay	H35	VID1_D5_P	VID1_D5_P (N/C)
36	ROW H	Overlay	H36	VID1_D5_N	DP_POWER

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	SBC2A72-VNXP Name
37	ROW H	Overlay	H37	GND	GND
38	ROW H	Overlay	H38	GND	
39	ROW H	Overlay	H39	USB2_VBUS	USB2_VBUS (N/C)
40	ROW H	Overlay	H40	RFU	RFU
41	ROW H	Overlay	H41	GND	GND
42	ROW H	Overlay	H42	GND	GND
43	ROW H	Overlay	H43	MEZZ_H2_P	MEZZ_H3_P (N/C)
44	ROW H	Overlay	H44	MEZZ_H2_N	MEZZ_H3_N (N/C)
45	ROW H	Overlay	H45	GND	GND
46	ROW H	Overlay	H46	GND	GND
47	ROW H	Overlay	H47	MEZZ_H3_P	MEZZ_H3_P (N/C)
48	ROW H	Overlay	H48	MEZZ_H3_N	MEZZ_H3_N (N/C)
49	ROW H	Overlay	H49	GND	GND
50	ROW H	Overlay	H50	GND	GND

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX	3.3V Auxiliary Input	3	3.6	Vdc
Pd	Max Power Dissipation		30	W
Storage Temp		-40	+105	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Mass			0.35 (TBC)	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID	Total Ionizing Dose	30K	rad (Si)
nd-SEL Immunity		37	MeV-cm2/mg
Total Single Event Rate Requiring External or Ground Intervention	LEO ISS MEO GEO	6.17E-04 10.7E-03 13.7E-03	Event per year

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@ 70 °C @ 50 °C @ 30 °C	318,894 TBD TBD	hours
Reliability (R)	3 years @ 70°C @ 100 Duty Cycle 5 years @ 70°C @ 100 Duty Cycle 7 years @ 70°C @ 100 Duty Cycle	0.872 0.825 0.719	

Acceptance Testing (FM3 Class C and FM4 Class D)

Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	

Qualification Testing

Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles
Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Functional Description

The Frontgrade™ SBC2A72-VNXP is a compact, radiation-tolerant single board computer designed to provide high-performance computing, graphics processing, networking, and system management capabilities for mission-critical harsh-environment applications. Implemented as a 19 mm VITA 90.0 VNX+ plug-in module, it delivers an optimized balance of Size, Weight, Power, and Cost (SWaP-C) while supporting demanding edge-computing and onboard data-processing requirements.

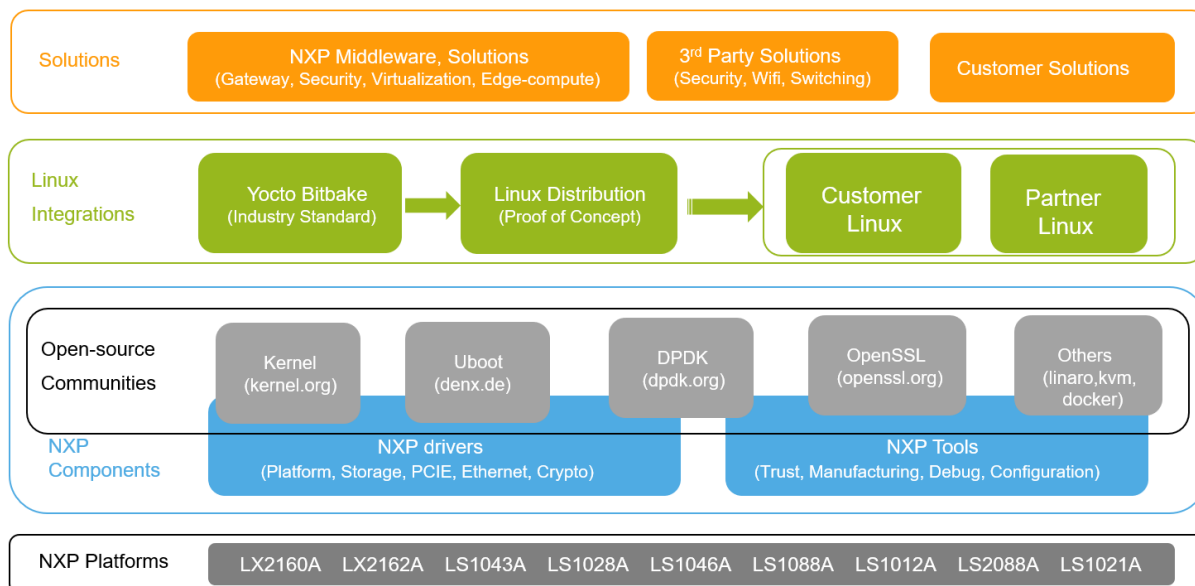
At the core of the SBC is the Vorago VA7230 dual-core ARM® Cortex®-A72 processor with an integrated Graphics Processing Unit (GPU), providing up to 10.4 GFLOPs of processing performance. This architecture enables execution of command and data handling functions, onboard payload processing, image and graphics processing, autonomous decision-making, and high-throughput communications tasks.

The SBC incorporates extensive memory resources and a broad range of communications interfaces to support data-intensive applications. Networking, telemetry, command and control, graphics, and payload data are routed through the VNX+ backplane interface, eliminating reliance on operational front-panel connections and simplifying integration.

A radiation-hardened microcontroller unit (MCU) provides platform management functions including health monitoring, power management, and coordination of system resources across multiple plug-in modules within a larger VNX+ architecture. The MCU also extends system connectivity by providing additional UART, SpaceWire, and GPIO interfaces.

Designed for operation in harsh environments, the SBC2A72-VNXP serves as a central processing element for command and data handling, robotic missions, payload processing platforms, and networking and communications architectures. Its combination of processing performance, radiation tolerance, extensive I/O capability, and compact form factor enables advanced autonomy and high-reliability mission operations.

Software Ecosystem



Features

Layerscape LDP Components

- Freely available
 - Download from public repositories (e.g. github.com)
 - No need to download a large ISO and extract
- Modularized
 - Boot-loaders, Kernels, User-space libraries, Tools, Configuration
 - Pick and choose ones you need
- Clean layering, separation
 - Separate patches on top of open source
 - Patches identified by platform/IP
- Easy updates via Git
 - Periodic releases and interim updates
 - Support for two recent LTS kernels

Layerscape LDP

- Easy boot mechanisms
 - Boot from multiple sources
 - Simple, quick updates from any mass-storage
 - Brick-proof mechanism* - easy recovery via SD
- Easy runtime upgrades
 - Rich LDP user-land and repositories
 - On-the-fly install with apt-get
 - Build/install from source on target
- Latest and greatest
 - Latest Layerscape platforms
 - Latest drivers and features
 - Layerscape specific tools, drivers

What's New In L6.1.1-1.0.0-LLDP

- NXP Layerscape LDP userland:
 - NXP Layerscape LDP, including Linux distro main packages and NXP packages
- Toolchain: gcc-11.2, glibc-2.36, binutils-2.38, gdb-12.1
- Linux kernel core and virtualization:
 - LTS kernel 6.1.1 update
- Linux kernel drivers:
 - Data Plane Development Kit (DPDK):
 - Virtualization - OVS-DPDK
- U-Boot bootloader:
 - U-Boot v2022.04 update
 - AQR113C on TWR-LS1021A, LS1088ARDB, and LX2162AQDS
- Other tools and utilities:
 - AQR113C firmware
 - Yocto bitbake

Mechanical Drawing

To Be Added

Revision History

Date	Rev	Author	Change Description	Page #
5/29/2026	1.0	DPA	Initial Preliminary Datasheet	All

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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