



FRONTGRADE

PRELIMINARY DATASHEET

SBC2A72-SVPX

Dual-Core ARM Cortex-A72 with GPU
SpaceVPX Single Board Computer

5/27/2026
Version #: 1.0



Introduction

The Frontgrade™ SBC2A72-SVPX Single Board Computer provides a compelling mix of high-performance processing and interface capability, in low power SWaP optimized design. Implemented a 3U-160mm SpaceVPX form factor, the SBC is ideal for on-board computing, payload computing, and graphics processing applications. This compact 3U design is small, lightweight, and power efficient while offering a strong combination of compute and graphics processing capability along with a strong mix of interfaces.

The Frontgrade SBC2A72-SVPX features the power efficient and radiation tolerant Vorago VA7230 Dual ARM® Cortex®-A72 processor with integrated Graphics Processing Unit (GPU) capable of 10.4 GFLOPs performance that is ideal for image processing and AI acceleration. Adding to the processing capabilities of the VA7230, the SBC provides a flexible complement of communications and interface protocols to support high-throughput networking, graphics, command, control, and telemetry in conjunction with extensive memory facilities.

Moreover, to address the wide mix of I/O interfaces required by different applications, the SBC2A72-SVPX integrates a companion CertusPro-NX-RT FPGA and XMC+ I/O expansion mezzanine interface. Leveraging the local FPGA and XMC+ interface, applications can implement additional I/O solutions optimized for their unique requirements without customizing the main SBC hardware. The FPGA currently implements a PCIe to SpaceFibre interface.

Finally, the SBC2A72-SVPX includes a radiation hardened MCU (VA41630, ARM Cortex-M4) which provides, among other things, system management between plug-in modules integrated into a larger system as well as local monitoring and power management to elements local to the SBC. Additionally, the MCU expands the interfaces to the system backplane in the form of UARTs, SpaceWire, and GPIO.

Applications

- Onboard Payload Processing
- Secure Command and Control
- AI and Edge Computing in Space
- Graphics and Human-Machine Interfaces

Why it Matters

The Frontgrade™ SBC2A72-SVPX delivers high-performance processing, graphics acceleration, and flexible I/O expansion in a compact, low-power 3U SpaceVPX platform optimized for demanding missions. Its radiation-tolerant architecture enables reliable onboard computing for AI, image processing, autonomy, and command-and-control applications in harsh environments. Integrated FPGA and XMC+ expansion capabilities allow mission-specific customization without redesigning the core SBC. By combining compute power, interface flexibility, and SWaP efficiency, the SBC2A72-SVPX helps reduce integration complexity, development risk, and overall system cost for next-generation platforms.

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
SBC2A72-SVPX-OP-EDU	EDU = EDU/EM (Room Temp only)	Lab / Development Use Cases
SBC2A72-SVPX-OP-FM4	COTS Parts Grade (-10°C to +50°C)	Target Mission Class D
SBC2A72-SVPX-OP-FM3	Level 3 Parts Grade (-10°C to +50°C)	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds.

Features

Processing Performance

- Based on Vorago VA7230 Processor (NXP LS1028A) with GPU Acceleration
 - Two 32/64-bit ARM® Cortex®-A72 cores with the following capabilities:
 - ~15K DMIPS performance at 1.5 GHz operation
 - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache
 - Single cluster of two cores sharing 1MB L2 cache
 - Graphics processing unit
 - Supports Geometry rate 100 Mtri/sec
 - Pixel rate 650 Mpixel/sec
 - 10.4 GFLOPS (32-bit high precision)
 - Supports OpenGL ES 3.0, 2.0, 1.1
 - Supports OpenCL 1.1, 1.2

User Memory

- 8GB + ECC DDR4 (x36 bus width)
 - 1600 MT/s
- Apps and Storage
 - 32GB e.MMC 5.1
 - Supports enhanced Secure Digital Host Controller (eSDHC)
 - Optional: 1Gb-8Gb DQSPI MRAM

Mass & Thermal

- Mass: <0.65 kg
- 3U Form Factor: 160mm x 100mm / 1.0" Pitch
- -10°C to +50°C operational case temperature
- Power consumption: <15W Typical / 30W Max
- TID: Up to 30k rad (Si)
- SEL Immune <= 37MeV

Debug Interfaces

- MCU JTAG, Debug UART, Reset and 2 GPIO
- CPU JTAG, Debug UART, Reset and 2 GPIO
- FPGA JTAG, Debug UART, Programming, and LEDs
- CPU Debug Reset

Security Features

- Secure boot
- Security Engine
- Arm TrustZone™

Backplane Interfaces

(VITA 78.0 Profile: SLT3-PAY-2F2T1Q-14.2.1)

- 4x GbE ports
 - 2x TSN 1GbE (SGMII)
 - 2x 1000Base-X (with magnetics)
- 1x PCIe 3.0 x1 port
- 1x USB 3.0 Interface
- 1x DisplayPort Out
 - DisplayPort 1.3 and eDP 1.4
- 6x GPIO + 2x GPIO/I2C, from CPU
- 4x GPIO, from FPGA
- 1x PPS Input
- 1x UART
- 1x SpW

Backplane Utility Segment

- 5x GA + 1x GA Parity
- SYSRESET*
- 1x I2C + SM_STAT* & SM_RESET*
- 1x LVDS REFCLK Input (100MHz)
- 1x LVDS AUXCLK, PPS
- 12V VS1
- 3.3V_AUX (Build Option)

Software

The SBC2A72-SVPX is supported by a SDK/BSP which offers Linux based off the NXP LS1028A layerscape distribution:

- [NXP Layerscape Software](#)

The NXP Middleware and additional 3rd Party Solutions are available. Please contact your local Frontgrade sales representative for additional information.

Block Diagram

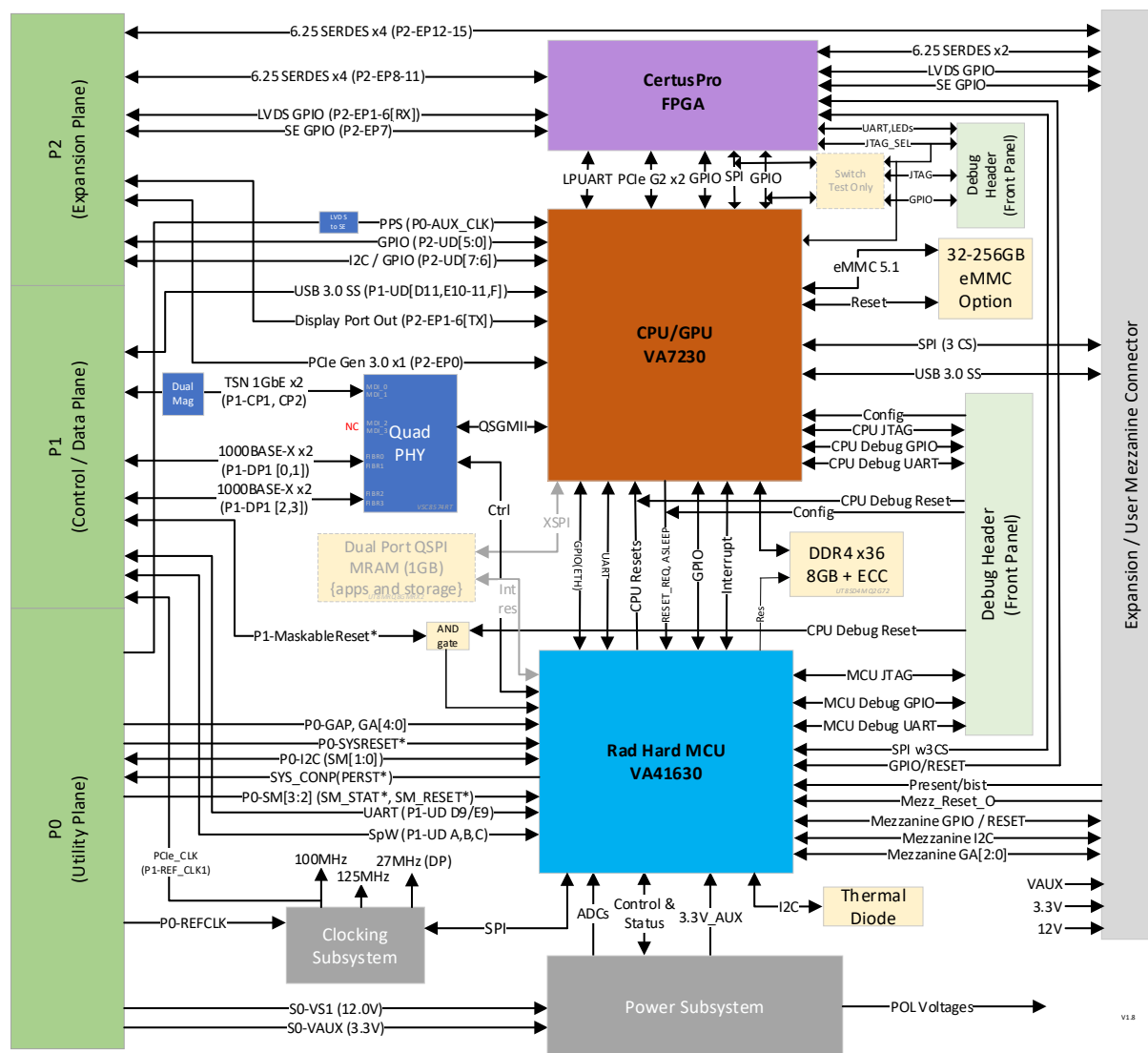


Figure 1. SBC2A72-SVPX High Level Block Diagram

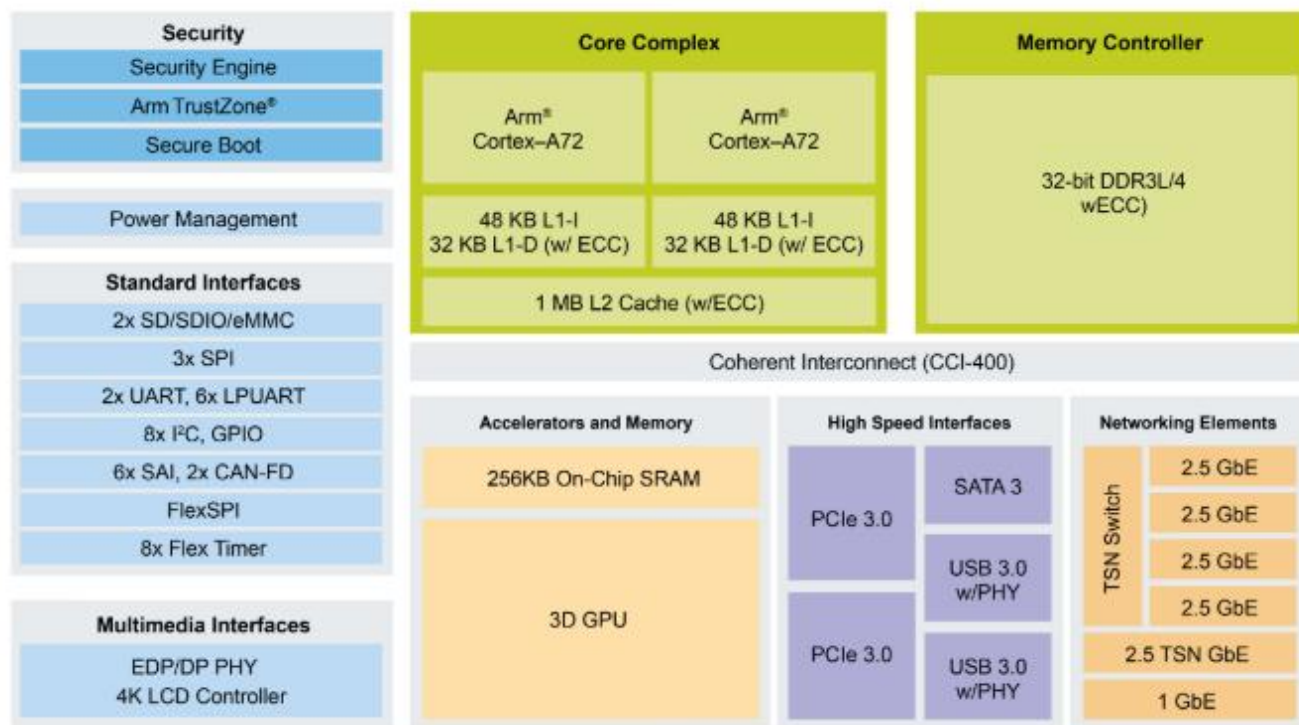


Figure 2. VA7230 Processor High Level Block Diagram

Debug Connector Interfaces

The SBC2A72-SPVX provides a two Debug Interfaces to the front side of the plug-in module. The main debug interface is for the VA7230 CPU and VA41630 MCU.

The other Debug Interface is for the CertusPro FPGA which is described in table 2.

The debug interfaces are only intended for ground/lab level testing and pre-flight configuration of the SBC software.

Table 1. J1 and J2 Connector Part Number and Manufacturer

Connector	Position	Part Number	Vendor
40-Pin Front Panel	J1	LSHM-120-01-F-DH-A-S-K-TR	SAMTEC
20-Pin Front Panel	J2	LSHM-110-01-F-DH-A-S-K-TR	SAMTEC

J1: 40-pin Front Panel Debug Connector

Table 2. J1 Debug Connector Pin list

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	MCU_JTAG_TRSTN	2	SE Input	CPU_JTAG_TRSTN
3	SE Input	MCU_JTAG_TCK	4	SE Input	CPU_JTAG_TCK
5	SE Input	MCU_JTAG_TMS	6	SE Input	CPU_JTAG_TMS
7	SE Input	MCU_JTAG_TDI	8	SE Input	CPU_JTAG_TDI
9	SE Output	MCU_JTAG_TDO	10	SE Output	CPU_JTAG_TDO
11	PWR	GND	12	PWR	GND
13	SE Input	MCU_RESET	14	SE Input	CPU_RESET
15	SE Input	MCU_UART_RX	16	SE Input	CPU_UART_RX
17	SE Input	MCU_UART_TX	18	SE Input	CPU_UART_TX
19	SE Input	MCU_GPIO_LED0	20	SE Input	CPU_GPIO_LED0
21	SE Output	MCU_GPIO_LED1	22	SE Output	CPU_GPIO_LED1
23	PWR	GND	24	PWR	GND
25	SE In/Out	SDHC2_DAT0	26	SE In/Out	SDHC2_DAT2
27	SE In/Out	SDHC2_DAT1	28	SE In/Out	SDHC2_DAT3
29	SE Input	SDHC2_CMD	30	SE Input	MCU_CPU_ASLEEP
31	SE Input	SDHC2_CLK	32	SE Input	MCU_CPU_UART_RX
33	PWR	GND	34	PWR	GND
35	NC	NC	36	SE Output	CPU_CLK_OUT
37	PWR	1.8V	38	SE Output	CPU_TA_PROG
39	PWR	GND	40		GND

J2: 20-pin Front Panel Debug Connector

Table 3. J2 FPGA Debug Connector Pin list

Pin #	Type	Signal Name	Pin #	Type	Signal Name
1	SE Input	FPGA_JTAG_TCK	2	SE Input	FPGA_RESET
3	SE Input	FPGA_JTAG_TMS	4	SE Input	FPGA_UART_RX
5	SE Input	FPGA_JTAG_TDI	6	SE Output	FPGA_UART_TX
7	SE Output	FPGA_JTAG_TDO	8	SE Input	JTAG_SELECT
9	PWR	GND	10	PWR	GND
11	PWR	1.8V	12	PWR	1.8V
13	SE Input	FPGA_PROG	14	SE Output	FPGA_LED0
15	SE Input	FPGA_INT	16	SE Output	FPGA_LED1
17	SE Input	FPGA_DONE	18	NC	NC
19	PWR	GND	20	PWR	GND

Backplane Slot Profile and Connection Tables

The SBC2A72-SVPX is a 3U VPX card that measures 100 mm x 160mm and is based off the VITA 78.0 standard. The backplane interface is based on the VITA 78.0 Payload Slot Profile: SLT3-PAY-2F2T1Q-14.2.1.

For reference, the slot profile for VITA 78.0 is shown below.

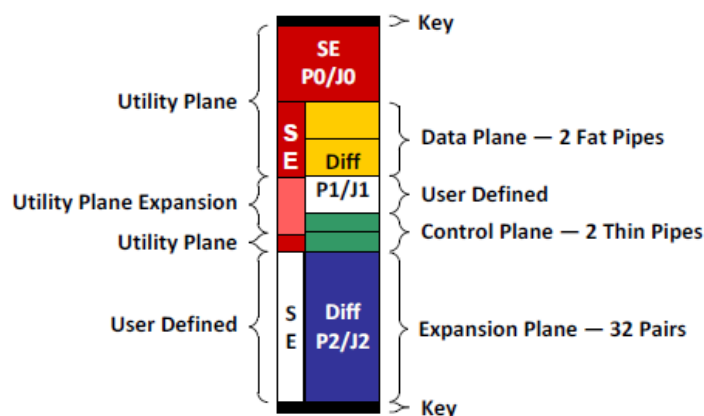


Figure 4. Backplane Slot Profile, SLT3-PAY-2F2T1Q-14.2.1

The table below provides a brief description of each one of the different plans defined in the SLT3-PAY-2F2T1Q-14.2.1 payload slot profile.

Table 4. VITA 78.0 Plane Definitions

Plane	Description
Data Plane	High-speed payload and mission data transfer between processing modules.
Control Plane	Command, control, and health/status communications.
Utility Plane	Power distribution, timing, clocks, reset, discretes, housekeeping.
Expansion Plane	Local or optional I/O expansion between modules (e.g., co-processors or sensors).

Table 5. P0, P1, and P2 Connector Part Number and Manufacturer (Module)

Connector	Position	Part Number	Vendor
Backplane P0 (Module)	P0	KX1HCP02C1TBH	Smiths Connector
Backplane P1 (Module)	P1	KX1FCD02C1TBH	Smiths Connector
Backplane P2 (Module)	P2	KX1FED02C1TBH	Smiths Connector

Table 6. J0, J1, and J2 Connector Part Number and Manufacturer (Backplane)

Connector	Position	Part Number	Vendor
Backplane P0 (Backplane)	J0	KX2HCU01C1TAH	Smiths Connector
Backplane P1 (Backplane)	J1	KX2FCU01C1TAH	Smiths Connector
Backplane P2 (Backplane)	J2	KX2FEU01C1TAH	Smiths Connector

Backplane Slot Profile and Connection Tables

The SBC2A72-SVPX Single Board Computer is in a 3U, 160mm, SpaceVPX form factor with VITA 78.0 based backplane profile SLT3-PAY-2F2T1Q-14.2.1. The P0, P1, and P2 Connector Pinouts are depicted below.

P0 Backplane Connector Signal/Pin Mapping

Table 7. SBC2A72-SBC Utility Plane Signal on P0

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Table 8. SBC2A72-SVPX Utility Plane Signal on P0 and SBC2A72-SVPX Signal Name

P0 Connector Pin Location	P0 Connector Name	SBC2A72 Name	Signal Type
RowG1	Vs1	12V VS1	
RowG2	Vs1	12V VS1	
RowG3	Vs3	N/C	
RowG4	SM2	MCU (SM_RESET)	
RowG5	GAP*	MCU (GAP)	
RowG6	GA3*	MCU (GA3)	
RowG7	TCK		
RowG8	GND	Ground	
RowF1	Vs1	12V VS1	
RowF2	Vs1	12V VS1	
RowF3	Vs3	N/C	
RowF4	SM3	MCU (SM_STAT)	
RowF5	GA4*	MCU (GA4)	
RowF6	GA2*	MCU (GA2)	
RowF7	GND	Ground	
RowF8	REF_CLK-	Clock Subsystem	

P0 Connector Pin Location	P0 Connector Name	SBC2A72 Name	Signal Type
RowE1	Vs1	12V VS1	
RowE2	Vs1	12V VS1	
RowE3	Vs3	N/C	
RowE4	GND	Ground	
RowE5	GND	Ground	
RowE6	GND	Ground	
RowE7	TDO		
RowE8	REF_CLK+	Clock Subsystem	
RowD1	No Pad*		
RowD2	No Pad*		
RowD3	No Pad*		
RowD4	-12V_Aux		
RowD5	3.3V_Aux	3.3V Aux (Build Option)	
RowD6	+12V_Aux		
RowD7	TDI		
RowD8	GND	Ground	
RowC1	Vs2	N/C	
RowC2	Vs2	N/C	
RowC3	Vs3	N/C	
RowC4	GND	Ground	
RowC5	GND	Ground	
RowC6	GND	Ground	
RowC7	GND	Ground	
RowC8	AUX_CLK-	LVDS to SE (PPS)	
RowB1	Vs2	N/C	
RowB2	Vs2	N/C	
RowB3	Vs3	N/C	
RowB4	SYSRESET*	MCU (RSTn)	
RowB5	SM0	MCU (I2C)	
RowB6	GA1*	MCU (GA1)	
RowB7	TMS		
RowB8	AUX_CLK+	LVDS to SE (PPS)	
RowA1	Vs2	N/C	
RowA2	Vs2	N/C	
RowA3	Vs3	N/C	
RowA4	NVMRO		
RowA5	SM1	MCU (I2C)	

P0 Connector Pin Location	P0 Connector Name	SBC2A72 Name	Signal Type
RowA6	GA0*	MCU (GA0)	
RowA7	TRST*		
RowA8	GND	Ground	

P1 Backplane Connector Signal/Pin Mapping

Table 9. SBC2A72-SVPX Module P1 Connector Pinout

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	SYS_CONP*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		REF_CLK1-	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	REF_CLK1+	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		REF_CLK2-	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane	REF_CLK2+	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

The SpaceVPX Control Plane is implemented with a SpaceWire (SpW) and UART interface which is connected to the VA41630 Processor.

The Data Plane is implemented with 4 Gigabit Ethernet Ports which include 2x TSN 1GbE and 2x 1000Base-X interfaces.

Table 10. SBC2A72-SVPX Module P1 Connector Pinout and SBC2A72-SVPX Signal Name

P1 Connector Pin Location	P1 Connector Name	SBC2A72-SVPX Name	Signal Type
RowG1	SYS_CONP*	MCU (SYS_CONP)	
RowG2	GND	Ground	
RowG3	VBAT	N/C	
RowG4	GND	Ground	
RowG5	SYS_CON*	MCU (SYS_CON)	
RowG6	GND	Ground	
RowG7	REF_CLK1-	Clock Subsystem	
RowG8	GND	Ground	
RowG9	REF_CLK1+	Clock Subsystem	
RowG10	GND	Ground	

P1 Connector Pin Location	P1 Connector Name	SBC2A72-SVPX Name	Signal Type
RowG11	REF_CLK2-	N/C	
RowG12	GND	Ground	
RowG13	REF_CLK2+	N/C	
RowG14	GND	Ground	
RowG15	Maskable Reset*	MCU (MaskableReset)	
RowG16	GND	Ground	
RowF1	GND	Ground	
RowF2	DP01-TD1-	Quad 1GbE PHY	
RowF3	GND	Ground	
RowF4	DP01-TD3-	Quad 1GbE PHY	
RowF5	GND	Ground	
RowF6	DP02-TD1-	Quad 1GbE PHY	
RowF7	GND	Ground	
RowF8	DP02-TD3-	Quad 1GbE PHY	
RowF9	GND	Ground	
RowF10	UD	VA7230 (USB1)	
RowF11	GND	Ground	
RowF12	UD	VA7230 (USB1)	
RowF13	GND	Ground	
RowF14	CPtp02-DD-	Quad 1GbE PHY	
RowF15	GND	Ground	
RowF16	CPtp01-DD-	Quad 1GbE PHY	
RowE1_Even	GND-J1	Ground	
RowE2_Even	DP01-TD1+	Quad 1GbE PHY	
RowE3_Even	GND-J1	Ground	
RowE4_Even	DP01-TD3+	Quad 1GbE PHY	
RowE5_Even	GND-J1	Ground	
RowE6_Even	DP02-TD1+	Quad 1GbE PHY	
RowE7_Even	GND-J1	Ground	
RowE8_Even	DP02-TD3+	Quad 1GbE PHY	
RowE9_Even	GND-J1	Ground	
RowE10_Even	UD	VA7230 (USB1)	
RowE11_Even	GND-J1	Ground	
RowE12_Even	UD	VA7230 (USB1)	
RowE13_Even	GND-J4	Ground	
RowE14_Even	CPtp02-DD+	Quad 1GbE PHY	
RowE15_Even	GND-J4	Ground	
RowE16_Even	CPtp01-DD+	Quad 1GbE PHY	
RowE1_Odd	DP01-TD0-		
RowE2_Odd	GND-J1	Ground	
RowE3_Odd	DP01-TD2-		
RowE4_Odd	GND-J1	Ground	
RowE5_Odd	DP02-TD0-		
RowE6_Odd	GND-J1	Ground	
RowE7_Odd	DP02-TD2-		
RowE8_Odd	GND-J1	Ground	

P1 Connector Pin Location	P1 Connector Name	SBC2A72-SVPX Name	Signal Type
RowE9_Odd	UD	MCU (UART)	
RowE10_Odd	GND-J1	Ground	
RowE11_Odd	UD	VA7230 (USB1)	
RowE12_Odd	GND-J1	Ground	
RowE13_Odd	CPTp02-DB-	Quad 1GbE PHY	
RowE14_Odd	GND-J4	Ground	
RowE15_Odd	CPTp01-DB-	Quad 1GbE PHY	
RowE16_Odd	GND-J4	Ground	
RowD1	DP01-TD0+		
RowD2	GND	Ground	
RowD3	DP01-TD2+		
RowD4	GND	Ground	
RowD5	DP02-TD0+		
RowD6	GND	Ground	
RowD7	DP02-TD2+		
RowD8	GND	Ground	
RowD9	UD	MCU (UART)	
RowD10	GND	Ground	
RowD11	UD	VA7230 (USB1)	
RowD12	GND	Ground	
RowD13	CPTp02-DB+	Quad 1GbE PHY	
RowD14	GND	Ground	
RowD15	CPTp01-DB+	Quad 1GbE PHY	
RowD16	GND	Ground	
RowC1	GND	Ground	
RowC2	DP01-RD1-	Quad 1GbE PHY	
RowC3	GND	Ground	
RowC4	DP01-RD3-	Quad 1GbE PHY	
RowC5	GND	Ground	
RowC6	DP02-RD1-	Quad 1GbE PHY	
RowC7	GND	Ground	
RowC8	DP02-RD3-	Quad 1GbE PHY	
RowC9	GND	Ground	
RowC10	UD	MCU (SpW)	
RowC11	GND	Ground	
RowC12	UD	MCU (SpW)	
RowC13	GND	Ground	
RowC14	CPTp02-DC-	Quad 1GbE PHY	
RowC15	GND	Ground	
RowC16	CPTp01-DC-	Quad 1GbE PHY	
RowB1_Even	GND-J1	Ground	
RowB2_Even	DP01-RD1+	Quad 1GbE PHY	
RowB3_Even	GND-J1	Ground	
RowB4_Even	DP01-RD3+	Quad 1GbE PHY	
RowB5_Even	GND-J1	Ground	
RowB6_Even	DP02-RD1+	Quad 1GbE PHY	
RowB7_Even	GND-J1	Ground	

P1 Connector Pin Location	P1 Connector Name	SBC2A72-SVPX Name	Signal Type
RowB8_Even	DP02-RD3+	Quad 1GbE PHY	
RowB9_Even	GND-J1	Ground	
RowB10_Even	UD	MCU (SpW)	
RowB11_Even	GND-J1	Ground	
RowB12_Even	UD	MCU (SpW)	
RowB13_Even	GND-J4	Ground	
RowB14_Even	CPTp02-DC+	Quad 1GbE PHY	
RowB15_Even	GND-J4	Ground	
RowB16_Even	CPTp01-DC+	Quad 1GbE PHY	
RowB1_Odd	DP01-RD0-	Quad 1GbE PHY	
RowB2_Odd	GND-J1	Ground	
RowB3_Odd	DP01-RD2-	Quad 1GbE PHY	
RowB4_Odd	GND-J1	Ground	
RowB5_Odd	DP02-RD0-	Quad 1GbE PHY	
RowB6_Odd	GND-J1	Ground	
RowB7_Odd	DP02-RD2-	Quad 1GbE PHY	
RowB8_Odd	GND-J1	Ground	
RowB9_Odd	UD	MCU (SpW)	
RowB10_Odd	GND-J1	Ground	
RowB11_Odd	UD	MCU (SpW)	
RowB12_Odd	GND-J1	Ground	
RowB13_Odd	CPTp02-DA-	Quad 1GbE PHY	
RowB14_Odd	GND-J4	Ground	
RowB15_Odd	CPTp01-DA-	Quad 1GbE PHY	
RowB16_Odd	GND-J4	Ground	
RowA1	DP01-RD0+	Quad 1GbE PHY	
RowA2	GND	Ground	
RowA3	DP01-RD2+	Quad 1GbE PHY	
RowA4	GND	Ground	
RowA5	DP02-RD0+	Quad 1GbE PHY	
RowA6	GND	Ground	
RowA7	DP02-RD2+	Quad 1GbE PHY	
RowA8	GND	Ground	
RowA9	UD	MCU (SpW)	
RowA10	GND	Ground	
RowA11	UD	MCU (SpW)	
RowA12	GND	Ground	
RowA13	CPTp02-DA+	Quad 1GbE PHY	
RowA14	GND	Ground	
RowA15	CPTp01-DA+	Quad 1GbE PHY	
RowA16	GND	Ground	

P2 Backplane Connector Signal/Pin Mapping

Table 11. SBC2A72-SVPX Module P2 Connector Pinout

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Backplane J2		Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	Expansion Plane X16 using [15:0]	UD	GND	GND-J2	EP00-TD-	EP00-TD+	GND	GND-J2	EP00-RD-	EP00-RD+
2		GND	EP01-TD-	EP01-TD+	GND-J2	GND	EP01-RD-	EP01-RD+	GND-J2	GND
3		UD	GND	GND-J2	EP02-TD-	EP02-TD+	GND	GND-J2	EP02-RD-	EP02-RD+
4		GND	EP03-TD-	EP03-TD+	GND-J2	GND	EP03-RD-	EP03-RD+	GND-J2	GND
5		UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6		GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7		UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8		GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10		GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11		UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12		GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13		UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14		GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15		UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16		GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

The Expansion Plane contains the following I/O:

- VA7230 CPU
 - o PCIe Gen 3.0 x 1
 - o DisplayPort 1.3 and eDP 1.4
 - o 8 SE GPIO
- CertusPro FGPA
 - o 6.25 SERDES x 4
 - o 6 LVDS GPIO pairs
 - o 4 SE GPIO

Table 12. SBC2A72-SVPX Module P2 Connector Pinout and SBC2A72-SVPX Signal Name

P2 Connector Pin Location	P2 Connector Name	SBC2A72-SVPX Name	Signal Type
RowG1	UD	VA7230 (GPIO)	
RowG2	GND	Ground	
RowG3	UD	VA7230 (GPIO)	
RowG4	GND	Ground	
RowG5	UD	VA7230 (GPIO)	
RowG6	GND	Ground	
RowG7	UD	VA7230 (GPIO)	

P2 Connector Pin Location	P2 Connector Name	SBC2A72-SVPX Name	Signal Type
RowG8	GND	Ground	
RowG9	UD	VA7230 (GPIO)	
RowG10	GND	Ground	
RowG11	UD	VA7230 (GPIO)	
RowG12	GND	Ground	
RowG13	UD	VA7230 (I2C/GPIO)	
RowG14	GND	Ground	
RowG15	UD	VA7230 (I2C/GPIO)	
RowG16	GND	Ground	
RowF1	GND	Ground	
RowF2	EP01-TD-	VA7230 (DP)	
RowF3	GND	Ground	
RowF4	EP03-TD-	VA7230 (DP)	
RowF5	GND	Ground	
RowF6	EP05-T-	VA7230 (DP)	
RowF7	GND	Ground	
RowF8	EP07-T-	CertusPro (GPIO)	
RowF9	GND	Ground	
RowF10	EP09-T-	CertusPro (SERDES)	
RowF11	GND	Ground	
RowF12	EP11-T-	CertusPro (SERDES)	
RowF13	GND	Ground	
RowF14	EP13-T-	Mezzanine (SERDES)	
RowF15	GND	Ground	
RowF16	EP15-T-	Mezzanine (SERDES)	
RowE1_Even	GND-J2	Ground	
RowE2_Even	EP01-TD+	VA7230 (DP)	
RowE3_Even	GND-J2	Ground	
RowE4_Even	EP03-TD+	VA7230 (DP)	
RowE5_Even	GND-J2	Ground	
RowE6_Even	EP05-T+	VA7230 (DP)	
RowE7_Even	GND-J2	Ground	
RowE8_Even	EP07-T+	CertusPro (GPIO)	
RowE9_Even	GND-J2	Ground	
RowE10_Even	EP09-T+	CertusPro (SERDES)	
RowE11_Even	GND-J2	Ground	
RowE12_Even	EP11-T+	CertusPro (SERDES)	
RowE13_Even	GND-J2	Ground	
RowE14_Even	EP13-T+	Mezzanine (SERDES)	
RowE15_Even	GND-J2	Ground	
RowE16_Even	EP15-T+	Mezzanine (SERDES)	
RowE1_Odd	EP00-TD-	VA7230 (PCIe)	
RowE2_Odd	GND-J2	Ground	
RowE3_Odd	EP02-TD-	VA7230 (DP)	
RowE4_Odd	GND-J2	Ground	
RowE5_Odd	EP04-T-	VA7230 (DP)	

P2 Connector Pin Location	P2 Connector Name	SBC2A72-SVPX Name	Signal Type
RowE6_Odd	GND-J2	Ground	
RowE7_Odd	EP06-T-	Power Subsystem (DP 3.3V)	
RowE8_Odd	GND-J2	Ground	
RowE9_Odd	EP08-T-	CertusPro (SERDES)	
RowE10_Odd	GND-J2	Ground	
RowE11_Odd	EP10-T-	CertusPro (SERDES)	
RowE12_Odd	GND-J2	Ground	
RowE13_Odd	EP12-T-	Mezzanine (SERDES)	
RowE14_Odd	GND-J2	Ground	
RowE15_Odd	EP14-T-	Mezzanine (SERDES)	
RowE16_Odd	GND-J2	Ground	
RowD1	EP00-TD+	VA7230 (PCIe)	
RowD2	GND	Ground	
RowD3	EP02-TD+	VA7230 (DP)	
RowD4	GND	Ground	
RowD5	EP04-T+	VA7230 (DP)	
RowD6	GND	Ground	
RowD7	EP06-T+	VA7230 (DP)	
RowD8	GND	Ground	
RowD9	EP08-T+	CertusPro (SERDES)	
RowD10	GND	Ground	
RowD11	EP10-T+	CertusPro (SERDES)	
RowD12	GND	Ground	
RowD13	EP12-T+	Mezzanine (SERDES)	
RowD14	GND	Ground	
RowD15	EP14-T+	Mezzanine (SERDES)	
RowD16	GND	Ground	
RowC1	GND	Ground	
RowC2	EP01-RD-	CertusPro (LVDS GPIO)	
RowC3	GND	Ground	
RowC4	EP03-RD-	CertusPro (LVDS GPIO)	
RowC5	GND	Ground	
RowC6	EP05-R-	CertusPro (LVDS GPIO)	
RowC7	GND	Ground	
RowC8	EP07-R-	CertusPro (GPIO)	
RowC9	GND	Ground	
RowC10	EP09-R-	CertusPro (SERDES)	
RowC11	GND	Ground	
RowC12	EP11-R-	CertusPro (SERDES)	
RowC13	GND	Ground	
RowC14	EP13-R-	Mezzanine (SERDES)	
RowC15	GND	Ground	
RowC16	EP15-R-	Mezzanine (SERDES)	
RowB1_Even	GND-J2	Ground	
RowB2_Even	EP01-RD+	CertusPro (LVDS GPIO)	
RowB3_Even	GND-J2	Ground	
RowB4_Even	EP03-RD+	CertusPro (LVDS GPIO)	

P2 Connector Pin Location	P2 Connector Name	SBC2A72-SVPX Name	Signal Type
RowB5_Even	GND-J2	Ground	
RowB6_Even	EP05-R+	CertusPro (LVDS GPIO)	
RowB7_Even	GND-J2	Ground	
RowB8_Even	EP07-RD+	CertusPro (GPIO)	
RowB9_Even	GND-J2	Ground	
RowB10_Even	EP09-R+	CertusPro (SERDES)	
RowB11_Even	GND-J2	Ground	
RowB12_Even	EP11-R+	CertusPro (SERDES)	
RowB13_Even	GND-J2	Ground	
RowB14_Even	EP13-R+	Mezzanine (SERDES)	
RowB15_Even	GND-J2	Ground	
RowB16_Even	EP15-R+	Mezzanine (SERDES)	
RowB1_Odd	EP00-RD-	VA7230 (PCIe)	
RowB2_Odd	GND-J2	Ground	
RowB3_Odd	EP02-RD-	CertusPro (LVDS GPIO)	
RowB4_Odd	GND-J2	Ground	
RowB5_Odd	EP04-R-	CertusPro (LVDS GPIO)	
RowB6_Odd	GND-J2	Ground	
RowB7_Odd	EP06-R-	CertusPro (LVDS GPIO)	
RowB8_Odd	GND-J2	Ground	
RowB9_Odd	EP08-R-	CertusPro (SERDES)	
RowB10_Odd	GND-J2	Ground	
RowB11_Odd	EP10-R-	CertusPro (SERDES)	
RowB12_Odd	GND-J2	Ground	
RowB13_Odd	EP12-R-	Mezzanine (SERDES)	
RowB14_Odd	GND-J2	Ground	
RowB15_Odd	EP14-R-	Mezzanine (SERDES)	
RowB16_Odd	GND-J2	Ground	
RowA1	EP00-RD+	VA7230 (PCIe)	
RowA2	GND	Ground	
RowA3	EP02-RD+	CertusPro (LVDS GPIO)	
RowA4	GND	Ground	
RowA5	EP04-R+	CertusPro (LVDS GPIO)	
RowA6	GND	Ground	
RowA7	EP06-R+	CertusPro (LVDS GPIO)	
RowA8	GND	Ground	
RowA9	EP08-R+	CertusPro (SERDES)	
RowA10	GND	Ground	
RowA11	EP10-R+	CertusPro (SERDES)	
RowA12	GND	Ground	
RowA13	EP12-R+	Mezzanine (SERDES)	
RowA14	GND	Ground	
RowA15	EP14-R+	Mezzanine (SERDES)	
RowA16	GND	Ground	

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX	3.3V Auxiliary Input	3	3.6	Vdc
Pd	Max. Power Dissipation		30	W
Storage Temp		-40	+105C	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Mass			0.65 (TBC)	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID		30K	rad (Si)
nd-SEL Immunity		37	MeV-cm ² /mg
Total Single Event Rate Requiring External or Ground Intervention	LEO ISS @ 500km / 51° Inclination	6.17E-04	Event per year

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@ 70 °C	318,894	hours
Reliability (R)	3 years @ 70°C @ 100 Duty Cycle 5 years @ 70°C @ 100 Duty Cycle 7 years @ 70°C @ 100 Duty Cycle	0.872 0.825 0.719	

Acceptance Testing (FM3 Class C and FM4 Class D)

Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	

Qualification Testing

Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles
Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Functional Description

The Frontgrade™ SBC2A72-SVPX is a high-performance, low-power Single Board Computer (SBC) designed for harsh-environment applications requiring advanced processing, graphics acceleration, and flexible interface capability within a compact 3U-160mm SpaceVPX form factor. The board is optimized for Size, Weight, and Power (SWaP) constrained missions including onboard computing, payload processing, graphics-intensive applications, command and control, and high-throughput data handling.

At the core of the SBC is the radiation tolerant Vorago VA7230 processor, featuring dual ARM® Cortex®-A72 CPU cores and an integrated Graphics Processing Unit (GPU). This architecture provides efficient general-purpose computing alongside graphics and image-processing acceleration, delivering up to 10.4 GFLOPs of processing capability suitable for AI inference, sensor processing, and visualization workloads. The processor subsystem is complemented by extensive onboard memory resources and a broad set of high-speed communication interfaces supporting networking, telemetry, graphics, and mission data transport functions.

To provide application flexibility and interface scalability, the SBC2A72-SVPX integrates a CertusPro-NX-RT FPGA and an XMC+ mezzanine expansion interface. This architecture enables users to implement custom or mission specific I/O functions without modifying the base SBC hardware. The onboard FPGA currently provides PCIe-to-SpaceFibre functionality and can be adapted to support additional protocols and interface requirements for evolving payload and system architectures.

The board also incorporates a radiation hardened VA41630 ARM Cortex®-M4 microcontroller that performs system management and housekeeping functions. The MCU manages local monitoring and power control while supporting coordination and communication between plug-in modules within a larger SpaceVPX system. Additional system interfaces provided through the MCU include UART, SpaceWire, and GPIO connectivity to the system backplane.

Overall, SBC2A72-SVPX combines radiation tolerant processing, graphics acceleration, configurable FPGA resources, and extensive interface support in a compact and power-efficient platform intended for demanding computing applications.

Software Ecosystem

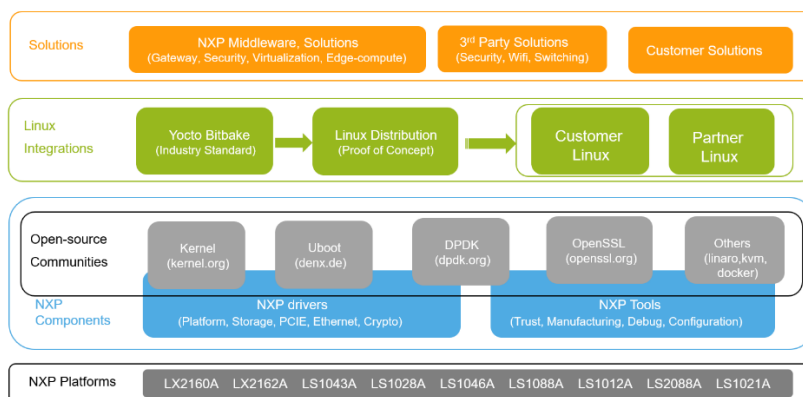


Figure 5. NXP Layerscape Software

Features

Layerscape LDP Components

- Freely available
 - Download from public repositories (e.g. github.com)
 - No need to download a large ISO and extract
- Modularized
 - Boot-loaders, Kernels, User-space libraries, Tools, Configuration
 - Pick and choose ones you need
- Clean layering, separation
 - Separate patches on top of open source
 - Patches identified by platform/IP
- Easy updates via Git
 - Periodic releases and interim updates
 - Support for two recent LTS kernels

Layerscape LDP

- Easy boot mechanisms
 - Boot from multiple sources
 - Simple, quick updates from any mass-storage
 - Brick-proof mechanism* - easy recovery via SD
- Easy runtime upgrades
 - Rich LDP user-land and repositories
 - On-the-fly install with apt-get
 - Build/install from source on target
- Latest and greatest
 - Latest Layerscape platforms
 - Latest drivers and features
 - Layerscape specific tools, drivers

What's New In L6.1.1-1.0.0-LLDP

- NXP Layerscape LDP userland:
 - NXP Layerscape LDP, including Linux distro main packages and NXP packages
- Toolchain: gcc-11.2, glibc-2.36, binutils-2.38, gdb-12.1
- Linux kernel core and virtualization:
 - LTS kernel 6.1.1 update
- Linux kernel drivers:
 - Data Plane Development Kit (DPDK):
 - Virtualization - OVS-DPDK
- U-Boot bootloader:
 - U-Boot v2022.04 update
 - AQR113C on TWR-LS1021A, LS1088ARDB, and LX2162AQDS
- Other tools and utilities:
 - AQR113C firmware
 - Yocto bitbake

Mechanical Drawing

Placeholder (needs updated with latest information)

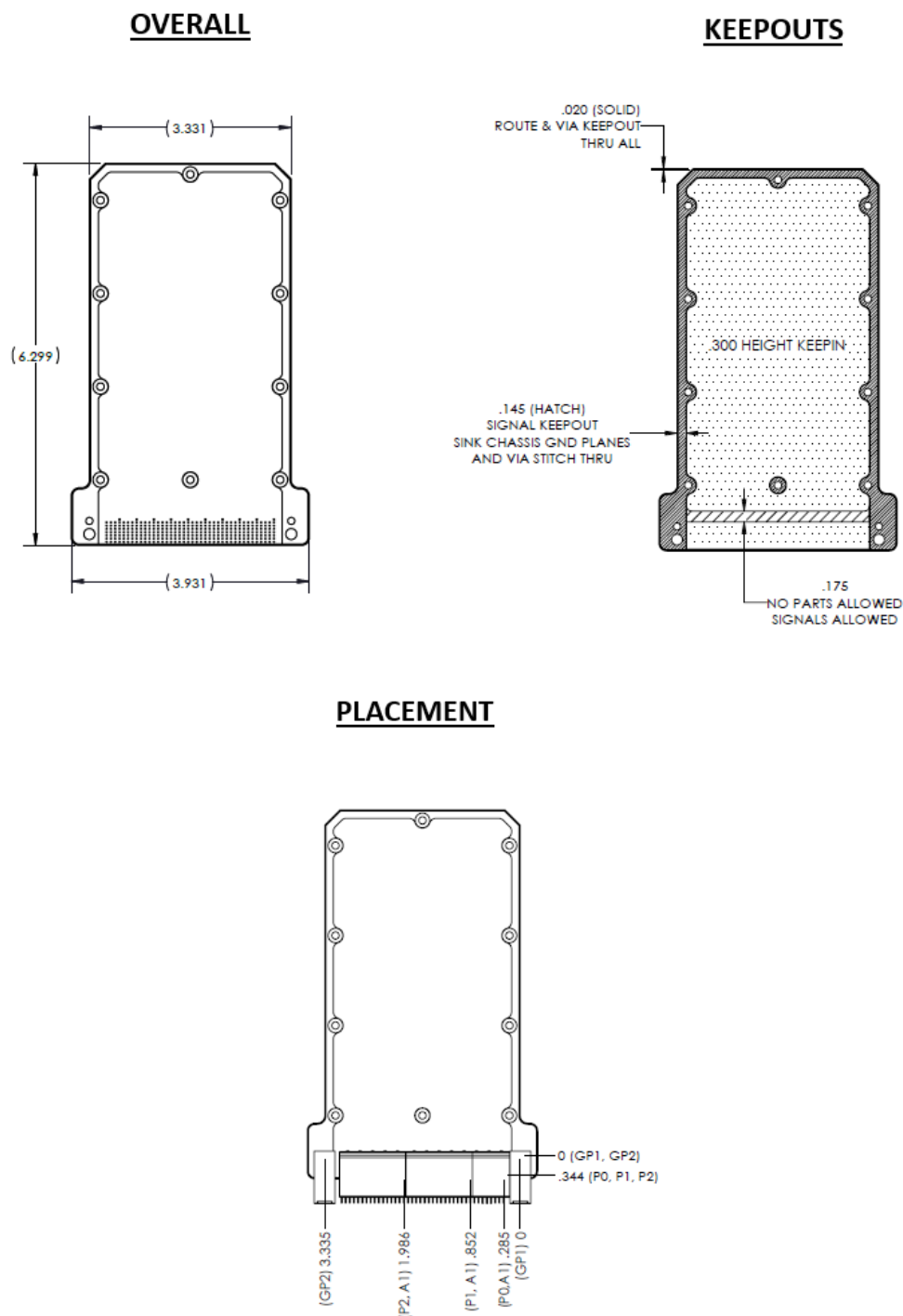


Figure 6. SBC2A72-SVPX Mechanical Information

Revision History

Date	Rev	Author	Change Description	Page #
5/27/2026	1.0	DPA	Initial Release of Preliminary Datasheet	All

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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