FRONTGRADE

PRELIMINARY DATASHEET

3U SpaceVPX Versal VC1902 Reconfigurable Processing Module

RPMG1-SVPX

4/28/2026 | Version #1.0



Introduction

RPMG1-SVPX Reconfigurable Processing Module
High-Performance Adaptive Computing for SpaceVPX™ Architectures

The **Frontgrade RPMG1-SVPX** is a high-performance **Reconfigurable Processing Module (RPM)** designed to deliver adaptive compute, deterministic control, and high-bandwidth data movement for advanced space and defense missions. Based on the **AMD Versal® VC1902 System-on-Chip**, the RPMG1-SVPX combines multicore processing, programmable logic, and high-speed I/O in a compact **3U SpaceVPX™ form factor**, enabling next-generation onboard autonomy, sensor processing, and real-time mission computing.

The Frontgrade RPMG1-SVPX is an ideal processing backbone for advanced sensor payloads including **EO/IR, SAR, EW, SIGINT, and focal plane array** systems. Its heterogeneous Versal architecture enables deterministic front-end processing, hardware-accelerated signal conditioning, and software-defined mission control within a single, space-qualified SpaceVPX module.

At the core of the RPMG1-SVPX is the **Versal VC1902 SoC**, integrating **dual Arm® Cortex-A72 application processors (up to 1.7 GHz)** and **dual Cortex-R5 real-time processors (up to 750 MHz)** alongside a large programmable logic fabric and hardened AI/ML plus DSP resources. This heterogeneous architecture allows software-defined control, real-time deterministic processing, and hardware-accelerated data paths to coexist on a single module—supporting complex workloads that blend signal processing, AI/ML inference, protocol handling, and mission management.

The module includes **16 GB of DDR4 volatile memory**, **8 Gbits of QSPI boot memory**, and up to **1 Tb of raw non-volatile data storage configured in SLC mode**, providing robust memory resources for mission software, intermediate data buffering, and payload processing. When configured with the **Fibre Optic as an example, the board can interface with a mezzanine Card (FIOM-RPMG1)** and the RPMG1-SVPX expands its connectivity to support **four 10Gbase-SR Fiber Optic Ethernet port, six 1000Base-T Ethernet ports**, **eight RS-422 GPIO and a 1PPS LVDS input**, an **RS-422 UART**. This flexibility enables seamless integration with sensors, payloads, timing sources, and spacecraft avionics.

Optimized for deployment in SWaP-constrained environments, the RPMG1-SVPX is housed in a **standard 3U 160 mm SpaceVPX form factor** with an estimated **mass under 650 grams**. The module supports operation up to **51 °C when mounted to a regulated thermal interface** and has a **maximum power consumption of 125 W**, with up to **80 W allocated to the Versal SoC core**. Radiation performance supports >**30 krads (Si) TID**

Target Applications

- Onboard payload and sensor data processing
  - EO/IR payload processing
  - Synthetic Aperture Radar (SAR) processing
  - Focal Plane Array (FPA) control and readout
  - EW / SIGINT / ELINT processing
- Real-time signal processing and software-defined radios
- AI/ML inference and autonomous decision-making
- Ethernet gateway routing and protocol processing
- Distributed SpaceVPX compute architectures

Why It Matters

The **RPMG1-SVPX** delivers **adaptive, high-performance computing** where it matters most—**onboard the platform**. By combining general-purpose processing, real-time control, and reconfigurable acceleration in a single SpaceVPX module, it allows system architects to consolidate functions, reduce latency, and increase mission autonomy. Its flexibility, performance, and radiation-aware design make it an ideal foundation for next-generation spacecraft, airborne ISR platforms, and systems that demand deterministic behavior, high data throughput, and long-term reliability in harsh environments.

Ordering Information

Ordering PN	Product Grade	Mission Class / Environment
RPMG1-SVPX-OP-EDU	EDU = EM (Room Temp only)	Lab / Development Use Cases
RPMG1-SVPX-OP-FM4	COTS Parts with FM3 AI&T	Target Mission Class D
RPMG1-SVPX-OP-FM3	Level 3 Parts Grade	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds. If Frontgrade selected parts are not suitable for the application, NRE to select and upscreen alternate parts may be quoted separately.

FEATURES

Versal VC1902 Processing Capabilities

Processing System (PS)

- Application Processing
  - — CPU: 2× Arm® Cortex-A72
  - — Max Frequency: up to 1.7 GHz
  - — Performance (est.)
    - ~3.5 DMIPS/MHz/core
    - ~6,000 DMIPS per core @ 1.7 GHz
    - ~12,000 DMIPS total (dual-core)
- Real-Time Processing
  - — CPU: 2× Arm® Cortex-R5F
  - — Max Frequency: up to 750 MHz
  - — Modes: Lockstep or split
  - — Performance (est.)
    - ~1.6–2.0 DMIPS/MHz/core
    - ~1,200–1,500 DMIPS per core
- Platform Management
  - — PMC (Platform Management Controller): Dedicated secure processor
  - — Functions: Secure boot, configuration, clocking, power, device management

Programmable Logic (PL) & Acceleration

- FPGA Fabric
  - — Logic Resources: ~900k system logic
  - — On-Chip Memory:
    - BRAM + UltraRAM (URAM) for low-latency buffering
  - — Partial Reconfiguration: Supported
- DSP Resources
  - — DSP48E2 Slices: ~1,968
  - — Peak Arithmetic Throughput:
    - ~1TMAC FP32 performance @ 600MHz
- AIE Resources
  - — 400 AIE Tiles
    - ~130 TOPS INT8 performance 1GHz

User Memory

- 2x 8GByte + ECC DDR4 (x72 bus width) 2400MT/s
- 1GByte MRAM NV Configuration Storage
- 128 GByte (pSLC) raw NAND Flash

Application Backplane Interfaces (VITA 78.0 Profile: SLT3-PAY-2F2T1Q-14.2.1)

- (P1 DP01) VC1902 GTY Bank
- (P1 DP02) VC1902 GTY Bank
- (P1 CPtp01-02) VC1902 GTY Bank
- (P1 UD0:6) VC1902 XPIO Bank
- (P1 UD7:8) 700MHz CLK VC1902 GTY Bank
- (P1 REF_CLK2:1) Custom Pulse VC1902 GTY XPIO Bank
- (P2 EP00-03) VC1902 GTY Bank
- (P2 EP04-07) VC1902 GTY Bank
- (P2 EP08-011) VC1902 GTY Bank
- (P2 EP12-15) VC1902 GTY Bank
- (P2 UD) VC1902 UART. CONFIG & RST LP_MIO Bank
- (P2 UD) Microcontroller UART, CONFIG & RST

Backplane Utility Segment

- 5x GA + 1x GA Parity
- (IPMI SM0:3) SDA, SCL, SM_STAT# & SM_RESET#
- SYSRESET#
- 1x LVDS REFCLK VC1902 HDIO Bank
- 1x LVDS AUXCLK (1PPS) VC1902 HDIO Bank
- 12V VS1
- 3.3V_AUX (Optional)

Mezzanine Interfaces

- (P15) F/O SERDES VC1902 GTY Bank
- (P15) RGMII Port 6 VC1902 XPIO Bank
- (P16) RGMII Port 4&5 VC1902 XPIO Bank
- (P16) RGMII Port 1-3 VC1902 XPIO Bank
- 8x RS-422 GPIO
- 1x LVDS PPS Input

Mass & Thermal

- Mass: <0.65 kg
- 3U Form Factor: 160mm x 100mm / 1.2” Pitch
- -25°C to +51°C operational temp ref to
- Power consumption: <15W Typical / 30W Max
- TID: Up to 30 krads (Si)
- SEL Immune < 37MeV

Block Diagram

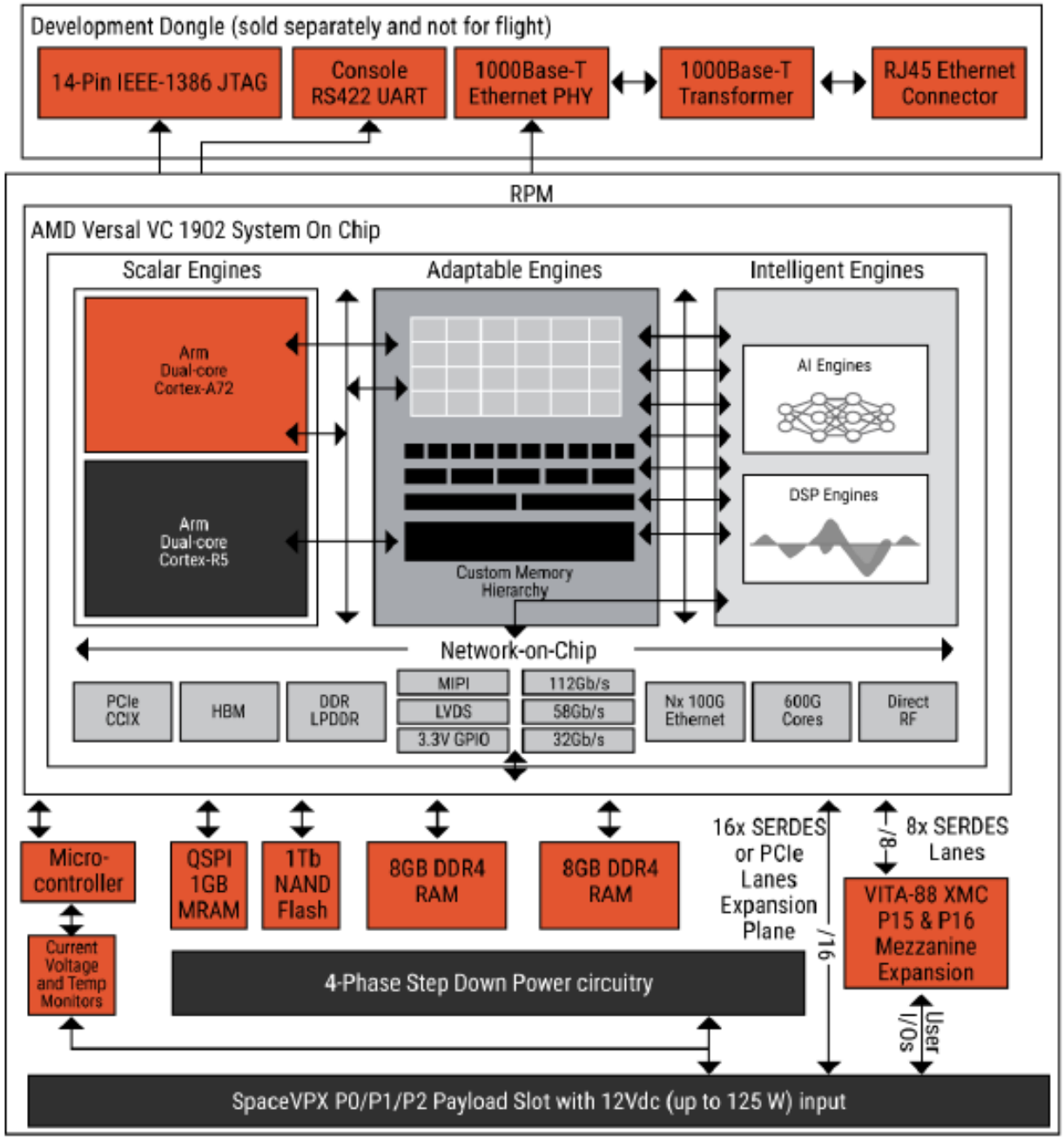


Figure 1. RPMG1-SVPX High Level Block Diagram

XMC Connector Interface

The RPMG1-SVPX provides a two Mezzanine connector Interfaces to the front side of the plug-in module.

Note: In the example above, the board interfacing with a XMC Mezzanine card and is connected via the P15 & P16 pinouts. The actual usage gets defined based on the choice of the mezzanine card that the board interfaces with. Our current offering for the Mezzanine card is the FIOM-RPMG1.

The interface is provided via Ports P15 & P16.

P15: Primary XMC Connector Pin Definition

Table 1. P15 XMC Connector Pin list

	A	B	C	D	E	F
01	DP00+	DP00-	3.3V	DP01+	DP01-	VPWR
02	GND	GND	TRST#	GND	GND	MRSTI#
03	DP02+	DP02-	3.3V	DP03+	DP03-	VPWR
04	GND	GND	TCK	GND	GND	MRSTO#
05	DP04+	DP04-	3.3V	DP05+	DP05-	VPWR
06	GND	GND	TMS	GND	GND	+12V
07	DP06+	DP06-	3.3V	DP07+	DP07-	VPWR
08	GND	GND	TDI	GND	GND	-12V
09	DP08+	DP08-	RPS	DP09+	DP09-	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	DP10+	DP10-	MBIST#	DP11+	DP11-	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	DP12+	DP12-	3.3V AUX	DP13+	DP13-	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	DP14+	DP14-	RPS	DP15+	DP15-	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	DP16+	DP16-	RFU	DP17+	DP17-	RFU
18	GND	GND	RPS	GND	GND	RPS
19	DP18+	DP18-	RPS	DP19+	DP19-	RPS

Table 2. P15 XMC Connector Pin list and Mezzanine Signal Name

P15 Connector Pin Location	P15 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
A01	DP00+	TD_IN_1_FIBER_P	
A02	GND	GND	
A03	DP02+	TD_IN_2_FIBER_P	
A04	GND	GND	
A05	DP04+	TD_IN_3_FIBER_P	
A06	GND	GND	
A07	DP06+	TD_IN_4_FIBER_P	
A08	GND	GND	
A09	DP08+	MEZ_SERDES_0_CLK_P	
A10	GND	GND	
A11	DP10+	LVDS-IN0 LV (1PPS)	
A12	GND	GND	
A13	DP12+	NC	

P15 Connector Pin Location	P15 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
A14	GND	GND	
A15	DP14+	QSGMII_0_TX_P	
A16	GND	GND	
A17	DP16+	QSGMII_1_TX_P	
A18	GND	GND	
A19	DP18+	125MhHz QSGMII_CLKI_P	
B01	DP00-	TD_IN_1_FIBER_N	
B02	GND	GND	
B03	DP02-	TD_IN_2_FIBER_N	
B04	GND	GND	
B05	DP04-	TD_IN_3_FIBER_N	
B06	GND	GND	
B07	DP06-	TD_IN_4_FIBER_N	
B08	GND	GND	
B09	DP08-	MEZ_SERDES_0_CLK_N	
B10	GND	GND	
B11	DP10-	NC	
B12	GND	GND	
B13	DP12-	NC	
B14	GND	GND	
B15	DP14-	QSGMII_0_TX_N	
B16	GND	GND	
B17	DP16-	QSGMII_1_TX_N	
B18	GND	GND	
B19	DP18-	125MhHz QSGMII_CLKI_N	
C01	3.3V	NC	
C02	TRST#	RSTN_IN_FIBER (3.3V)	
C03	3.3V	NC	
C04	TCK	QSGMII_MDC	
C05	3.3V	NC	
C06	TMS	QSGMII_MDIO	
C07	3.3V	NC	
C08	TDI	MODPRSN_FIBER (3.3V)	
C09	RPS	VBIT2_FIBER (3.3V)	
C10	TDO	VBIT1_FIBER (3.3V)	
C11	MBIST#	NC	
C12	GA1	NC	
C13	3.3V AUX	NC	
C14	GA2	NC	
C15	RPS	NC	
C16	MVMRO	NC	
C17	RFU	NC	
C18	RPS	422_TX_7 (3.3V)	
C19	RPS	422_TX_8 (3.3V)	
D01	DP01+	RD_OUT_1_FIBER_P	

P15 Connector Pin Location	P15 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
D02	GND	GND	
D03	DP03+	RD_OUT_2_FIBER_P	
D04	GND	GND	
D05	DP05+	RD_OUT_3_FIBER_P	
D06	GND	GND	
D07	DP07+	RD_OUT_4_FIBER_P	
D08	GND	GND	
D09	DP09+	NC	
D10	GND	GND	
D11	DP11+	NC	
D12	GND	GND	
D13	DP13+	NC	
D14	GND	GND	
D15	DP15+	QSGMII_0_RX_P	
D16	GND	GND	
D17	DP17+	QSGMII_1_RX_P	
D18	GND	GND	
D19	DP19+	NC	
E01	DP01-	RD_OUT_1_FIBER_N	
E02	GND	GND	
E03	DP03-	RD_OUT_2_FIBER_N	
E04	GND	GND	
E05	DP05-	RD_OUT_3_FIBER_N	
E06	GND	GND	
E07	DP07-	RD_OUT_4_FIBER_N	
E08	GND	GND	
E09	DP09-	NC	
E10	GND	GND	
E11	DP11-	NC	
E12	GND	GND	
E13	DP13-	NC	
E14	GND	GND	
E15	DP15-	QSGMII_0_RX_N	
E16	GND	GND	
E17	DP17-	QSGMII_1_RX_N	
E18	GND	GND	
E19	DP19-	NC	
F01	VPWR	+12V	
F02	MRSTI#	VERSAL_POR_B	
F03	VPWR	+12V	
F04	MRSTO#	NC	
F05	VPWR	+12V	
F06	+12V	+12V	
F07	VPWR	+12V	

P15 Connector Pin Location	P15 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
F08	-12V	NC	
F09	VPWR	+12V	
F10	GA0	NC	
F11	VPWR	+12V	
F12	MPRESENT#	Mezz_Present (Pulldown)	
F13	VPWR	+12V	
F14	MSDA	NC	
F15	VPWR	+12V	
F16	MSCL	NC	
F17	RFU	NC	
F18	RPS	422_TX_5 (3.3V)	
F19	RPS	422_TX_6 (3.3V)	

P16: Secondary XMC Connector Pin Definition

Table 3. P16 – Secondary XMC Connector Pin list

	A	B	C	D	E	F
01	DP00+	DP00-	UD	DP01+	DP01-	UD
02	GND	GND	UD	GND	GND	UD
03	DP02+	DP02-	UD	DP03+	DP03-	UD
04	GND	GND	UD	GND	GND	UD
05	DP04+	DP04-	UD	DP05+	DP05-	UD
06	GND	GND	UD	GND	GND	UD
07	DP06+	DP06-	UD	DP07+	DP07-	UD
08	GND	GND	UD	GND	GND	UD
09	DP08+	DP08-	UD	DP09+	DP09-	UD
10	GND	GND	UD	GND	GND	UD
11	DP10+	DP10-	UD	DP11+	DP11-	UD
12	GND	GND	UD	GND	GND	UD
13	DP12+	DP12-	UD	DP13+	DP13-	UD
14	GND	GND	UD	GND	GND	UD
15	DP14+	DP14-	UD	DP15+	DP15-	UD
16	GND	GND	UD	GND	GND	UD
17	DP16+	DP16-	UD	DP17+	DP17-	UD
18	GND	GND	UD	GND	GND	UD
19	DP18+	DP18-	UD	DP19+	DP19-	UD

Table 4. P16 – Secondary XMC Connector Pin list and Mezzanine Signal Name

P16 Connector Pin Location	P16 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
A01	DP00+	NC	
A02	GND	GND	
A03	DP02+	NC	
A04	GND	GND	
A05	DP04+	NC	
A06	GND	GND	
A07	DP06+	NC	
A08	GND	GND	
A09	DP08+	125MHz_QSGMII_CLK2_P	
A10	GND	GND	
A11	DP10+	NC	
A12	GND	GND	
A13	DP12+	MOSI_FIBER_LV	
A14	GND	GND	
A15	DP14+	422_RX_1 (3.3V)	
A16	GND	GND	
A17	DP16+	422_RX_2 (3.3V)	
A18	GND	GND	
A19	DP18+	R22_RX_3 (3.3V)	
B01	DP00-	NC	

P16 Connector Pin Location	P16 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
B02	GND	GND	
B03	DP02-	NC	
B04	GND	GND	
B05	DP04-	NC	
B06	GND	GND	
B07	DP06-	NC	
B08	GND	GND	
B09	DP08-	125MHz_QSGMII_CLK2_N	
B10	GND	GND	
B11	DP10-	SCK_FIBER_LV	
B12	GND	GND	
B13	DP12-	NC	
B14	GND	GND	
B15	DP14-	422_RX_4 (3.3V)	
B16	GND	GND	
B17	DP16-	422_RX_5 (3.3V)	
B18	GND	GND	
B19	DP18-	R22_RX_6 (3.3V)	
C01	UD	NC	
C02	UD	NC	
C03	UD	NC	
C04	UD	NC	
C05	UD	NC	
C06	UD	NC	
C07	UD	NC	
C08	UD	NC	
C09	UD	NC	
C10	UD	NC	
C11	UD	NC	
C12	UD	NC	
C13	UD	NC	
C14	UD	NC	
C15	UD	NC	
C16	UD	NC	
C17	UD	NC	
C18	UD	NC	
C19	UD	NC	
D01	DP01+	NC	
D02	GND	NC	
D03	DP03+	NC	
D04	GND	NC	
D05	DP05+	NC	
D06	GND	NC	
D07	DP07+	NC	

P16 Connector Pin Location	P16 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
D08	GND	NC	
D09	DP09+	NC	
D10	GND	NC	
D11	DP11+	NC	
D12	GND	NC	
D13	DP13+	NC	
D14	GND	NC	
D15	DP15+	NC	
D16	GND	NC	
D17	DP17+	NC	
D18	GND	NC	
D19	DP19+	NC	
E01	DP01-	NC	
E02	GND	GND	
E03	DP03-	NC	
E04	GND	GND	
E05	DP05-	NC	
E06	GND	GND	
E07	DP07-	SSN_FIBER_LV	
E08	GND	GND	
E09	DP09-	NC	
E10	GND	GND	
E11	DP11-	MISO_FIBER_LV	
E12	GND	GND	
E13	DP13-	NC	
E14	GND	GND	
E15	DP15-	422_TX_2 (3.3V)	
E16	GND	GND	
E17	DP17-	422_TX_3 (3.3V)	
E18	GND	GND	
E19	DP19-	R22_TX_4 (3.3V)	
F01	UD	NC	
F02	UD	NC	
F03	UD	NC	
F04	UD	NC	
F05	UD	NC	
F06	UD	NC	
F07	UD	NC	
F08	UD	NC	
F09	UD	NC	
F10	UD	NC	
F11	UD	NC	
F12	UD	NC	
F13	UD	NC	
F14	UD	NC	

P16 Connector Pin Location	P16 Connector Name	Mezz Name (FIOM-RPMG1)	Signal Type
F15	UD	NC	
F16	UD	NC	
F17	UD	NC	
F18	UD	NC	
F19	UD	NC	

Backplane Slot Profile and Connection Tables

The RPMG1-SVPX is a 3U VPX card that measures 100 mm x 160mm and is based off the VITA 78.0 standard. The backplane interface is based on the VITA 78.0 Payload Slot Profile: SLT3-PAY-2F2T1Q-14.2.1.

For reference, the slot profile for VITA 78.0 is shown below.

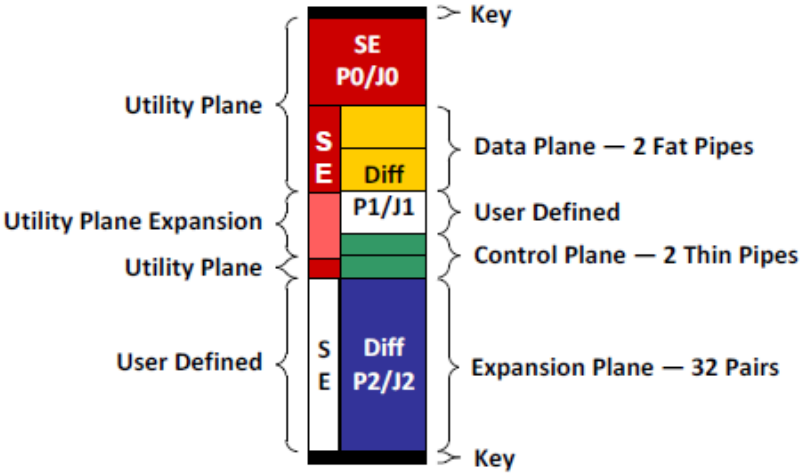


Figure 2. Backplane Slot Profile, SLT3-PAY-2F2T1Q-14.2.1

The table below provides a brief description of each one of the different plans defined in the SLT3-PAY-2F2T1Q-14.2.1 payload slot profile.

Table 5. VITA 78.0 Data, Control, Utility, and Expansion Plane Definitions

Plane	Description
Data Plane	High-speed payload and mission data transfer between processing modules.
Control Plane	Command, control, and health/status communications.
Utility Plane	Power distribution, timing, clocks, reset, discretes, housekeeping.
Expansion Plane	Local or optional I/O expansion between modules (e.g., co-processors or sensors).

Backplane Slot Profile and Connection Tables

The RPMG1-SVPX is a Reconfigurable Processor Module (AMD VC1902 Based) in a 3U, 160mm, SpaceVPX form factor with VITA 78.0 backplane profile SLT3-PAY-2F2T1Q-14.2.1. The P1 and P2 Connector Pinouts are depicted below.

PO Backplane Connector Signal/Pin Mapping

The utility backplane signals get connected to P0

Table 6. RPMG1-SVPX Utility Plane Signal on P0

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Table 7. RPMG1-SVPX Utility Plane Signal on P0 and RPMG1-SVPX Signal Name

P0 Connector Pin Location	P0 Connector Name	RPMG1-SVPX Name	Signal Type
RowG1	Vs1	+12V	
RowG2	Vs1	+12V	
RowG3	Vs3	N/C	
RowG4	SM2	SM2_RESET_IN	
RowG5	GAP*	GAP_VPX	
RowG6	GA3*	GA3_VPX	
RowG7	TCK	N/C	
RowG8	GND	GND	
RowF1	Vs1	+12V	
RowF2	Vs1	+12V	
RowF3	Vs3	N/C	
RowF4	SM3	SM3_STAT_OUT	
RowF5	GA4*	GA4_VPX	
RowF6	GA2*	GA2_VPX	
RowF7	GND	GND	

P0 Connector Pin Location	P0 Connector Name	RPMG1-SVPX Name	Signal Type
RowF8	REF_CLK-	REF_CLK_2V5_N	
RowE1	Vs1	+12V	
RowE2	Vs1	+12V	
RowE3	Vs3	N/C	
RowE4	GND	GND	
RowE5	GND	GND	
RowE6	GND	GND	
RowE7	TDO	N/C	
RowE8	REF_CLK+	REF_CLK_2V5_P	
RowD1	No Pad*	N/C	
RowD2	No Pad*	N/C	
RowD3	No Pad*	N/C	
RowD4	-12V_Aux	-12V	
RowD5	3.3V_Aux	3.3V	
RowD6	+12V_Aux	N/C	
RowD7	TDI	N/C	
RowD8	GND	GND	
RowC1	Vs2	N/C	
RowC2	Vs2	N/C	
RowC3	Vs3	N/C	
RowC4	GND	GND	
RowC5	GND	GND	
RowC6	GND	GND	
RowC7	GND	GND	
RowC8	AUX_CLK-	AUX_CLK_2V5_N	
RowB1	Vs2	N/C	
RowB2	Vs2	N/C	
RowB3	Vs3	N/C	
RowB4	SYSRESET*	SYSRESET#	
RowB5	SM0	IPMI_SDA	
RowB6	GA1*	GA1_VPX	
RowB7	TMS	N/C	
RowB8	AUX_CLK+	AUX_CLK_2V5_P	
RowA1	Vs2	N/C	
RowA2	Vs2	N/C	
RowA3	Vs3	N/C	
RowA4	NVMRO	NVMRO	
RowA5	SM1	IPMI_SCL	
RowA6	GA0*	GA0_VPX	
RowA7	TRST*	N/C	
RowA8	GND	GND	

P1 Backplane Connector Signal/Pin Mapping

Connector Manufacturer: Smiths Interconnect

Manufacturer Part Number: KX1FCD02C1TBH-SL1

Mates with Backplane Connector Part Number: KX2FCU01C1TAH-SL1

Table 8. RPMG1-SVPX Module P1 Connector Pinout

Plug-In Module P1			Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	X8 x4 / 2x2 / 4x1	SYS_CONP*	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3			VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2		SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6			GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7			REF_CLK1-	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8			GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined		REF_CLK1+	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11			REF_CLK2-	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12			GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane		REF_CLK2+	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14			GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15			Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16			GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

The SpaceVPX Control Plane is implemented with a SpaceWire (SpW) and UART interface which is connected to the VC1902Processor.

The Data Plane is implemented with 4 Gigabit Ethernet Ports which include 2x TSN 1GbE and 2x 1000Base-X interfaces.

Table 9. RPMG1-SVPX Module P1 Connector Pinout and RPMG1-SVPX Signal Name

P1 Connector Pin Location	P1 Connector Name	RPMG1-SVPX Name	Signal Type
RowG1	SYS_CONP*	GND	
RowG2	GND	GND	
RowG3	VBAT	N/C	
RowG4	GND	GND	
RowG5	SYS_CON*	N/C	

P1 Connector Pin Location	P1 Connector Name	RPMG1-SVPX Name	Signal Type
RowG6	GND	GND	
RowG7	REF_CLK1-	CUSTOM_PULSE_1_N	
RowG8	GND	GND	
RowG9	REF_CLK1+	CUSTOM_PULSE_1_P	
RowG10	GND	GND	
RowG11	REF_CLK2-	CUSTOM_PULSE_2_N	
RowG12	GND	GND	
RowG13	REF_CLK2+	CUSTOM_PULSE_2_P	
RowG14	GND	GND	
RowG15	Maskable Reset*	N/C	
RowG16	GND	GND	
RowF1	GND	GND	
RowF2	DP01-TD1-	MEZ_SERDES_0_TX1_C_N	
RowF3	GND	GND	
RowF4	DP01-TD3-	MEZ_SERDES_0_TX3_C_N	
RowF5	GND	GND	
RowF6	DP02-TD1-	VPX_SERDES_5_TX1_C_N	
RowF7	GND	GND	
RowF8	DP02-TD3-	VPX_SERDES_5_TX3_C_N	
RowF9	GND	GND	
RowF10	UD	DP3_VPX_1V5_N	
RowF11	GND	GND	
RowF12	UD	DP6_VPX_1V5_N	
RowF13	GND	GND	
RowF14	CPtp02-DD-	DP6_VPX_2V5_N	
RowF15	GND	GND	
RowF16	CPtp01-DD-	DP7_VPX_2V5_N	
RowE1_Even	GND-J1	N/C	
RowE2_Even	DP01-TD1+	MEZ_SERDES_0_TX1_C_P	
RowE3_Even	GND-J1	N/C	
RowE4_Even	DP01-TD3+	MEZ_SERDES_0_TX3_C_P	
RowE5_Even	GND-J1	N/C	
RowE6_Even	DP02-TD1+	VPX_SERDES_5_TX1_C_P	
RowE7_Even	GND-J1	N/C	
RowE8_Even	DP02-TD3+	VPX_SERDES_5_TX3_C_P	
RowE9_Even	GND-J1	N/C	
RowE10_Even	UD	DP3_VPX_1V5_P	
RowE11_Even	GND-J1	N/C	
RowE12_Even	UD	DP6_VPX_1V5_P	
RowE13_Even	GND-J4	N/C	
RowE14_Even	CPtp02-DD+	DP6_VPX_2V5_P	
RowE15_Even	GND-J4	N/C	
RowE16_Even	CPtp01-DD+	DP7_VPX_2V5_P	
RowE1_Odd	DP01-TD0-	MEZ_SERDES_0_TX0_C_N	
RowE2_Odd	GND-J1	N/C	
RowE3_Odd	DP01-TD2-	MEZ_SERDES_0_TX2_C_N	
RowE4_Odd	GND-J1	N/C	
RowE5_Odd	DP02-TD0-	VPX_SERDES_5_TX0_C_N	

P1 Connector Pin Location	P1 Connector Name	RPMG1-SVPX Name	Signal Type
RowE6_Odd	GND-J1	N/C	
RowE7_Odd	DP02-TD2-	VPX_SERDES_5_TX2_C_N	
RowE8_Odd	GND-J1	N/C	
RowE9_Odd	UD	DP1_VPX_1V5_N	
RowE10_Odd	GND-J1	N/C	
RowE11_Odd	UD	DP5_VPX_1V5_N	
RowE12_Odd	GND-J1	N/C	
RowE13_Odd	CPtp02-DB-	DP2_VPX_2V5_N	
RowE14_Odd	GND-J4	N/C	
RowE15_Odd	CPtp01-DB-	DP3_VPX_2V5_N	
RowE16_Odd	GND-J4	N/C	
RowD1	DP01-TD0+	MEZ_SERDES_0_TX0_C_P	
RowD2	GND	GND	
RowD3	DP01-TD2+	MEZ_SERDES_0_TX2_C_P	
RowD4	GND	GND	
RowD5	DP02-TD0+	VPX_SERDES_5_TX0_C_P	
RowD6	GND	GND	
RowD7	DP02-TD2+	VPX_SERDES_5_TX2_C_P	
RowD8	GND	GND	
RowD9	UD	DP1_VPX_1V5_P	
RowD10	GND	GND	
RowD11	UD	DP5_VPX_1V5_P	
RowD12	GND	GND	
RowD13	CPtp02-DB+	DP2_VPX_2V5_P	
RowD14	GND	GND	
RowD15	CPtp01-DB+	DP3_VPX_2V5_P	
RowD16	GND	GND	
RowC1	GND	GND	
RowC2	DP01-RD1-	MEZ_SERDES_0_RX1_N	
RowC3	GND	GND	
RowC4	DP01-RD3-	MEZ_SERDES_0_RX3_N	
RowC5	GND	GND	
RowC6	DP02-RD1-	VPX_SERDES_5_RX1_N	
RowC7	GND	GND	
RowC8	DP02-RD3-	VPX_SERDES_5_RX3_N	
RowC9	GND	GND	
RowC10	UD	DP2_VPX_1V5_N	
RowC11	GND	GND	
RowC12	UD	REF_CLK_700MHZ_N	
RowC13	GND	GND	
RowC14	CPtp02-DC-	DP4_VPX_2V5_N	
RowC15	GND	GND	
RowC16	CPtp01-DC-	DP5_VPX_2V5_N	
RowB1_Even	GND-J1	N/C	
RowB2_Even	DP01-RD1+	MEZ_SERDES_0_RX1_P	
RowB3_Even	GND-J1	N/C	
RowB4_Even	DP01-RD3+	MEZ_SERDES_0_RX3_P	
RowB5_Even	GND-J1	N/C	

P1 Connector Pin Location	P1 Connector Name	RPMG1-SVPX Name	Signal Type
RowB6_Even	DP02-RD1+	VPX_SERDES_5_RX1_P	
RowB7_Even	GND-J1	N/C	
RowB8_Even	DP02-RD3+	VPX_SERDES_5_RX3_P	
RowB9_Even	GND-J1	N/C	
RowB10_Even	UD	DP2_VPX_1V5_P	
RowB11_Even	GND-J1	N/C	
RowB12_Even	UD	REF_CLK_700MHZ_P	
RowB13_Even	GND-J4	N/C	
RowB14_Even	CPtp02-DC+	DP4_VPX_2V5_P	
RowB15_Even	GND-J4	N/C	
RowB16_Even	CPtp01-DC+	DP5_VPX_2V5_P	
RowB1_Odd	DP01-RD0-	MEZ_SERDES_0_RX0_N	
RowB2_Odd	GND-J1	N/C	
RowB3_Odd	DP01-RD2-	MEZ_SERDES_0_RX2_N	
RowB4_Odd	GND-J1	N/C	
RowB5_Odd	DP02-RD0-	VPX_SERDES_5_RX0_N	
RowB6_Odd	GND-J1	N/C	
RowB7_Odd	DP02-RD2-	VPX_SERDES_5_RX2_N	
RowB8_Odd	GND-J1	N/C	
RowB9_Odd	UD	DP0_VPX_1V5_N	
RowB10_Odd	GND-J1	N/C	
RowB11_Odd	UD	DP4_VPX_1V5_N	
RowB12_Odd	GND-J1	N/C	
RowB13_Odd	CPtp02-DA-	DP0_VPX_2V5_N	
RowB14_Odd	GND-J4	N/C	
RowB15_Odd	CPtp01-DA-	DP1_VPX_2V5_N	
RowB16_Odd	GND-J4	N/C	
RowA1	DP01-RD0+	MEZ_SERDES_0_RX0_P	
RowA2	GND	GND	
RowA3	DP01-RD2+	MEZ_SERDES_0_RX2_P	
RowA4	GND	GND	
RowA5	DP02-RD0+	VPX_SERDES_5_RX0_P	
RowA6	GND	GND	
RowA7	DP02-RD2+	VPX_SERDES_5_RX2_P	
RowA8	GND	GND	
RowA9	UD	DP0_VPX_1V5_P	
RowA10	GND	GND	
RowA11	UD	DP4_VPX_1V5_P	
RowA12	GND	GND	
RowA13	CPtp02-DA+	DP0_VPX_2V5_P	
RowA14	GND	GND	
RowA15	CPtp01-DA+	DP1_VPX_2V5_P	
RowA16	GND	GND	

P2 Backplane

Connector Signal/Pin Mapping

Connector Manufacturer: Smiths Interconnect

Manufacturer Part Number: KX1FED02C1TBH-SL1 (Same as P1 Connector)

Mates with Backplane Connector Part Number: KX2FCU01C1TAH-SL1

Table 10. RPMG1-SVPX Module P2 Connector Pinout

Plug-In Module P2				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Expansion Plane X16 using [15:0]	x8 using[7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-TD-	EP00-TD+	GND	GND-J2	EP00-RD-	EP00-RD+
2				GND	EP01-TD-	EP01-TD+	GND-J2	GND	EP01-RD-	EP01-RD+	GND-J2	GND
3				UD	GND	GND-J2	EP02-TD-	EP02-TD+	GND	GND-J2	EP02-RD-	EP02-RD+
4				GND	EP03-TD-	EP03-TD+	GND-J2	GND	EP03-RD-	EP03-RD+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using [15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

Table 11. RPMG1-SVPX Module P2 Connector Pinout and RPMG1-SVPX Signal Name

P2 Connector Pin Location	P2 Connector Name	RPMG1-SVPX Name	Signal Type
RowG1	UD	UART_Tx_Versal	
RowG2	GND	GND	
RowG3	UD	UART_Rx_Versal	
RowG4	GND	GND	
RowG5	UD	UART_CFG_Versal	
RowG6	GND	GND	
RowG7	UD	UART_RSTn_Versal	
RowG8	GND	GND	
RowG9	UD	UART_Tx_uC	
RowG10	GND	GND	

P2 Connector Pin Location	P2 Connector Name	RPMG1-SVPX Name	Signal Type
RowG11	UD	UART_Rx_uC	
RowG12	GND	GND	
RowG13	UD	UART_CFG_uC	
RowG14	GND	GND	
RowG15	UD	UART_RSTn_uC	
RowG16	GND	GND	
RowF1	GND	GND	
RowF2	EP01-TD-	VPX_SERDES_4_TX1_C_N	
RowF3	GND	GND	
RowF4	EP03-TD-	VPX_SERDES_4_TX3_C_N	
RowF5	GND	GND	
RowF6	EP05-T-	VPX_SERDES_0_TX1_C_N	
RowF7	GND	GND	
RowF8	EP07-T-	VPX_SERDES_0_TX3_C_N	
RowF9	GND	GND	
RowF10	EP09-T-	VPX_SERDES_1_TX1_C_N	
RowF11	GND	GND	
RowF12	EP11-T-	VPX_SERDES_1_TX3_C_N	
RowF13	GND	GND	
RowF14	EP13-T-	VPX_SERDES_2_TX2_N	
RowF15	GND	GND	
RowF16	EP15-T-	VPX_SERDES_2_TX4_N	
RowE1_Even	GND-J2	N/C	
RowE2_Even	EP01-TD+	VPX_SERDES_4_TX1_C_P	
RowE3_Even	GND-J2	N/C	
RowE4_Even	EP03-TD+	VPX_SERDES_4_TX3_C_P	
RowE5_Even	GND-J2	N/C	
RowE6_Even	EP05-T+	VPX_SERDES_0_TX1_C_P	
RowE7_Even	GND-J2	N/C	
RowE8_Even	EP07-T+	VPX_SERDES_0_TX3_C_P	
RowE9_Even	GND-J2	N/C	
RowE10_Even	EP09-T+	VPX_SERDES_1_TX1_C_P	
RowE11_Even	GND-J2	N/C	
RowE12_Even	EP11-T+	VPX_SERDES_1_TX3_C_P	
RowE13_Even	GND-J2	N/C	
RowE14_Even	EP13-T+	VPX_SERDES_2_TX2_P	
RowE15_Even	GND-J2	N/C	
RowE16_Even	EP15-T+	VPX_SERDES_2_TX4_P	
RowE1_Odd	EP00-TD-	VPX_SERDES_4_TX0_C_N	
RowE2_Odd	GND-J2	N/C	
RowE3_Odd	EP02-TD-	VPX_SERDES_4_TX2_C_N	
RowE4_Odd	GND-J2	N/C	
RowE5_Odd	EP04-T-	VPX_SERDES_0_TX0_C_N	
RowE6_Odd	GND-J2	N/C	
RowE7_Odd	EP06-T-	VPX_SERDES_0_TX2_C_N	
RowE8_Odd	GND-J2	N/C	
RowE9_Odd	EP08-T-	VPX_SERDES_1_TX0_C_N	
RowE10_Odd	GND-J2	N/C	

P2 Connector Pin Location	P2 Connector Name	RPMG1-SVPX Name	Signal Type
RowE11_Odd	EP10-T-	VPX_SERDES_1_TX2_C_N	
RowE12_Odd	GND-J2	N/C	
RowE13_Odd	EP12-T-	VPX_SERDES_2_TX1_N	
RowE14_Odd	GND-J2	N/C	
RowE15_Odd	EP14-T-	VPX_SERDES_2_TX3_N	
RowE16_Odd	GND-J2	N/C	
RowD1	EP00-TD+	VPX_SERDES_4_TX0_C_P	
RowD2	GND	GND	
RowD3	EP02-TD+	VPX_SERDES_4_TX2_C_P	
RowD4	GND	GND	
RowD5	EP04-T+	VPX_SERDES_0_TX0_C_P	
RowD6	GND	GND	
RowD7	EP06-T+	VPX_SERDES_0_TX2_C_P	
RowD8	GND	GND	
RowD9	EP08-T+	VPX_SERDES_1_TX0_C_P	
RowD10	GND	GND	
RowD11	EP10-T+	VPX_SERDES_1_TX2_C_P	
RowD12	GND	GND	
RowD13	EP12-T+	VPX_SERDES_2_TX1_P	
RowD14	GND	GND	
RowD15	EP14-T+	VPX_SERDES_2_TX3_P	
RowD16	GND	GND	
RowC1	GND	GND	
RowC2	EP01-RD-	VPX_SERDES_4_RX1_N	
RowC3	GND	GND	
RowC4	EP03-RD-	VPX_SERDES_4_RX3_N	
RowC5	GND	GND	
RowC6	EP05-R-	VPX_SERDES_0_RX1_N	
RowC7	GND	GND	
RowC8	EP07-R-	VPX_SERDES_0_RX3_N	
RowC9	GND	GND	
RowC10	EP09-R-	VPX_SERDES_1_RX1_N	
RowC11	GND	GND	
RowC12	EP11-R-	VPX_SERDES_1_RX3_N	
RowC13	GND	GND	
RowC14	EP13-R-	VPX_SERDES_2_RX2_N	
RowC15	GND	GND	
RowC16	EP15-R-	VPX_SERDES_2_RX4_N	
RowB1_Even	GND-J2	N/C	
RowB2_Even	EP01-RD+	VPX_SERDES_4_RX1_P	
RowB3_Even	GND-J2	N/C	
RowB4_Even	EP03-RD+	VPX_SERDES_4_RX3_P	
RowB5_Even	GND-J2	N/C	
RowB6_Even	EP05-R+	VPX_SERDES_0_RX1_P	
RowB7_Even	GND-J2	N/C	
RowB8_Even	EP07-R+	VPX_SERDES_0_RX3_P	
RowB9_Even	GND-J2	N/C	
RowB10_Even	EP09-R+	VPX_SERDES_1_RX1_P	

P2 Connector Pin Location	P2 Connector Name	RPMG1-SVPX Name	Signal Type
RowB11_Even	GND-J2	N/C	
RowB12_Even	EP11-R+	VPX_SERDES_1_RX3_P	
RowB13_Even	GND-J2	N/C	
RowB14_Even	EP13-R+	VPX_SERDES_2_RX2_P	
RowB15_Even	GND-J2	N/C	
RowB16_Even	EP15-R+	VPX_SERDES_2_RX4_P	
RowB1_Odd	EP00-RD-	VPX_SERDES_4_RX0_N	
RowB2_Odd	GND-J2	N/C	
RowB3_Odd	EP02-RD-	VPX_SERDES_4_RX2_N	
RowB4_Odd	GND-J2	N/C	
RowB5_Odd	EP04-R-	VPX_SERDES_0_RX0_N	
RowB6_Odd	GND-J2	N/C	
RowB7_Odd	EP06-R-	VPX_SERDES_0_RX2_N	
RowB8_Odd	GND-J2	N/C	
RowB9_Odd	EP08-R-	VPX_SERDES_1_RX0_N	
RowB10_Odd	GND-J2	N/C	
RowB11_Odd	EP10-R-	VPX_SERDES_1_RX2_N	
RowB12_Odd	GND-J2	N/C	
RowB13_Odd	EP12-R-	VPX_SERDES_2_RX1_N	
RowB14_Odd	GND-J2	N/C	
RowB15_Odd	EP14-R-	VPX_SERDES_2_RX3_N	
RowB16_Odd	GND-J2	N/C	
RowA1	EP00-RD+	VPX_SERDES_4_RX0_P	
RowA2	GND	GND	
RowA3	EP02-RD+	VPX_SERDES_4_RX2_P	
RowA4	GND	GND	
RowA5	EP04-R+	VPX_SERDES_0_RX0_P	
RowA6	GND	GND	
RowA7	EP06-R+	VPX_SERDES_0_RX2_P	
RowA8	GND	GND	
RowA9	EP08-R+	VPX_SERDES_1_RX0_P	
RowA10	GND	GND	
RowA11	EP10-R+	VPX_SERDES_1_RX2_P	
RowA12	GND	GND	
RowA13	EP12-R+	VPX_SERDES_2_RX1_P	
RowA14	GND	GND	
RowA15	EP14-R+	VPX_SERDES_2_RX3_P	
RowA16	GND	GND	

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
12V VS1	12V Supply Input	11	13	Vdc
3.3V_AUX	3.3V Auxiliary Input	3	3.6	Vdc
SERDES data rate	Maximum SERDES Data Rate		5 (per lane)	Gsps
Storage Temp		-40	+105	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Mass			0.65 TBC	kg

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID		30	krads (Si)
nd-SEL Immunity		37	MeV-cm^2/mg
Total Single Event Rate Requiring External or Ground Intervention	Total System Level	1.80e-04	per year

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@ 30 °C (TBC @ 40 °C (TBC) @ 50 °C (TBC)	1,180,618 834,273 556,357	hours
Reliability (R)	3 years 5 years 7 years	0.968 0.946 0.926	

Acceptance Testing (FM3 Class C and FM4 Class D)

Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	

Qualification Testing

Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles
Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Functional Description

The Reconfigurable Processing Module for SpaceVPX (RPMG1-SVPX) input/output and connectivity capabilities are a central focus, enabling flexible development and system integration. The RPMG1-SVPX incorporates multiple interfaces, including Ethernet, USB, serial ports, and high-speed SERDES connections. These interfaces support communication, debugging, and programming functions, allowing developers to interact with the system efficiently.

Software BSP and Firmware Support

QuantumBSP (Board Support Package) is a modular, reusable design framework for embedded FPGA product development. It provides a standardized platform that unifies FPGA firmware, embedded software, and IP core structure, enabling scalable and maintainable designs across a variety of hardware configurations. The framework establishes a clean, well-defined interface between hardware logic, firmware control, and software abstraction layers. It supports advanced embedded processing across multiple FPGA families, including AMD Versal™, Lattice Avant-X™, and Microchip PolarFire®, enabling consistent performance, rapid bring-up, and streamlined maintenance across mission-critical product lines.

Mechanical Drawing

Placeholder (needs updated with latest information)

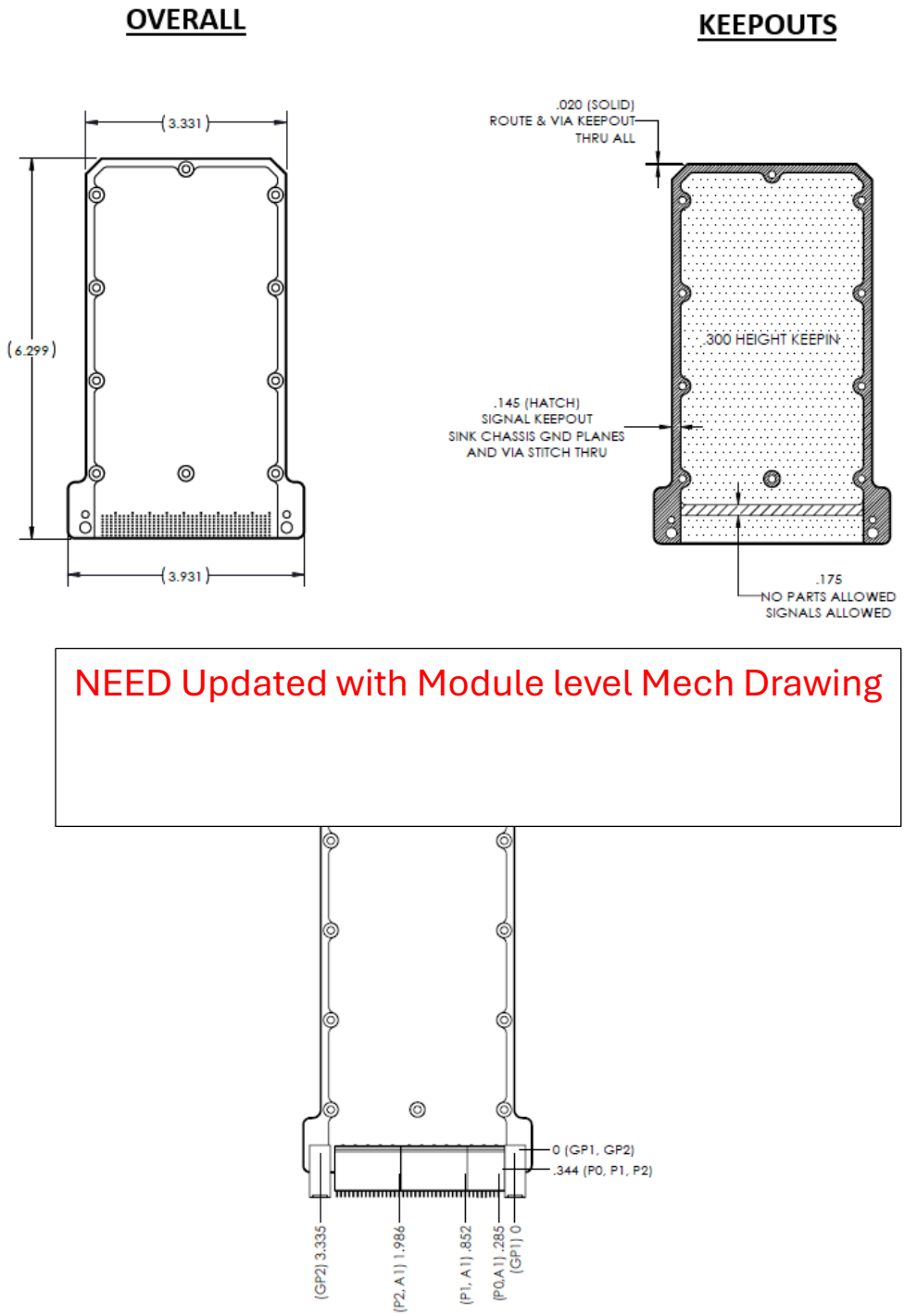


Figure 6. RPMG1-SVPX Mechanical Information

Revision History

Date	Rev	Author	Change Description	Page #
4/28/2026	1.0	DPA	Initial Preliminary Datasheet Draft	All

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
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Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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