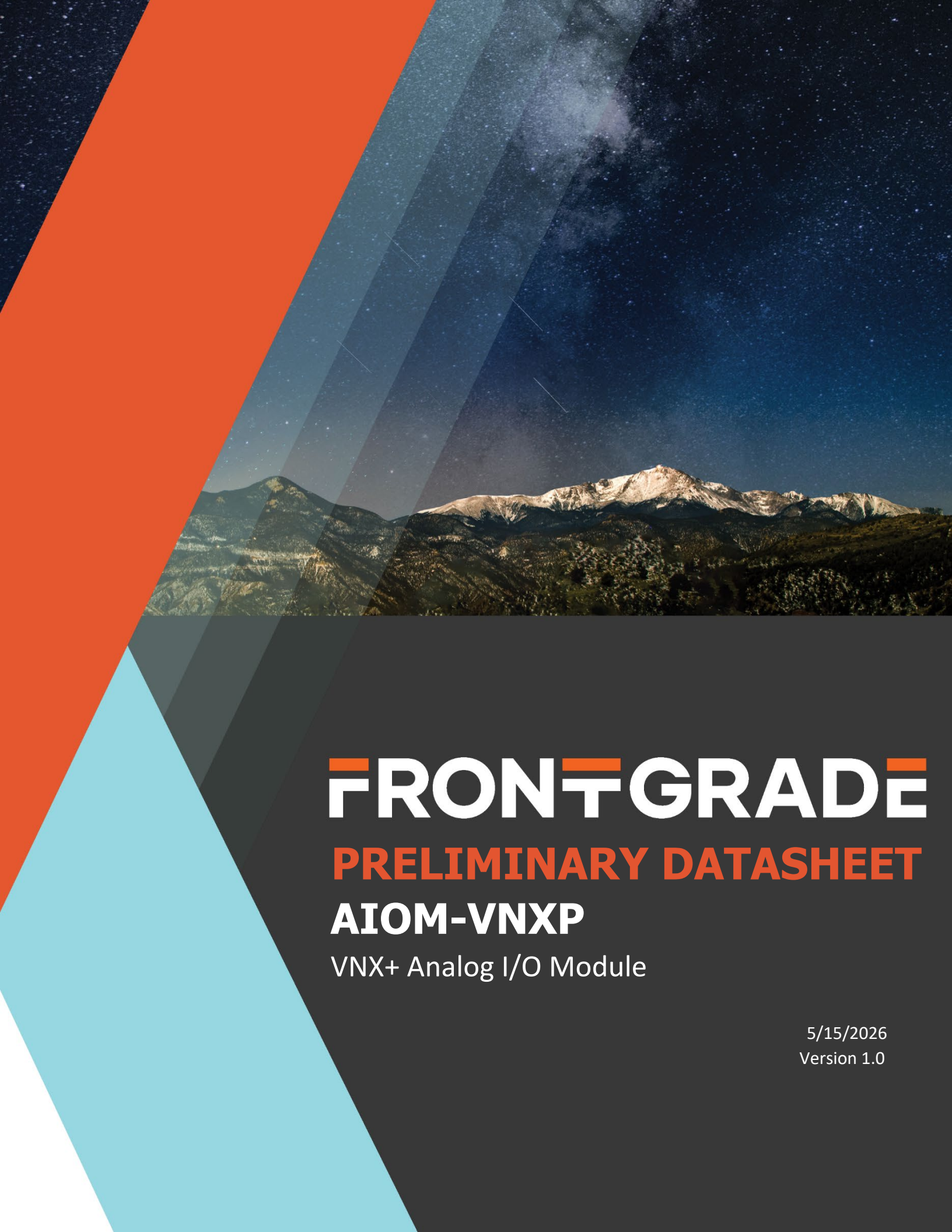




FRONTGRADE

PRELIMINARY DATASHEET

AIOM-VNXP

VNX+ Analog I/O Module

5/15/2026
Version 1.0



Introduction

The VNXP+ Analog I/O Module (AIOM-VNXP) is a high-performance RF Data Converter, enabling efficient conversion between analog signals and digital data. As a dual-channel analog front end, it supports both receive and transmit functions. On receive, it samples RF signals across UHF to X-Band and converts them into baseband digital data. On transmit, it digitally generates and upconverts signals for RF output, enabling flexible SDR processing and simplifying complex RF systems.

The module utilizes the advanced capabilities of the Texas Instruments' AFE7950 RF sampling transceiver, with dual ADC and DAC channels, and a dedicated observation channel for feedback. It supports up to 1200 MHz instantaneous bandwidth across a 650–8000 MHz frequency range and leverages high-speed JESD204C interfaces and integrated frequency synthesis. Packaged in a compact VNXP+ form factor, it is optimized for environments with radiation tolerance and controlled operating conditions, balancing high performance with efficient size, weight, and power (SWaP).

A key strength of the AIOM-VNXP is its ability to consolidate RF functionality into a single mixed-signal platform. By integrating RF sampling, digital up/down conversion, and multi-channel support, it reduces system complexity and shifts signal processing into software. This enables scalable, reconfigurable architectures' that can adapt to evolving mission requirements, while also reducing development time, cost, and risk associated with traditional RF hardware designs.

Supported by a broader MAMBA ecosystem, the product offers a competitive alternative to custom-built payloads and is positioned as a next-generation solution for flexible, high-performance RF mission architectures.

Applications

- Software-Defined Radios (SDR)
- Phased Array Antenna Systems
- Electronic Warfare (EW) & Signals Intelligence (SIGINT)
- Remote Sensing & Earth Observation
- Satellite Communications Payloads

Why it Matters

The **AIOM-VNXP** matters because it fundamentally **reduces the complexity, size, weight, and power demands** of **modern RF payloads** while **increasing flexibility and performance**. By consolidating multiple RF functions into a single, software-driven platform, it enables faster development cycles and lowers the cost and risk of deploying advanced systems. This allows operators to adapt to changing mission needs, support multi-band operations, and achieve higher data throughput without redesigning hardware, delivering a significant competitive and operational advantage.

Ordering Information

Ordering PN	Product Grade	Target Mission Class / Environment
AIOM-VNXP-OP-EDU	E = EDU/EM (Room Temp only)	Lab / Development Use Cases
AIOM-VNXP-OP-FM4	COTS Parts Grade (-10°C to +50°C)	Target Mission Class D
AIOM-VNXP-OP-FM3	Level 3 Parts Grade (-10°C to +50°C)	Target Mission Class C

Note: Frontgrade makes best effort to fit equivalent parts grading to build corresponding FM# level, but exceptions should be expected, particularly where Level 1 or Level 2 parts grades are not achievable/practical for standard hardware builds.

Features

RF Sampling Transceiver

- TI AFE7950 Integrated RF Transceiver
- Direct RF Sampling (650 MHz – 8 GHz)
- Integrated Digital Up/Down Conversion

Channel Configuration

- 2x ADCs (Receive Channels)
- 2x DACs (Transmit Channels)

Bandwidth & Performance

- 1200 MHz Instantaneous Bandwidth
- High Dynamic Range, Multi-Band Operation

High-Speed Interfaces

- 8x JESD204C SERDES Lanes (Full Duplex)
 - Max Lane Rate 17.4 Gbps
- 2x SPI (1.8V)
- 11x GPIO (1.8V)

RF & Clock Interfaces (VITA 90.2 interconnect)

- 2x Rx Coax Inputs
- 2x Tx Coax Outputs
- 1x External Reference Clock Input

Mechanical, Power & Environmental

- VNXP+ Form Factor: 89mm x 78mm x 19mm
- Mass: <388 g
- Power Dissipation: < 21W Max
- Operating Temp: -10°C to +50°C
- TID (TBC): Up to 30 krad(Si)
- SEL Immunity (TBC): < 37 MeV-cm²/mg

Block Diagram

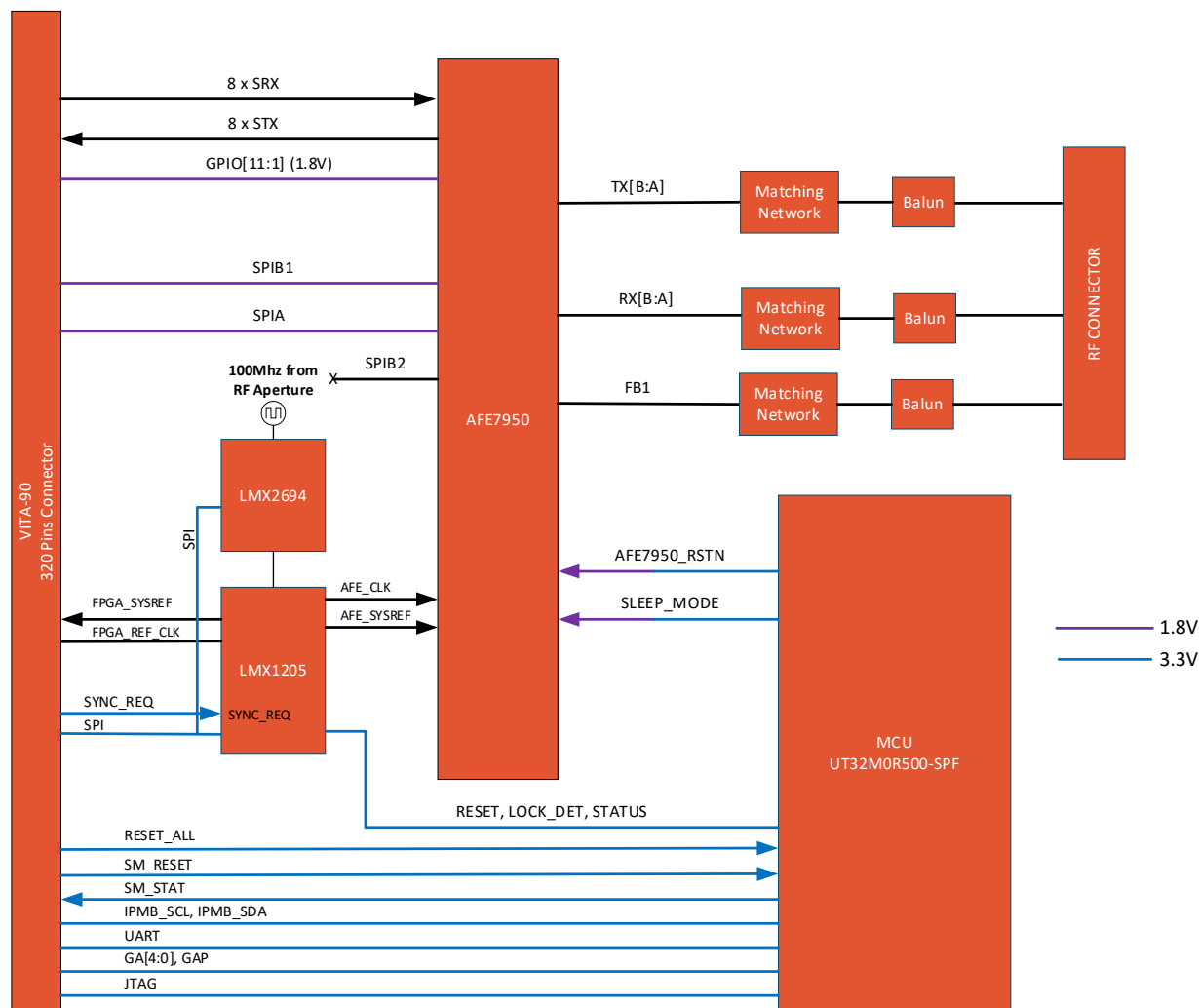


Figure 1. AIOM-VNXP Block Diagram

Backplane Slot Profile and Connection Tables

The AIOM-VNXP is a 19mm pitch VNX+ plug-in module (PIM). As such, the backplane interface is a single 320-pin connector based on Profile: VNX.PL-1-HH.320-8.2.2.1 in addition to a 10-pin RF aperture. The following represents the view of the connector.

Figure 2. 320-Pin Connector with 10-Pin RF aperture

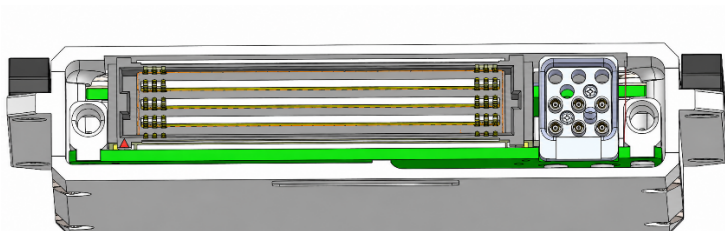


Figure 3. RF Aperture Pin Description



Table 1. RF Aperture Pinout

Position	AIOM-VNXP Name
A1	RXB_IN (RX 2)
A2	NC
A3	TXA (Tx2)
B1	RXA_IN (RX 1)
B2	EXT_100M (REF_CLK)
B3	TXA (Tx1)
C4	NC
D1	NC
D2	NC
D3	NC
GP	NC

Backplane and RF Aperture Connector Part Numbers

Table 2. 320-Pin Backplane Connector Part Numbers

Connector	Position	Part Number	Vendor
320-Pin Right-Angle (Tin-Lead)	Module	ASP-232973-01	SAMTEC
320-Pin Vertical (Tin-Lead)	Backplane	ASP-232972-01	SAMTEC

Table 3. 9-Pin RF Aperture Connector Part Numbers

Connector	Position	Part Number	Vendor
9-Pin RF Aperture	Module	RSP-233193-01	SAMTEC
9-Pin RF Aperture	Backplane	RSP-233192-01	SAMTEC

Backplane Connector Signal/Pin Mapping

Table 4. 320-pin Connector Pinout

RFFE-N Pinout			Revision: 0.16 Date: 2024-08-29	Title: User:	320-Pin Compute Module, Single Video, Mezz I/O												VITA 90.1 Slot Profile:				VITA 90 320-Pin I/O Intensive Compute Profile											
Row A			Row B			Row C			Row D			Row E			Row F			Row G			Row H			Row I								
Col	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Col							
1	Expansion	A1	JESD024 SR00 P	B1	GND	C1	JESD024 SR00 P	D1	GND	E1	JESD024 SR00 P	F1	GND	G1	GND	H1	+12V INPUT	I1	+12V INPUT	J1	GND	K1	GND	L1	GND	1						
2		A2	JESD024 SR00 N	B2	GND	C2	JESD024 SR00 N	D2	GND	E2	JESD024 SR00 N	F2	GND	G2	GND	H2		GND		2												
3		A3	JESD024 SR00 P	B3	GND	C3	JESD024 SR00 P	D3	GND	E3	JESD024 SR00 P	F3	GND	G3	GND	H3		GND		3												
4		A4	GND	B4	JESD024 SR00 N	C4	GND	D4	JESD024 SR00 N	E4	GND	F4	N/C	G4	N/C	H4		N/C		4												
5		A5	JESD024 SR00 P	B5	GND	C5	JESD024 SR00 P	D5	GND	E5	JESD024 SR00 P	F5	GND	G5	GND	H5		GND		5												
6		A6	JESD024 SR00 N	B6	GND	C6	JESD024 SR00 N	D6	GND	E6	JESD024 SR00 N	F6	GND	G6	GND	H6		GND		6												
7	Data	A7	GND	B7	N/C	C7	GND	D7	N/C	E7	GND	F7	N/C	G7	N/C	H7	N/A	I7	N/A	J7	N/A	K7	N/A	L7	N/A	7						
8		A8	GND	B8	N/C	C8	GND	D8	N/C	E8	GND	F8	N/C	G8	N/C	H8		GND		8												
9		A9	N/C	B9	GND	C9	N/C	D9	GND	E9	N/C	F9	GND	G9	N/C	H9		GND		9												
10		A10	N/C	B10	GND	C10	N/C	D10	GND	E10	N/C	F10	GND	G10	N/C	H10		GND		10												
11		A11	GND	B11	N/C	C11	N/C	D11	N/C	E11	N/C	F11	N/C	G11	N/C	H11		N/A		11												
12		A12	GND	B12	N/C	C12	N/C	D12	N/C	E12	N/C	F12	N/C	G12	N/C	H12		N/A		12												
13	Control	A13	N/C	B13	GND	C13	MI_RESET*	D13	GND	E13	N/C	F13	GND	G13	N/C	H13	N/A	I13	N/A	J13	N/A	K13	N/A	L13	N/A	13						
14		A14	N/C	B14	GND	C14	MI_STBY*	D14	GND	E14	N/C	F14	GND	G14	N/C	H14	N/A	I14	N/A	J14	N/A	K14	N/A	14								
15		A15	GND	B15	MIH_SCL	C15	GND	D15	MPI_RST_LIAR0	E15	GND	F15	N/C	G15	N/C	H15	GND	I15	GND	J15	GND	K15	GND	15								
16		A16	N/C	B16	GND	C16	JESD024 ST00 P	D16	GND	E16	N/C	F16	GND	G16	N/C	H16	N/A	I16	N/A	J16	N/A	K16	N/A	16								
17		A17	N/C	B17	GND	C17	JESD024 ST00 P	D17	GND	E17	N/C	F17	GND	G17	N/C	H17	N/A	I17	N/A	J17	N/A	K17	N/A	17								
18		A18	N/C	B18	GND	C18	JESD024 ST00 N	D18	GND	E18	N/C	F18	GND	G18	N/C	H18	GND	I18	N/A	J18	N/A	K18	N/A	L18	N/A	18						
19	Expansion	A19	GND	B19	JESD024 ST00 P	C19	GND	D19	JESD024 ST00 P	E19	GND	F19	N/C	G19	N/C	H19	GND	I19	N/A	J19	N/A	K19	N/A	L19	N/A	19						
20		A20	GND	B20	JESD024 ST00 P	C20	GND	D20	JESD024 ST00 N	E20	GND	F20	N/C	G20	N/C	H20	GND	I20	N/A	J20	N/A	K20	N/A	L20	N/A	20						
21		A21	GND	B21	JESD024 ST00 P	C21	GND	D21	JESD024 ST00 P	E21	GND	F21	N/C	G21	N/C	H21	GND	I21	N/A	J21	N/A	K21	N/A	L21	N/A	21						
22		A22	GND	B22	JESD024 ST00 N	C22	GND	D22	JESD024 ST00 P	E22	GND	F22	N/C	G22	N/C	H22	GND	I22	N/A	J22	N/A	K22	N/A	L22	N/A	22						
23		A23	GND	B23	JESD024 ST00 P	C23	GND	D23	JESD024 ST00 N	E23	GND	F23	N/C	G23	N/C	H23	GND	I23	N/A	J23	N/A	K23	N/A	L23	N/A	23						
24		A24	GND	B24	JESD024 ST00 N	C24	GND	D24	JESD024 ST00 P	E24	GND	F24	N/C	G24	N/C	H24	GND	I24	N/A	J24	N/A	K24	N/A	L24	N/A	24						
25	Data	A25	N/C	B25	GND	C25	N/C	D25	GND	E25	N/C	F25	GND	G25	N/C	H25	GND	I25	N/A	J25	N/A	K25	N/A	L25	N/A	25						
26		A26	N/C	B26	GND	C26	N/C	D26	GND	E26	N/C	F26	GND	G26	N/C	H26	GND	I26	N/A	J26	N/A	K26	N/A	L26	N/A	26						
27		A27	GND	B27	N/C	C27	N/C	D27	GND	E27	N/C	F27	GND	G27	N/C	H27	GND	I27	N/A	J27	N/A	K27	N/A	L27	N/A	27						
28		A28	GND	B28	N/C	C28	N/C	D28	GND	E28	N/C	F28	GND	G28	N/C	H28	GND	I28	N/A	J28	N/A	K28	N/A	L28	N/A	28						
29		A29	N/C	B29	GND	C29	N/C	D29	GND	E29	N/C	F29	GND	G29	N/C	H29	GND	I29	N/A	J29	N/A	K29	N/A	L29	N/A	29						
30		A30	N/C	B30	GND	C30	N/C	D30	GND	E30	N/C	F30	GND	G30	N/C	H30	GND	I30	N/A	J30	N/A	K30	N/A	L30	N/A	30						
31	Control	A31	GND	B31	MUTL_CLK_P	C31	GND	D31	AFE_GPO 4, 1.8	E31	GND	F31	ITAG_TRST*	G31	GND	H31	ITAG_TCK	I31	ITAG_TDI	J31	ITAG_TDO	K31	ITAG_TDO	L31	ITAG_TDO	31						
32		A32	GND	B32	MUTL_CLK_N	C32	GND	D32	AFE_GPO 5, 1.8	E32	GND	F32	ITAG_Select-NC	G32	GND	H32	ITAG_TCK	I32	ITAG_TDI	J32	ITAG_TDO	K32	ITAG_TDO	L32	ITAG_TDO	32						
33		A33	N/C	B33	GND	C33	DCCLK_P	D33	AFE_GPO 0, 1.8	E33	GND	F33	AFE_GPO 0, 1.8	G33	AFE_GPO 0, 1.8	H33	ITAG_TCK	I33	ITAG_TDI	J33	ITAG_TDO	K33	ITAG_TDO	L33	ITAG_TDO	33						
34		A34	N/C	B34	GND	C34	DCCLK_N	D34	AFE_GPO 1, 1.8	E34	GND	F34	AFE_GPO 1, 1.8	G34	AFE_GPO 1, 1.8	H34	ITAG_TCK	I34	ITAG_TDI	J34	ITAG_TDO	K34	ITAG_TDO	L34	ITAG_TDO	34						
35		A35	GND	B35	SYNREF_P	C35	GND	D35	AFE_GPO 6, 1.8	E35	GND	F35	MCU_GPO 2, 3.3	G35	MCU_GPO 2, 3.3	H35	AFE_SPM_CLK, 1.8	I35	AFE_SPM_CLK, 1.8	J35	AFE_SPM_CLK, 1.8	K35	AFE_SPM_CLK, 1.8	L35	AFE_SPM_CLK, 1.8	35						
36		A36	GND	B36	SYNREF_N	C36	GND	D36	AFE_GPO 7, 1.8	E36	GND	F36	MCU_GPO 3, 3.3	G36	MCU_GPO 3, 3.3	H36	AFE_SPM_CLK, 1.8	I36	AFE_SPM_CLK, 1.8	J36	AFE_SPM_CLK, 1.8	K36	AFE_SPM_CLK, 1.8	L36	AFE_SPM_CLK, 1.8	36						
37	Control	A37	N/C	B37	GND	C37	AFE_GPO 15, 1.8	D37	AFE_GPO 1, 1.8	E37	AFE_GPO 2, 1.8	F37	AFE_GPO 3, 1.8	G37	AFE_SPM_CLK, 1.8	H37	AFE_SPM_CLK, 1.8	I37	AFE_SPM_CLK, 1.8	J37	AFE_SPM_CLK, 1.8	K37	AFE_SPM_CLK, 1.8	L37	AFE_SPM_CLK, 1.8	37						
38		A38	N/C	B38	GND	C38	LMX2664_SYNC_3,3	D38	AFE_GPO 3, 1.8	E38	AFE_GPO 4, 1.8	F38	AFE_SPM_CLK, 1.8	G38	AFE_SPM_CLK, 1.8	H38	AFE_SPM_CLK, 1.8	I38	AFE_SPM_CLK, 1.8	J38	AFE_SPM_CLK, 1.8	K38	AFE_SPM_CLK, 1.8	L38	AFE_SPM_CLK, 1.8	38						
39		A39	GND	B39	VSYSREF_RED_P	C39	GND	D39	AFE_GPO 8, 1.8	E39	AFE_GPO 5, 1.8	F39	AFE_SPM_CLK, 1.8	G39	AFE_SPM_CLK, 1.8	H39	AFE_SPM_CLK, 1.8	I39	AFE_SPM_CLK, 1.8	J39	AFE_SPM_CLK, 1.8	K39	AFE_SPM_CLK, 1.8	L39	AFE_SPM_CLK, 1.8	39						
40		A40	GND	B40	VSYSREF_RED_N	C40	GND	D40	AFE_GPO 9, 1.8	E40	AFE_GPO 6, 1.8	F40	AFE_SPM_CLK, 1.8	G40	AFE_SPM_CLK, 1.8	H40	AFE_SPM_CLK, 1.8	I40	AFE_SPM_CLK, 1.8	J40	AFE_SPM_CLK, 1.8	K40	AFE_SPM_CLK, 1.8	L40	AFE_SPM_CLK, 1.8	40						
41		A41	N/C	B41	GND	C41	VSYSREF_RED_P	D41	AFE_GPO 10, 1.8	E41	AFE_GPO 7, 1.8	F41	AFE_SPM_CLK, 1.8	G41	AFE_SPM_CLK, 1.8	H41	AFE_SPM_CLK, 1.8	I41	AFE_SPM_CLK, 1.8	J41	AFE_SPM_CLK, 1.8	K41	AFE_SPM_CLK, 1.8	L41	AFE_SPM_CLK, 1.8	41						
42		A42	N/C	B42	GND	C42	VSYSREF_RED_N	D42	AFE_GPO 11, 1.8	E42	AFE_GPO 8, 1.8	F42	AFE_SPM_CLK, 1.8	G42	AFE_SPM_CLK, 1.8	H42	AFE_SPM_CLK, 1.8	I42	AFE_SPM_CLK, 1.8	J42	AFE_SPM_CLK, 1.8	K42	AFE_SPM_CLK, 1.8	L42	AFE_SPM_CLK, 1.8	42						

Backplane Pin list / Cross Reference

Table 5. 320-pin Connector, ROW A

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW A	Expansion	A1	EP1_RX0_P	JESD204_SRX0_P
2	ROW A	Expansion	A2	EP1_RX0_N	JESD204_SRX0_N
3	ROW A	Expansion	A3	GND	GND
4	ROW A	Expansion	A4	GND	GND
5	ROW A	Expansion	A5	EP1_RX1_P	JESD204_SRX1_P
6	ROW A	Expansion	A6	EP1_RX1_N	JESD204_SRX1_N
7	ROW A	Data	A7	GND	GND
8	ROW A	Data	A8	GND	GND
9	ROW A	Data	A9	DP1_RX0_P	N/C
10	ROW A	Data	A10	DP1_RX0_N	N/C
11	ROW A	Data	A11	GND	GND
12	ROW A	Data	A12	GND	GND
13	ROW A	Control	A13	CP1_RX0_P	N/C
14	ROW A	Control	A14	CP1_RX0_N	N/C
15	ROW A	Control	A15	GND	GND
16	ROW A	Control	A16	GND	GND
17	ROW A	Control	A17	CP1_TX0_P	N/C
18	ROW A	Control	A18	CP1_TX0_N	N/C
19	ROW A	Expansion	A19	GND	GND
20	ROW A	Expansion	A20	GND	GND
21	ROW A	Expansion	A21	EP1_TX0_P	JESD204_STX0_P
22	ROW A	Expansion	A22	EP1_TX0_N	JESD204_STX0_N
23	ROW A	Expansion	A23	GND	GND
24	ROW A	Expansion	A24	GND	GND
25	ROW A	Data	A25	DP1_TX0_P	N/C
26	ROW A	Data	A26	DP1_TX0_N	N/C
27	ROW A	Data	A27	GND	GND
28	ROW A	Data	A28	GND	GND
29	ROW A	Data	A29	DP1_TX1_P	N/C
30	ROW A	Data	A30	DP1_TX1_N	N/C
31	ROW A	Control	A31	GND	GND
32	ROW A	Control	A32	GND	GND
33	ROW A	Control	A33	CP2_TX0_P	N/C
34	ROW A	Control	A34	CP2_TX0_N	N/C
35	ROW A	Control	A35	GND	GND
36	ROW A	Control	A36	GND	GND

37	ROW A	Control	A37	CP2_RX0_P	N/C
38	ROW A	Control	A38	CP2_RX0_N	N/C
39	ROW A	Control	A39	GND	GND
40	ROW A	Control	A40	GND	GND

Table 6. 320-pin Connector, ROW B

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW B	Expansion	B1	GND	GND
2	ROW B	Expansion	B2	GND	GND
3	ROW B	Expansion	B3	EP1_RX2_P	JESD204_SRX2_P
4	ROW B	Expansion	B4	EP1_RX2_N	JESD204_SRX2_N
5	ROW B	Expansion	B5	GND	GND
6	ROW B	Expansion	B6	GND	GND
7	ROW B	Data	B7	DP1_RX1_P	N/C
8	ROW B	Data	B8	DP1_RX1_N	N/C
9	ROW B	Data	B9	GND	GND
10	ROW B	Data	B10	GND	GND
11	ROW B	Data	B11	DP1_RX2_P	N/C
12	ROW B	Data	B12	DP1_RX2_N	N/C
13	ROW B	Utility	B13	GND	GND
14	ROW B	Utility	B14	GND	GND
15	ROW B	Utility	B15	SMA_SCL	SMA_SCL
16	ROW B	Utility	B16	SMA_SDA	SMA_SDA
17	ROW B	Expansion	B17	GND	GND
18	ROW B	Expansion	B18	GND	GND
19	ROW B	Expansion	B19	EP1_TX1_P	JESD204_STX1_P
20	ROW B	Expansion	B20	EP1_TX1_N	JESD204_STX1_N
21	ROW B	Expansion	B21	GND	GND
22	ROW B	Expansion	B22	GND	GND
23	ROW B	Expansion	B23	EP1_TX2_P	JESD204_STX2_P
24	ROW B	Expansion	B24	EP1_TX2_N	JESD204_STX2_N
25	ROW B	Data	B25	GND	GND
26	ROW B	Data	B26	GND	GND
27	ROW B	Data	B27	DP1_TX2_P	N/C
28	ROW B	Data	B28	DP1_TX2_N	N/C
29	ROW B	Data	B29	GND	GND
30	ROW B	Data	B30	GND	GND
31	ROW B	Overlay	B31	VID1_D1_P	MGT1_CLK_P
32	ROW B	Overlay	B32	VID1_D1_N	MGT1_CLK_N
33	ROW B	Overlay	B33	GND	GND
34	ROW B	Overlay	B34	GND	GND
35	ROW B	Overlay	B35	VID1_D2_P	SYSREF_P
36	ROW B	Overlay	B36	VID1_D2_N	SYSREF_N
37	ROW B	Overlay	B37	GND	GND
38	ROW B	Overlay	B38	GND	GND

39	ROW B	Overlay	B39	VID1_D3_P	SYSREF_REQ_P
40	ROW B	Overlay	B40	VID1_D3_N	SYSREF_REQ_N

Table 7. 320-pin Connector, ROW C

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW C	Expansion	C1	EP1_RX3_P	JESD204_SRX3_P
2	ROW C	Expansion	C2	EP1_RX3_N	JESD204_SRX3_N
3	ROW C	Expansion	C3	GND	GND
4	ROW C	Expansion	C4	GND	GND
5	ROW C	Expansion	C5	EP1_RX4_P	JESD204_SRX4_P
6	ROW C	Expansion	C6	EP1_RX4_N	JESD204_SRX4_N
7	ROW C	Data	C7	GND	GND
8	ROW C	Data	C8	GND	GND
9	ROW C	Data	C9	DP1_RX3_P	N/C
10	ROW C	Data	C10	DP1_RX3_N	N/C
11	ROW C	Data	C11	GND	GND
12	ROW C	Data	C12	GND	GND
13	ROW C	Utility	C13	SMB_SCL	SM_RESET*
14	ROW C	Utility	C14	SMB_SDA	SM_STAT*
15	ROW C	Utility	C15	GND	GND
16	ROW C	Utility	C16	GND	GND
17	ROW C	Expansion	C17	EP1_TX3_P	JESD204_STX3_P
18	ROW C	Expansion	C18	EP1_TX3_N	JESD204_STX3_N
19	ROW C	Expansion	C19	GND	GND
20	ROW C	Expansion	C20	GND	GND
21	ROW C	Expansion	C21	EP1_TX4_P	JESD204_STX4_P
22	ROW C	Expansion	C22	EP1_TX4_N	JESD204_STX4_N
23	ROW C	Expansion	C23	GND	GND
24	ROW C	Expansion	C24	GND	GND
25	ROW C	Data	C25	DP1_TX3_P	N/C
26	ROW C	Data	C26	DP1_TX3_N	N/C
27	ROW C	Data	C27	GND	GND
28	ROW C	Data	C28	GND	GND
29	ROW C	Data	C29	DP2_TX0_P	N/C
30	ROW C	Data	C30	DP2_TX0_N	N/C
31	ROW C	Overlay	C31	GND	GND
32	ROW C	Overlay	C32	GND	GND
33	ROW C	Overlay	C33	PP1_TX1_P	DCLK0_P
34	ROW C	Overlay	C34	PP1_TX1_N	DCLK0_N
35	ROW C	Overlay	C35	GND	GND
36	ROW C	Overlay	C36	GND	GND
37	ROW C	Overlay	C37	PP1_RX1_P	AFE_GPIO_10_1.8
38	ROW C	Overlay	C38	PP1_RX1_N	LMX2694_SYNC_3.3

39	ROW C	Overlay	C39	GND	GND
40	ROW C	Overlay	C40	GND	GND

Table 8. 320-pin Connector, ROW D

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW D	Expansion	D1	GND	GND
2	ROW D	Expansion	D2	GND	GND
3	ROW D	Expansion	D3	EP1_RX5_P	JESD204_SRX5_P
4	ROW D	Expansion	D4	EP1_RX5_N	JESD204_SRX5_N
5	ROW D	Expansion	D5	GND	GND
6	ROW D	Expansion	D6	GND	GND
7	ROW D	Data	D7	DP2_RX0_P	N/C
8	ROW D	Data	D8	DP2_RX0_N	N/C
9	ROW D	Data	D9	GND	GND
10	ROW D	Data	D10	GND	GND
11	ROW D	Data	D11	DP2_RX1_P	N/C
12	ROW D	Data	D12	DP2_RX1_N	N/C
13	ROW D	Utility	D13	GND	GND
14	ROW D	Utility	D14	GND	GND
15	ROW D	Utility	D15	MP1_RXD	MP1_RXD - UART0
16	ROW D	Utility	D16	MP1_TXD	MP1_TXD - UART0
17	ROW D	Expansion	D17	GND	GND
18	ROW D	Expansion	D18	GND	GND
19	ROW D	Expansion	D19	EP1_TX5_P	JESD204_STX5_P
20	ROW D	Expansion	D20	EP1_TX5_N	JESD204_STX5_N
21	ROW D	Expansion	D21	GND	GND
22	ROW D	Expansion	D22	GND	GND
23	ROW D	Expansion	D23	EP1_TX6_P	JESD204_STX6_P
24	ROW D	Expansion	D24	EP1_TX6_N	JESD204_STX6_N
25	ROW D	Data	D25	GND	GND
26	ROW D	Data	D26	GND	GND
27	ROW D	Data	D27	DP2_TX1_P	N/C
28	ROW D	Data	D28	DP2_TX1_N	N/C
29	ROW D	Data	D29	GND	GND
30	ROW D	Data	D30	GND	GND
31	ROW D	Overlay	D31	PP1_TX2_P	AFE_GPIO_4_1.8
32	ROW D	Overlay	D32	PP1_TX2_N	AFE_GPIO_5_1.8
33	ROW D	Overlay	D33	GND	GND
34	ROW D	Overlay	D34	GND	GND
35	ROW D	Overlay	D35	PP1_RX2_P	AFE_GPIO_6_1.8
36	ROW D	Overlay	D36	PP1_RX2_N	AFE_GPIO_7_1.8
37	ROW D	Overlay	D37	GND	GND
38	ROW D	Overlay	D38	GND	GND

39	ROW D	Overlay	D39	VID1_D0_P	AFE_GPIO_8_1.8
40	ROW D	Overlay	D40	VID1_D0_N	AFE_GPIO_9_1.8

Table 9. 320-pin Connector, ROW E

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW E	Expansion	E1	EP1_RX6_P	JESD204_SRX6_P
2	ROW E	Expansion	E2	EP1_RX6_N	JESD204_SRX6_N
3	ROW E	Expansion	E3	GND	GND
4	ROW E	Expansion	E4	GND	GND
5	ROW E	Expansion	E5	EP1_RX7_P	JESD204_SRX7_P
6	ROW E	Expansion	E6	EP1_RX7_N	JESD204_SRX7_N
7	ROW E	Data	E7	GND	GND
8	ROW E	Data	E8	GND	GND
9	ROW E	Data	E9	DP2_RX2_P	N/C
10	ROW E	Data	E10	DP2_RX2_N	N/C
11	ROW E	Data	E11	GND	GND
12	ROW E	Data	E12	GND	GND
13	ROW E	Data	E13	DP2_RX3_P	N/C
14	ROW E	Data	E14	DP2_RX3_N	N/C
15	ROW E	Utility	E15	GND	GND
16	ROW E	Utility	E16	GND	GND
17	ROW E	Utility	E17	REFCLK_P	N/C
18	ROW E	Utility	E18	REFCLK_N	N/C
19	ROW E	Expansion	E19	GND	GND
20	ROW E	Expansion	E20	GND	GND
21	ROW E	Expansion	E21	EP1_TX7_P	JESD204_STX7_P
22	ROW E	Expansion	E22	EP1_TX7_N	JESD204_STX7_N
23	ROW E	Expansion	E23	GND	GND
24	ROW E	Expansion	E24	GND	GND
25	ROW E	Data	E25	DP2_TX2_P	N/C
26	ROW E	Data	E26	DP2_TX2_N	N/C
27	ROW E	Data	E27	GND	GND
28	ROW E	Data	E28	GND	GND
29	ROW E	Data	E29	DP2_TX3_P	N/C
30	ROW E	Data	E30	DP2_TX3_N	N/C
31	ROW E	Overlay	E31	GND	GND
32	ROW E	Overlay	E32	GND	GND
33	ROW E	Overlay	E33	USB2SS_TX_P	AFE_GPIO_0_1.8
34	ROW E	Overlay	E34	USB2SS_TX_N	AFE_GPIO_1_1.8
35	ROW E	Overlay	E35	GND	GND
36	ROW E	Overlay	E36	GND	GND
37	ROW E	Overlay	E37	USB2SS_RX_P	AFE_GPIO_2_1.8
38	ROW E	Overlay	E38	USB2SS_RX_N	AFE_GPIO_3_1.8

39	ROW E	Overlay	E39	GND	GND
40	ROW E	Overlay	E40	GND	GND

Table 10. 320-pin Connector, ROW F

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW F	Utility	F1	GND	GND
2	ROW F	Utility	F2	GND	GND
3	ROW F	Utility	F3	GBE1_MDI0_P	N/C
4	ROW F	Utility	F4	GBE1_MDI0_N	N/C
5	ROW F	Utility	F5	GND	GND
6	ROW F	Utility	F6	GND	GND
7	ROW F	Utility	F7	GBE1_MDI1_P	N/C
8	ROW F	Utility	F8	GBE1_MDI1_N	N/C
9	ROW F	Utility	F9	GND	GND
10	ROW F	Utility	F10	GND	GND
11	ROW F	Utility	F11	GBE1_MDI2_P	N/C
12	ROW F	Utility	F12	GBE1_MDI2_N	N/C
13	ROW F	Utility	F13	GND	GND
14	ROW F	Utility	F14	GND	GND
15	ROW F	Utility	F15	GBE1_MDI3_P	N/C
16	ROW F	Utility	F16	GBE1_MDI3_N	N/C
17	ROW F	Utility	F17	GND	GND
18	ROW F	Utility	F18	GND	GND
19	ROW F	Utility	F19	AUXCLK_P	N/C
20	ROW F	Utility	F20	AUXCLK_N	N/C
21	ROW F	Utility	F21	GND	GND
22	ROW F	Utility	F22	GND	GND
23	ROW F	Utility	F23	USB1_D_P	N/C
24	ROW F	Utility	F24	USB1_D_N	N/C
25	ROW F	Utility	F25	GND	GND
26	ROW F	Utility	F26	GND	GND
27	ROW F	Utility	F27	GPLVDS1_P	N/C
28	ROW F	Utility	F28	GPLVDS1_N	N/C
29	ROW F	Utility	F29	GND	GND
30	ROW F	Utility	F30	GND	GND
31	ROW F	Overlay	F31	RFU	JTAG - TRST*
32	ROW F	Overlay	F32	RFU	JTAG - Select - NC
33	ROW F	Overlay	F33	GND	GND
34	ROW F	Overlay	F34	GND	GND
35	ROW F	Overlay	F35	RFU	MCU_GPIO_2_3.3
36	ROW F	Overlay	F36	RFU	MCU_GPIO_3_3.3
37	ROW F	Overlay	F37	GND	GND
38	ROW F	Overlay	F38	GND	GND

39	ROW F	Overlay	F39	USB2_D_P	AFE_SPIB_MOSI_1.8
40	ROW F	Overlay	F40	USB2_D_N	AFE_SPIB_MISO_1.8

Table 11. 320-pin Connector, ROW G

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW G	Utility	G1	VS1	+12V_INPUT
2	ROW G	Utility	G2	VS1	+12V_INPUT
3	ROW G	Utility	G3	VS1	+12V_INPUT
4	ROW G	Utility	G4	VS1	+12V_INPUT
5	ROW G	Utility	G5	GND	GND
6	ROW G	Utility	G6	VS2	N/C
7	ROW G	Utility	G7	VS2	N/C
8	ROW G	Utility	G8	VS2	N/C
9	ROW G	Utility	G9	VS2	N/C
10	ROW G	Utility	G10	GND	GND
11	ROW G	Utility	G11	VS3	N/C
12	ROW G	Utility	G12	VS3	N/C
13	ROW G	Utility	G13	VS4	N/C
14	ROW G	Utility	G14	VAUX	VAUX
15	ROW G	Utility	G15	GND	GND
16	ROW G	Utility	G16	UEIO0	UEIO0_3.3 - SPI_CLK
17	ROW G	Utility	G17	UEIO1	UEIO1_3.3 - SPI_MOSI
18	ROW G	Utility	G18	UEIO2	UEIO2_3.3 - SPI_MISO
19	ROW G	Utility	G19	GND	GND
20	ROW G	Utility	G20	UEIO3	UEIO3_3.3 - SPI_CS_2694
21	ROW G	Utility	G21	UEIO4	UEIO4_3.3 - SPI_CS_1205
22	ROW G	Utility	G22	UEIO5	N/C
23	ROW G	Utility	G23	GND	GND
24	ROW G	Utility	G24	UEIO6	N/C
25	ROW G	Utility	G25	UEIO7	N/C
26	ROW G	Utility	G26	USB1_VBUS	N/C
27	ROW G	Utility	G27	GND	GND
28	ROW G	Utility	G28	GDISCRETE1	GDISCRETE1 - (MR*)
29	ROW G	Utility	G29	GPIO1	MCU_GPIO_0_3.3
30	ROW G	Utility	G30	GPIO2	MCU_GPIO_1_3.3
31	ROW G	Overlay	G31	GND	GND
32	ROW G	Overlay	G32	GND	GND
33	ROW G	Overlay	G33	RFU	JTAG - TMS
34	ROW G	Overlay	G34	RFU	JTAG - TDO
35	ROW G	Overlay	G35	GND	GND
36	ROW G	Overlay	G36	GND	GND
37	ROW G	Overlay	G37	RFU	AFE_SPIB_CLK_1.8
38	ROW G	Overlay	G38	RFU	AFE_SPIB_CS_1.8

39	ROW G	Overlay	G39	GND	GND
40	ROW G	Overlay	G40	GND	GND

Table 12. 320-pin Connector, ROW H

Column	Row	Plane	Vita 90 Pin	VITA 90 Connector Pin Name	AIOM-VNXP Name
1	ROW H	Utility	H1	VS1	+12V_INPUT
2	ROW H	Utility	H2	VS1	+12V_INPUT
3	ROW H	Utility	H3	VS1	+12V_INPUT
4	ROW H	Utility	H4	VS1	+12V_INPUT
5	ROW H	Utility	H5	GND	GND
6	ROW H	Utility	H6	VS2	N/C
7	ROW H	Utility	H7	VS2	N/C
8	ROW H	Utility	H8	VS2	N/C
9	ROW H	Utility	H9	VS2	N/C
10	ROW H	Utility	H10	GND	GND
11	ROW H	Utility	H11	VS3	N/C
12	ROW H	Utility	H12	VS3	N/C
13	ROW H	Utility	H13	VHEATER	N/C
14	ROW H	Utility	H14	VBAT_3V	N/C
15	ROW H	Utility	H15	GND	GND
16	ROW H	Utility	H16	NVMRO	N/A
17	ROW H	Utility	H17	SYSRESET*	SYSRESET_B
18	ROW H	Utility	H18	GND	GND
19	ROW H	Utility	H19	SER1_RX_P	MCU_RXD_UART1
20	ROW H	Utility	H20	SER1_RX_N	SER1_RX_N - NC
21	ROW H	Utility	H21	SER1_TX_P	MCU_TXD_UART1
22	ROW H	Utility	H22	SER1_TX_N	SER1_TX_N - NC
23	ROW H	Utility	H23	GND	GND
24	ROW H	Utility	H24	GA0*	GA0
25	ROW H	Utility	H25	GA1*	GA1
26	ROW H	Utility	H26	GA2*	GA2
27	ROW H	Utility	H27	GA3*	GA3
28	ROW H	Utility	H28	GA4*	GA4
29	ROW H	Utility	H29	GAP*	GAP
30	ROW H	Utility	H30	GND	GND
31	ROW H	Overlay	H31	VID1_D4_P	JTAG - TCK
32	ROW H	Overlay	H32	VID1_D4_N	JTAG - TDI
33	ROW H	Overlay	H33	GND	GND
34	ROW H	Overlay	H34	GND	GND
35	ROW H	Overlay	H35	VID1_D5_P	AFE_SPIA_CLK_1.8
36	ROW H	Overlay	H36	VID1_D5_N	AFE_SPIA_CS_1.8
37	ROW H	Overlay	H37	GND	GND
38	ROW H	Overlay	H38	GND	GND

39	ROW H	Overlay	H39	USB2_VBUS	AFE_SPIA_MOSI_1.8
40	ROW H	Overlay	H40	RFU	AFE_SPIA_MISO_1.8

Operating Environment

Maximum Ratings

Parameter	Description/Comments	Min	Max	Units
Vin	12V Supply Input	11	13	Vdc
Pd	Max Power Dissipation		TBC	W
JESD204C Lane Rate	Max Lane Rate		17.4	Gbps
Storage Temp		-40	+105C	°C
Operating Temp	Measured at wedge lock	-10	+50	°C
Mass			388 (TBC)	grams

Radiation Performance

Parameter	Description/Comments	Limit	Units
Unshielded TID		30 (TBC)	krads (Si)
nd-SEL Immunity		37 (TBC)	MeV-cm ² /mg

Reliability & Quality

Parameter	Description/Comments	Limit	Units
MTBF	@Ta = 30 °C	2,612,040	hours
Reliability (R) @ 30°C / 100% Active	5 Years 7 Years 12 Years	0.983 0.977 0.961	

Acceptance Testing (FM3 Class C and FM4 Class D)

Temp Cycling	-10°C to +50°C (per SMC-S-016 – 6.3.8)	4	Cycles
Random Vibration (Unbiased)	3-axis / 1 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	7.1	GRMS
Electrical Testing	Functional and Performance	Pass/Fail	

Qualification Testing

Thermal Vacuum	-20°C to +60°C (per SMC-S-016 – 6.3.9)	10	Cycles
Random Vibration (Unbiased)	3-axis / 2 min per axis (20Hz to 2kHz) (per SMC-S-016 – 6.3.5)	14.1	GRMS
Mechanical Shock	3-axis / 1 per axis (per SMC-S-016 – 6.3.4)	MPE + 6dB	
Electrical Testing	Functional and Performance	Pass/Fail	

Functional Description

The AIOM-VNXP functions as a dual-channel RF data conversion and signal processing module that bridges analog RF signals and digital systems within a compact, integrated platform.

On the receive side, the module accepts RF input signals across a wide frequency range (650 MHz to 8 GHz, spanning UHF through X-Band). These signals are directly sampled by high-speed analog-to-digital converters (ADCs), translating them into digital baseband data.

On the transmit side, the module performs the inverse operation. It takes digital baseband data and converts it into RF signals using high-speed digital-to-analog converters (DACs). These RF outputs can be tuned across the same wide frequency range, supporting flexible waveform generation for a variety of mission profiles.

At the core of the module is the Texas Instruments AFE7950 RF sampling transceiver, which provides dual ADC and DAC channels along with an additional observation channel used for feedback, calibration, or linearization tasks. The module supports up to 1200 MHz of instantaneous bandwidth, enabling high-throughput, wideband operation. High-speed JESD204C interfaces facilitate data transfer between the converter and external processing elements such as VE2302, while integrated frequency synthesis eliminates the need for many external RF components.

Functionally, the AIOM-VNXP consolidates multiple RF front-end operations—including sampling, frequency conversion, and channelization—into a single mixed-signal device. This integration reduces reliance on discrete RF hardware, simplifies system architecture, and shifts much of the signal processing into software-defined domains. As a result, the module enables reconfigurable and scalable RF systems that can be adapted to different frequency bands, waveforms, and mission requirements without significant hardware redesign.

Packaged in a VNX+ form factor and designed for controlled, radiation-tolerant environments, the module delivers high performance while maintaining efficient size, weight, and power. It serves as a flexible RF front end for satellite payloads and advanced communication systems, supporting multi-band, multi-mission operation with reduced complexity and faster deployment timelines.

Mechanical Drawing

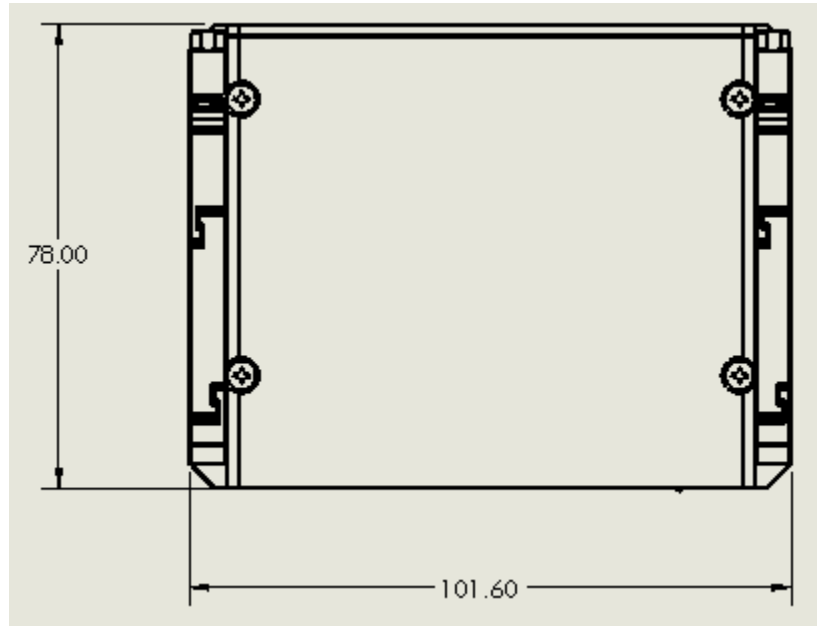


Figure 4. AIOM-VNXP Top View

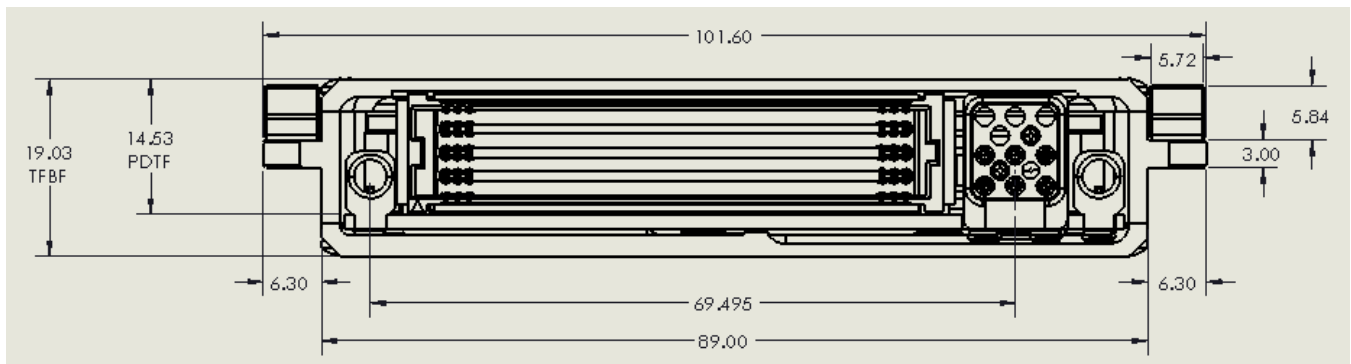


Figure 5. AIOM-VNXP Rear View

Revision History

Date	Revision #	Author	Change Description	Page #
5/15/2026	1.0	DPA	Initial release of Preliminary Datasheet.	All

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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