FRONTGRADE

DATASHEET

UT8SD4MQ2G72

18GB DDR4 SDRAM

12/4/2025
Version: 1.0.0

Features

- 18 Gbytes organized as 2G x 72-bits (16GB+2GB ECC)
- PC4-19200 UDIMM equivalent
- 9 die x 2G x 8 configuration
- Dedicated RESET each die
- Supports die SEFI recovery and maintain module availability
- Command/Address (CA) parity
- Up to 2400 MT/s data rate
- Maximum Power Savings Mode supported
- Low power auto self refresh
- Thermally enhanced packaging technology
- 266-pin PBGA Package
  — 15mm x 20mm x 1.92mm, 1.17gm
  — 1.0mm pitch
- 1.2V VDD & VDDQ
- 2.5VPP
- Power: 220mW burst READ/WRITE power per die
  — est. Theta JC < 5 °C/W
- MSL 3

Operational Environment

- Target Temperature Range: -55°C to +125°C
- TID: 50 krad(Si) using 3.9 µs refresh rate
- SEL Event Rate: 6E-08 Events/device▪day. (GEO) (See table 23 for more details)

Applications

- High-performance computing
- Processing data storage for AI and ML
- RF signal processing data storage
- Buffering data for SSDs

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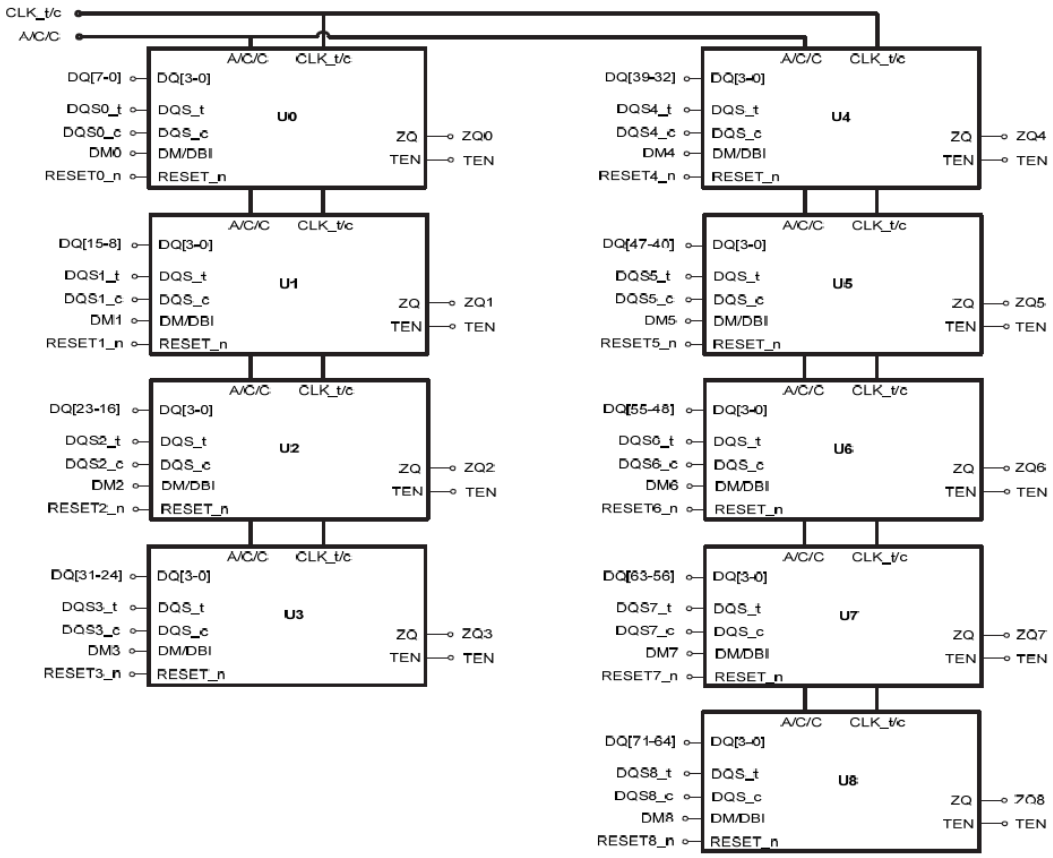

Figure 1: DDR4 DRAM Block Diagram

Functional Overview/System Summary

Features

For space applications demanding ultra-high memory density and throughput with exceptional space grade assurances, FRONTGRADE offers the industry leading 18Gbyte DDR4 DRAM memory module. The 18GB DDR4 provides a 2G addressing depth with a 64-bit data plus 8-bit ECC bus width capable of 2400 MT/s data throughput.

The radiation tolerant UT8SD4MQ2G72 is an ultra-high-density multi-chip module providing 18GB single-rank ECC UDIMM capability in a small 20mm x 15mm footprint. The solution allows for a module level bus width supporting 64-data bits plus 8-ECC check bits, which supports Single Error Correction and Double Error Detection (SECDED) ECC protection. To further enable SEFI recovery techniques, the UT8SD4MQ2G72 provides dedicated RESET for each die thus allowing the system controller to reset/recover SEFI die while holding the remaining die in a self-refreshing stand-by mode. For applications requiring strong EDAC and SEFI protection, the module can be used in a 48-bit data bus plus 24-bit Reed-Solomon EDAC configuration.

With the x72 module configuration, the UT8SD4MQ2G72 is optimally suited to interface with many of the dedicated DDR4 controller facilities available on leading space grade FPGAs and advanced processors like the FRONTGRADE GR765.

DDR4 Design Guidelines

Item	Description	Implementation Suggestion
JEDEC	JEDEC Standards	Follow guidelines per JEDEC Standards and Host Memory Interface requirements
Placement	DDR4 Interface between MCP & Host/Memory Controller	The MCP (Multi-chip package) should be placed as close as possible to the processor/memory controller, with direct / straight interconnect between them.
Rtt Termination	Termination for DDR4 address/command/control signals	Incorporated in MCP - not required externally
Differential Clock Termination	Clock Termination for DDR differential clock input signal	Incorporated in MCP - not required externally
RESET_n	Reset Signal	Requires external pull-up
Decoupling	High Speed Decoupling	Incorporated in MCP - not required externally
Bulk Decoupling	Low speed/low frequency	Needed for low frequency core current to provide bulk decoupling externally close to the MCP for VDD rail, typically 0.1µF & 1µF - approx 5 parts of each value
Plane	Power	Must incorporate Power Plane for good and effective power distribution
Plane	Ground	Must incorporate Ground Plane for good return path
Thermal	Ensure Tcase of device remains at or below 100C under expected operating conditions.	Customer should perform thermal simulation of device in application to determine appropriate thermal mitigation techniques required to ensure device case temperature maximum is not exceeded. Typical thermal mitigation techniques that may be required include heat sinks and/or PCB design enhancements such as thermal vias, heavier power and ground planes, etc.
Trace impedance	Impedance	Follow DDR4 impedance guidelines per signal group.
Trace Spacing	Crosstalk	Traces shall be spaced such that crosstalk in minimized
Trace Lengths	Data Byte Lanes	Trace lengths for each Byte Lane shall be tuned to be within 1%
Trace Lengths	Address & Command	Trace lengths for all Address and Control signals shall be tuned to be within 5%
Calibration	Zq resistor for drive strength calibration	FG recommends adding an external ZQ resistor population option to the motherboard layout (Zq=240 ohm +/- 1%).

Pin List

Table 1: Pin List

Pin Name	Direction	Description	Location
A<16:0>	IN	Address inputs	K1, K2, K4, K8, K10, L1, L3, L4, L6, L9, M2, M3, M4, M5, M6, M8, M10
ACT_n	IN	Command input: ACT_n indicates an ACTIVATE command	K9
Alert_n	OUT	Alert output	K3
BAx	IN	Bank address input	K6, M7

Pin Name	Direction	Description	Location
BGx	IN	Bank group address input	K7, M9
CBx	IN/OUT	DIMM ECC check bits	G11, H10, H11, H13, J6, J8, J10, J13
CK_c	IN	Register clocks input (negative line of differential pair)	L11
CK_t	IN	Register clock input (positive line of differential pair)	L12
CKE0	IN	Clock enable	N11
CS0_n	IN	Chip Select	J11
DMx	IN/OUT	Input Data Mask and Data Bus Inversion	C13, D8, F8, G13, H12, N13, T9, T13, U8
DQ<63:0>	IN/OUT	Data input/output	A6, A8, A10, A12, A13, B4, B6, B8, B10, B12, C6, C8, C10, C11, C12, D6, D10, E6, E10, E12, E13, F4, F6, F10, F12, G4, G6, G8, G10, G12, H4, H8, N3, N6, N8, N10, N12, P4, P6, P7, P8, P10, P12, R4, R6, R8, R9, R12, T6, T12, U6, U10, U11, U12, V4, V6, V8, V10, V12, W4, W8, W10, W12, W13
DQSx_t	IN/OUT	Data strobes, positive line	B9, C14, E14, F9, H14, R10, R14, U14, V9
DQSx_c	IN/OUT	Data strobes, negative line	B14, C9, E9, F14, J14, P14, T10, U9, V14
ODT0	IN	Register on-die termination control lines input	L10
PARITY	IN	Parity for command and address	M1
RESETn	IN	Device reset, individual die	C1, D1, E1, E2, G2, P2, R1, T1, U1
TEN	IN	Boundary Scan Mode Enable	K5
ZQx	PWR	Reference Ball for ZQ calibration	C7, D7, E7, F7, G7, R7, T7, U7, V7
VDD	PWR	Core and I/O power supply	A3, A4, B2, B13, D5, D12, E11, F2, F5, F13, G1, J1, J2, J4, J7, J9, K12, L2, L5, L8, L13, M11, M13, N1, N2, N4, N9, P5, P13, R11, T5, V3, V13, W2, W6
VSS	GND	Ground	A2, A5, A7, A9, A11, A14, B1, B3, B5, B7, B11, C3, C5, D3, D9, D11, D13, E3, E5, E8, F3, F11, G3, G5, G9, G14, H1, H3, H5, H6, H7, H9, J3, J5, J12, K11, K13, M12, N5, N7, N14, P3, P9, P11, R3, R5, R13, T3, T8, T11, U3, U5, U13, V1, V2, V5, V11, W3, W5, W7, W9, W11, W14
VTT	PWR	Power supply for termination of address, command, and control VDD/2	F1, K14, L14, M14, P1
VPP	PWR	DRAM activating power supply	A1, D14, T14, W1
Vrefca	PWR	Reference voltage for CA	L7
NC		No Connection	C2, C4, D2, D4, E4, H2, R2, T2, T4, U2, U4

Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VPP	GND	VDD	VDD	GND	DQ30	GND	DQ25	GND	DQ22	GND	DQ19	DQ17	GND	A
B	GND	VDD	GND	DQ28	GND	DQ29	GND	DQ27	DQS3_t	DQ20	GND	DQ16	VDD	DQS2_c	B
C	Reset0_n	NC	GND	NC	GND	DQ31	ZQ2	DQ26	DQS3_c	DQ23	DQ21	DQ18	DM2_n/DBI2	DQS2_t	C
D	Reset1_n	NC	GND	NC	VDD	DQ24	ZQ3	DM3_n/DBI3	GND	DQ15	GND	VDD	GND	VPP	D
E	Reset2_n	Reset3_n	GND	NC	GND	DQ3	ZQ1	GND	DQS0_c	DQ12	VDD	DQ10	DQ9	DQS1_t	E
F	VTT	VDD	GND	DQ7	VDD	DQ2	ZQ0	DM0_n/DBI0	DQS0_t	DQ13	GND	DQ8	VDD	DQS1_c	F
G	VDD	Reset8_n	GND	DQ4	GND	DQ5	ZQ8	DQ1	GND	DQ14	CB5	DQ11	DM1_n/DBI1	GND	G
H	GND	NC/A17	GND	DQ6	GND	GND	GND	DQ0	GND	CB7	CB2	DM8_n/DBI8	CB1	DQS8_t	H
J	VDD	VDD	GND	VDD	GND	CB6	VDD	CB3	VDD	CB4	CS0_n	GND	CB0	DQS8_c	J
K	A13	A9	ALERT_n	A6	TEN	BA1	BG0	A12/BC_n	ACT_n	A14/WE_n	GND	VDD	GND	VTT	K
L	A11	VDD	A7	A1	VDD	A4	VREFCA	VDD	A16/RAS_n	ODT0	CK_c	CK_t	VDD	VTT	L
M	PARITY	A2	A8	A0	A5	A3	BA0	A10/AP	BG1	A15/CAS_n	VDD	GND	VDD	VTT	M
N	VDD	VDD	DQ62	VDD	GND	DQ61	GND	DQ57	VDD	DQ54	CKE0	DQ51	DM6_n/DBI6	GND	N
P	VTT	Reset4_n	GND	DQ60	VDD	DQ58	DQ59	DQ52	GND	DQ55	GND	DQ48	VDD	DQS6_c	P
R	Reset5_n	NC	GND	DQ63	GND	DQ56	ZQ6	DQ34	DQ53	DQS7_t	VDD	DQ50	GND	DQS6_t	R
T	Reset6_n	NC	GND	NC	VDD	DQ39	ZQ7	GND	DM7_n/DBI7	DQS7_c	GND	DQ49	DM5_n/DBI5	VPP	T
U	Reset7_n	NC	GND	NC	GND	DQ32	ZQ5	DM4_n/DBI4	DQS4_c	DQ47	DQ45	DQ42	GND	DQS5_t	U
V	GND	GND	VDD	DQ38	GND	DQ37	ZQ4	DQ33	DQS4_t	DQ46	GND	DQ40	VDD	DQS5_c	V
W	VPP	VDD	GND	DQ36	GND	VDD	GND	DQ35	GND	DQ44	GND	DQ43	DQ41	GND	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2: Ball Assignments

Pin Descriptions

Table 2: Pin Descriptions

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0	Input	Clock Enable: CKE0 HIGH activates, and CKE0 Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE0 Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE0 is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE0, are disabled during power-down. Input buffers, excluding CKE0, are disabled during Self-Refresh.
CS0_n	Input	Chip Select: All commands are masked when CS0_n is registered HIGH. CS0_n provides for external Rank selection on systems with multiple Ranks. CS0_n is considered part of the command code.
ODT0	Input	On Die Termination: ODT0 (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT0 is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n, NU. For x16 configuration ODT0 is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT0 ball will be ignored if MR1 is programmed to disable RTT_NOM.

Symbol	Type	Function
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS0_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS0_n) define the command being entered. Those balls have multi-function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command balls for Read, Write and other command defined in command truth table.
DM_n/DBI_n, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0-BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0-BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0-A13, A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
PARITY	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACR_n, RAS_N/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12, A12/BC_n,BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE and ODT. Unused address pins that are density-and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RESET[8-0]_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
DQ<63:30>	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0 to DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
CB<7:0>	Input/ Output	Check Bit Input/ Output: Bi-directional ECC portion of data bus for x72 configurations
DQS_t, DQS_c,	Input/	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in

Symbol	Type	Function
DQSU_t, DQSU_c, DQSL_t, DQSL_c	Output	write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete.
TEN	Input	Boundary Scan Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this ball will enable boundary scan operation along with other balls. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
NC		No Connect: No internal electrical connection is present. Do not connect to these signals.
V_{DD}	Supply	Power Supply: 1.2 V +/- 0.06 V
GND	Supply	Ground
V_{TT}	Supply	Power Supply: 0.6 V +/- 3%
V_{PP}	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Ball for ZQ calibration

Notes:

1. No external termination required on input only balls (BG0-BG-1, BA0-BA1, A0-A17, ACT_n, RAS_n,/A16, CAS_n/A15, WE_n/A14, PARITY, CS_n, CKE, ODT).

Table 3: Truth Table

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA[1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
MODE REGISTER SET		MRS	H	H	L	H	L	L	L	BG	BA	V	OP code				7
REFRESH		REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	8, 9, 10
Self refresh exit		SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	8, 9, 10, 11
					L	H	H	H	H	V	V	V	V	V	V	V	
Single-bank PRECHARGE		PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
Reserved for future use		RFU	H	H	L	H	L	H	H	RFU							
Bank ACTIVATE		ACT	H	H	L	L	Row Addr (RA)			BG	BA	V	Row Addr (RA)				
WRITE	BL8 fixed, BC4 fixed	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
	BC4OTF	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
	BL8OTF	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
WRITE with auto	BL8 fixed, BC4 fixed	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
	BC4OTF	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA[1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
precharge	BL8OTF	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
READ	BL8 fixed, BC4 fixed	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
	BC4OTF	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
	BL8OTF	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
"READ with auto precharge"	BL8 fixed, BC4 fixed	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
	BC4OTF	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
	BL8OTF	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
NO OPERATION		NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	12
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	13
Power-down entry		PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
Power-down exit		PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	H	L	X	X	X	X	X	H	X	
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	H	L	X	X	X	X	X	L	X	

Notes:

1. • BG = Bank group address
   • BA = Bank address
   • RA = Row address
   • CA = Column address
   • BC_n = Burst chop
   • X = “Don’t Care”
   • V = Valid
2. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT_n = H, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n, respectively. When ACT_n = L, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14, respectively.
3. RESET_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
4. Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
5. V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
6. READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
7. During an MRS command, A17 is RFU and is device density- and configuration-dependent.
8. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
9. VPP and VREF (VREFCA) must be maintained during SELF REFRESH operation.
10. Refer to the Truth Table – CKE table for more details about CKE transition.
11. Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
12. The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.
13. The NOP command may not be used in place of the DESELECT command.
14. The power-down mode does not perform any REFRESH operation.

DDR4 Mode Registers

Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MRn) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The MRS command cycle time, tMRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the tMRD Timing figure. Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply tMRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- Maximum power saving mode
- CS to command/address latency
- CA parity latency mode
- VREFDQ training value
- VREFDQ training mode
- VREFDQ training range

Some mode register settings may not be supported because they are not required by certain speed bins.

tMRD Timing Diagram

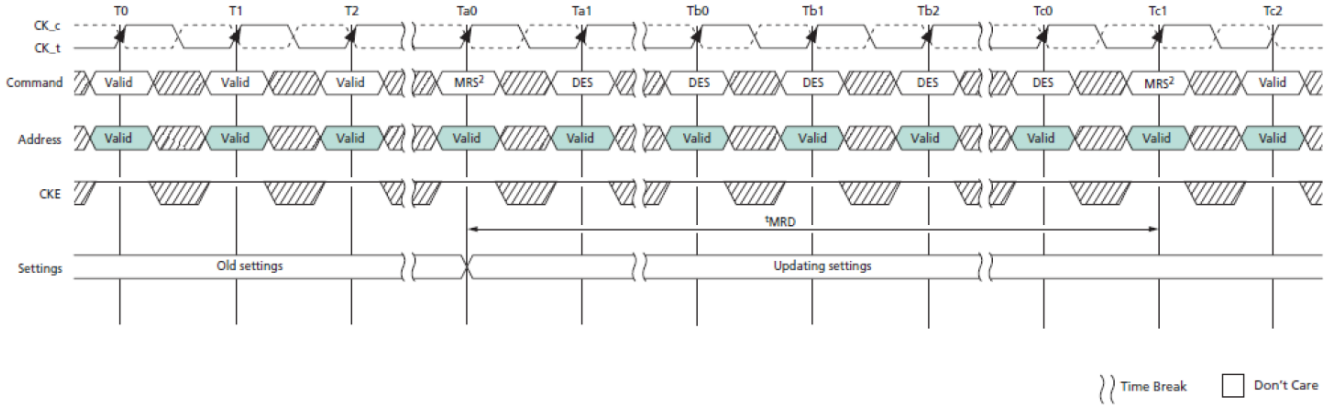

Figure 3: tMRD Timing

Notes:

1. This timing diagram depicts CA parity mode "disabled" case.

2. tMRD applies to all MRS commands with the following exceptions:
   - Gear-down mode
   - CA parity mode
   - CAL mode
   - Per-DRAM addressability mode
   - V_{REFDQ} training value, V_{REFDQ} training mode, and V_{REFDQ} training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET. tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the tMOD Timing figure.

tMOD Timing Diagram

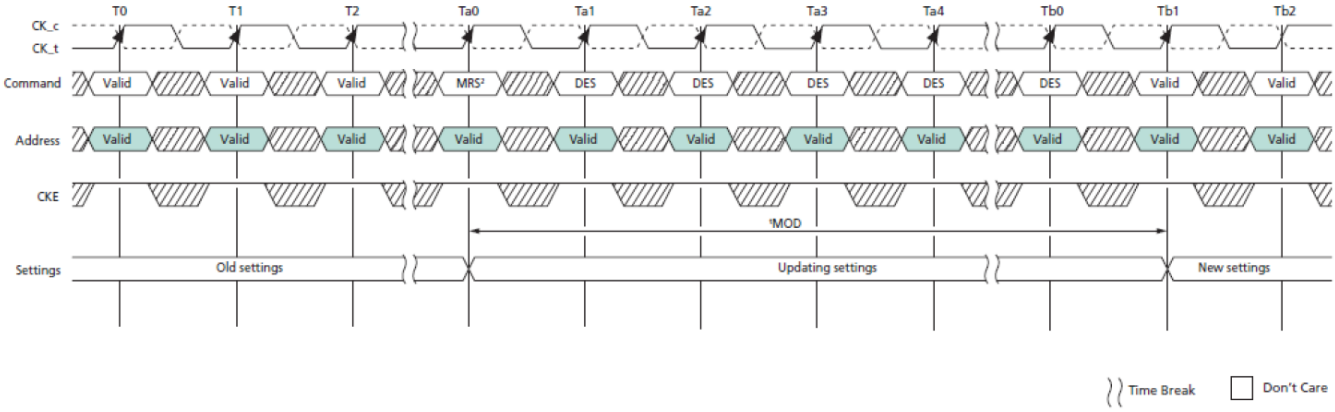

Figure 4: tMOD Timing

Notes:

1. This timing diagram depicts CA parity mode "disabled" case.
2. tMOD applies to all MRS commands with the following exceptions:
   - DLL enable, Gear-down mode
   - VREFDQ training value, internal VREF training monitor, VREFDQ training mode, and VREFDQ training range
   - Maximum power saving mode, Per-DRAM addressability mode, and CA parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the RTT(NOM) feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered HIGH after tMOD has expired. If the RTT(NOM) feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes. In some mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

Mode Register 0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 4: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 5: MR0 Register Definition

Mode Register 0	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13, 11:9	**WR (WRITE recovery)/RTP (READ-to-PRECHARGE)** 0000 = 10 / 5 clocks1 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks1 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks1 0101 = 20 /10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks1 1000 = 26 / 13 clocks1 1001 through 1111 = Reserved
8	**DLL reset** 0 = No 1 = Yes
7	**Test mode (TM)** – Manufacturer use only 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	**CAS latency (CL)** – Delay in clock cycles from the internal READ command to first data-out 00000 = 9 clocks /1 00001 = 10 clocks

Mode Register 0	Description
	00010 = 11 clocks /1 00011 = 12 clocks 00100 = 13 clocks /1 00101 = 14 clocks 00110 = 15 clocks /1 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks /1 01101 = 17 clocks /1 01110 = 19 clocks /1 01111 = 21 clocks /1 10000 = 25 clocks (3DS use only) 10001 = 26 clocks 10010 = 27 clocks (3DS use only) 10011 = 28 clocks 10100 = 29 clocks /1 10101 = 30 clocks 10110 = 31 clocks /1 10111 = 32 clocks
3	**Burst type (BT)** – Data burst ordering within a READ or WRITE burst access 0 = Nibble sequential 1 = Interleave
1:0	**Burst length (BL)** – Data burst size associated with each read or write access 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

Notes:

1. Note allowed when 1/4 rate gear-down is enabled.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 6: Burst Type and Burst Order /1

Burst Length	Read/Write	Starting Column Address (A[2,1,0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3

Burst Length	Read/Write	Starting Column Address (A[2,1,0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7 3	3

Notes:

1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for tWR and tWTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
3. T = Output driver for data and strobes are in High-Z.
   V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
   X = “Don’t Care.”

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery (WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WR (MIN) cycles = roundup (tWR[ns]/tCK[ns]). The WR value must be programmed to be equal to or larger than tWR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data. Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer: RTP (MIN) cycles = roundup (tRTP[ns]/tCK[ns]). The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

DLL Reset

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, tDLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example,).

Mode Register 1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 7: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 8: MR1 Register Definition

Mode Register 1	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6

Mode Register 1	Description
	111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) 1 = Disabled (both ODI and RTT)
11	Not Used
10, 9 ,8	**Nominal ODT (RTT(NOM) – Data bus termination setting (Zq=240 ohm)** 000 = RTT(NOM) disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
7	**Write leveling (WL) – Write leveling mode** 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
6, 5	**RFU** 0 = Must be programmed to 0 1 = Reserved
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 11 10 = CL - 2 11 = Reserved
2, 1	**Output driver impedance (ODI) – Output driver impedance setting (Zq=240 ohm)** 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAON, or tAOF parameters. During tDLLK, CKE

must continuously be registered H IGH. The device does not require DLL for any WRITE operation, except when RTT(WR) is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode. The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set RTT(WR), MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT $R_{TT(NOM)}$ Values

The device is capable of providing three different termination values: RTT(Static), RTT(NOM), and RTT(WR). The nominal termination value, RTT(NOM), is programmed in MR1. A separate value, RTT(WR), may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITE operations. The RTT(WR) value can be applied during WRITE commands even when RTT(NOM) is disabled. A third RTT value, RTT(Static), is programmed in MR5. RTT(Static) provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 9: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note:

1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Driver Impedance Control

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading

of the output drivers. For example, this feature may be useful when measuring MCP power. For normal operation, set MR1[12] to 0.

Mode Register 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 10: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 11: MR2 Register Definition

Mode Register 2	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**TRR mode** 0 = Disabled 1 = Enabled
12	**WRITE data bus CRC** 0 = Disabled 1 = Enabled
11:9	**Dynamic ODT (RTT(WR)) – Data bus termination setting during WRITEs (Zq=240 ohm)** 000 = RTT(WR) disabled (WRITE does not affect RTT value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm)

Mode Register 2	Description
	100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (TC: 0°C–85°C) 01 = Manual mode - Reduced operating temperature range (TC: 0°C–45°C) 10 = Manual mode - Extended operating temperature range (TC: 0°C–95°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL)** – Delay in clock cycles from the internal WRITE command to first data-in 1tCK WRITE preamble 000 = 9 (DDR4-1600) /1 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600) /1 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2tCK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	**TRR mode - BGn control** 00 = BG0 01 = BG1 10 = BG2 11 = BG3
1:0	**TRR mode - BAn control** 00 = BA0 01 = BA1 10 = BA2 11 = BA3

Note:

1. Not allowed when 1/4 rate gear-down mode is enabled.

CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT (RTT(WR)) settings in MR2[11:9]. In write leveling mode, only RTT(NOM) is available.

Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

Target Row Refresh Mode

For the device, rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (tMAW) before the adjacent rows need to be refreshed regardless of how the activates are distributed over tMAW. The row receiving the excessive activates is the target row (TRn); the two adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TRn, either the device must receive (roundup of tMAW / tREFI) REFRESH commands (REF) before another row activate is issued, or it needs to be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered the MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the activates from two target rows on a victim row should not exceed the MAC value as well. When the temperature controlled refresh (TCR) mode is enabled, tMAW should be adjusted depending on the TCR range as shown in the following table. Using TRR mode is not required, and in some cases has been rendered inoperable, as the device automatically performs TRR Mode in the background.

Mode Register 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 12: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 13: MR3 Register Definition

Mode Register 3	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:11	**Multipurpose register (MPR) – Read format** 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	**WRITE CMD latency when CRC/DM enabled** 00 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400) 10 = 6CK (DDR4-2666/2933/3200) Not Supported 11 = Reserved
8:6	**Fine granularity refresh mode** 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	**Temperature sensor status** 0 = Disabled 1 = Enabled
4	**Per-DRAM addressability** 0 = Normal operation (disabled) 1 = Enable
3	**Gear-down mode – Ratio of internal clock to external data rate** 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	**Multipurpose register (MPR) access** 0 = Normal operation

Mode Register 3	Description
	1 = Data flow from MPR
1:0	**MPR page select** 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MRn registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

Mode Register 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 14: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 15: MR4 Register Definition

Mode Register 4	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**Post Package Repair (PPR mode)** 0 = Disabled 1 = Enabled
12	**WRITE preamble setting** 0 = 1tCK toggle /1 0 = 2tCK toggle
11	**READ preamble setting** 0 = 1tCK toggle1 1 = 2tCK toggle (When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.)
10	**READ preamble training** 0 = Disabled 1 = Enabled

Mode Register 4	Description
9	**Self refresh abort mode** 0 = Disabled 1 = Enabled
8:6	**CMD (CAL) address latency** 000 = 0 clocks (disabled) 001 =3 clocks1 010 = 4 clocks 011 = 5 clocks1 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	**soft Post Package Repair (sPPR mode)** 0 = Disabled 1 = Enabled
4	**Internal VREF monitor** 0 = Disabled 1 = Enabled
3	**Temperature controlled refresh mode** 0 = Disabled 1 = Enabled
2	**Temperature controlled refresh range** 0 = Normal temperature mode 1 = Extended temperature mode
1	**Maximum power savings mode** 0 = Normal operation 1 = Enabled
0	**RFU** 0 = Must be programmed to 0 1 = Reserved

Note:

1. Not allowed when 1/4 rate gear-down mode is enabled.

Post Package Repair Mode

The post package repair (PPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether PPR mode is available (A7 = 1) or not available (A7 = 0). PPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is irrevocable so great care should be exercised when using.

Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is revocable by either doing a reset or power-down.

WRITE Preamble

Programmable WRITE preamble, tWPRE, can be set to 1tCK or 2tCK via the MR4 register. The 1tCK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

READ Preamble

Programmable READ preamble tRPRE can be set to 1tCK or 2tCK via the MR4 register. Both the 1tCK and 2tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble Training

Programmable READ preamble training can be set to 1tCK or 2tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCK(ns)/tCAL(ns)].

Internal VREF Monitor

The device generates its own internal VREFDQ. This mode may be enabled during VREFDQ training, and when enabled, VREF,time-short and VREF,time-long need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

Mode Register 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 16: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 17: MR5 Register Definition

Mode Register 5	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled 1 = Enabled
10	**Data mask (DM)** 0 = Disabled 1 = Enabled
9	**CA parity persistent error mode** 0 = Disabled 1 = Enabled
8:6	**Parked ODT value (RTT(Park)) (Zq=240 ohm)** 000 = RTT(Park) disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm)

Mode Register 5	Description
	100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	**ODT input buffer for power-down** 0 = Buffer enabled 1 = Buffer disabled
4	**CA parity error status** 0 = Clear 1 = Error
3	**CRC error status** 0 = Clear 1 = Error
2:0	**CA parity latency mode** 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400) /1 011 = 6 clocks (DDR4-2666) 100 = 8 clocks (DDR4-2933/3200) 101 = Reserved 110 = Reserved 111 = Reserved

Note:

1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12. DBI is not allowed during MPR READ operations.

Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled.

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during powerdown), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide RTT(NOM)

termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16 , CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

Mode Register 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 18: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

- RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 19: MR6 Register Definition

Mode Register 6	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4

Mode Register 6	Description
	101 = MR5 110 = MR6 111 = DNU
17	**RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:10	**tCCD_L** 000 = 4 clocks (≤1333 Mb/s) 001 = 5 clocks (>1333 Mb/s and ≤1866 Mb/s) 010 = 6 clocks (>1866 Mb/s and ≤2400 Mb/s) 011 = 7 clocks (>2400 Mb/s and ≤2666 Mb/s) Not Supported 100 = 8 clocks (>2666 Mb/s and ≤3200 Mb/s) Not Supported 101 = Reserved 110 = Reserved 111 = Reserved
9, 8	**RFU** 0 = Must be programmed to 0 1 = Reserved
7	**VREF Calibration Enable** 0 = Disable 1 = Enable
6	**VREF Calibration Range** 0 = Range 1 1 = Range 2
5:0	**VREF Calibration Value** See the VREFDQ Range and Levels (Table 19)

tCCD_L Programming

The device controller must program the correct tCCD_L value. tCCD_L will be programmed according to the value defined per operating frequency in the AC parameter table. Although JEDEC specifies the larger of 5nCK or Xns, Micron's DRAM supports the larger of 4nCK or Xns.

VREFDQ Calibration Enable

VREFDQ calibration is where the device internally generates its own VREFDQ to be used by the DQ input receivers. The VREFDQ value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal VREFDQ level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ calibration must be used whenever values are being written to the MR6[6:0] register.

VREFDQ Calibration Range

The device defines two VREFDQ calibration ranges: Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDD while Range 2 supports VREFDQ between 45% and 77% of VDD, as seen in VREFDQ Specification table. Although not a restriction, Range 1 was targeted for module based designs and Range 2 was added to target point-to-point designs.

VREFDQ Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ, as seen in VREFDQ Range and Levels table in the VREFDQ Calibration section.

DQ Internal Vref Specifications

VREFDQ Calibration and Training

The VREFDQ level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via VREFDQ calibration mode. If PDA or PPR modes are used prior to VREFDQ calibration, VREFDQ should initially be set at the midpoint between the VDD,max, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for VREFDQ calibration to determine the best internal VREFDQ level. The VREFDQ calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of VDD) or Range 2 (45% to 77.5% of VDD), and an MRS protocol using MR6[5:0] to adjust the VREFDQ level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is disabled. The DRAM controller will likely use a series of writes and reads in conjunction with VREFDQ adjustments to obtain the best VREFDQ, which in turn optimizes the data eye. The internal VREFDQ specification parameters are voltage range, step size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for DDR4 SDRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

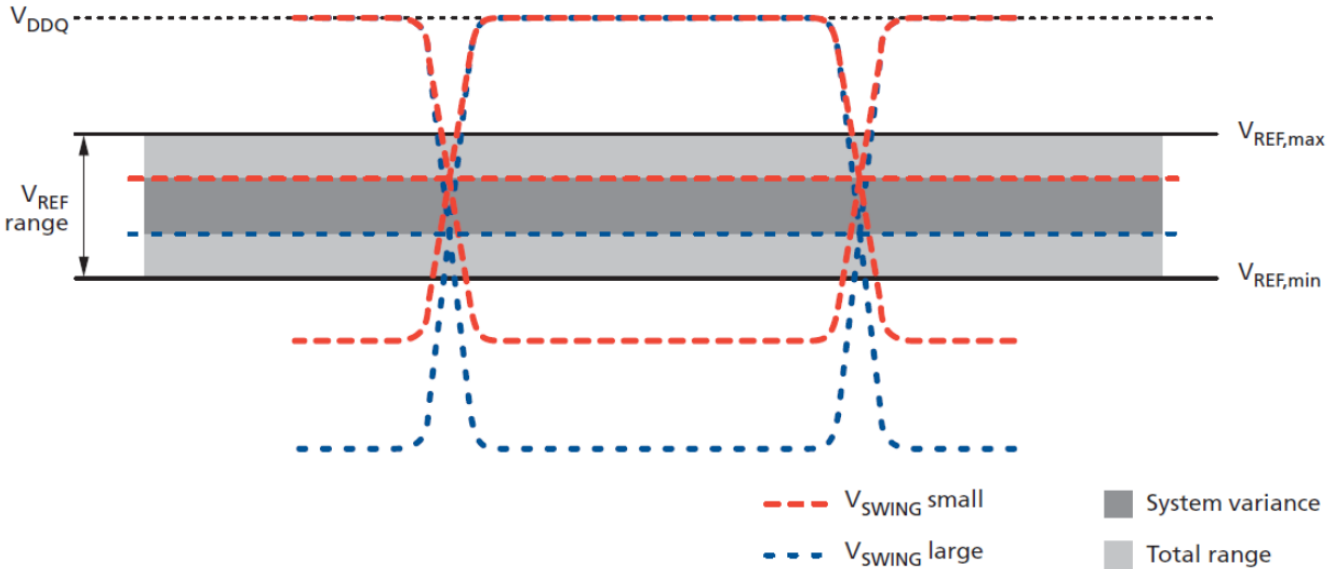

Figure 5: VREFDQ Voltage Range

Table 20: VREFDQ Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 = Reserved		

VREFDQ Step Size

The VREF step size is defined as the step size between adjacent steps. VREF step size ranges from 0.5% VDD to 0.8% VDD. However, for a given design, the device has one value for VREF step size that falls within the range. The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n. The VREF set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX VREF value

endpoints for a specified range. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

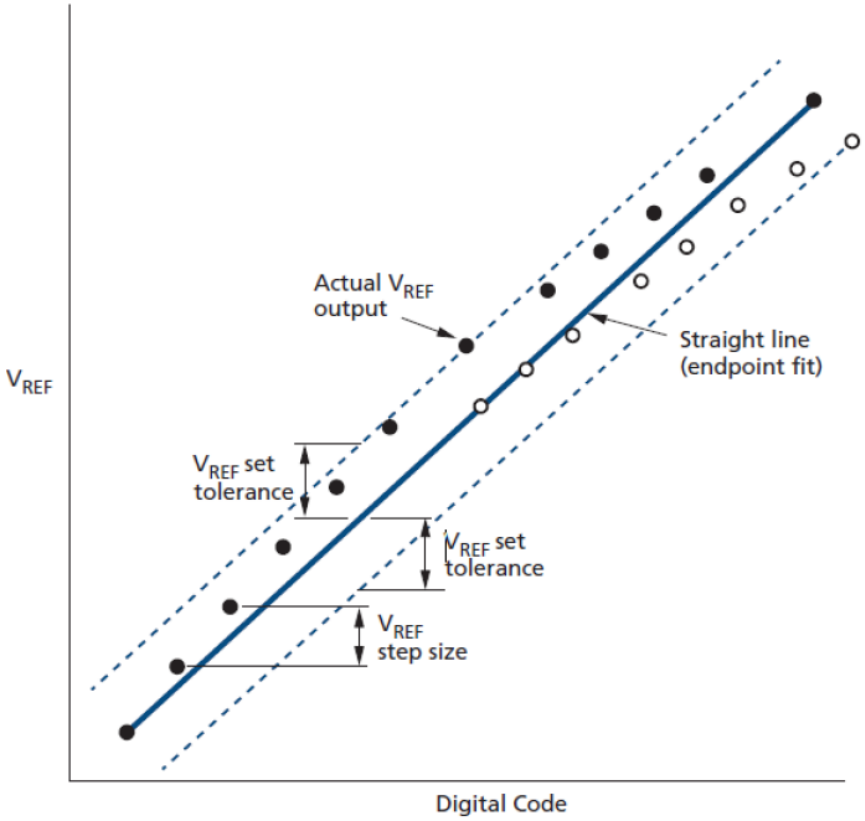

Figure 6: Example of VREF Set Tolerance and Step Size

Note: Maximum case shown.

VREFDQ Increment and Decrement Timing

The VREF increment/decrement step times are defined by VREF,time. VREF,time is defined from t0 to t1, where t1 is referenced to the VREF voltage at the final DC level within the VREF valid tolerance (VREF,val_tol). The VREF valid level is defined by VREF,val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment.

Note:
t0 is referenced to the MRS command clock
t1 is referenced to VREF, tol

VREFDQ Timing Diagram for VREF,time Parameter

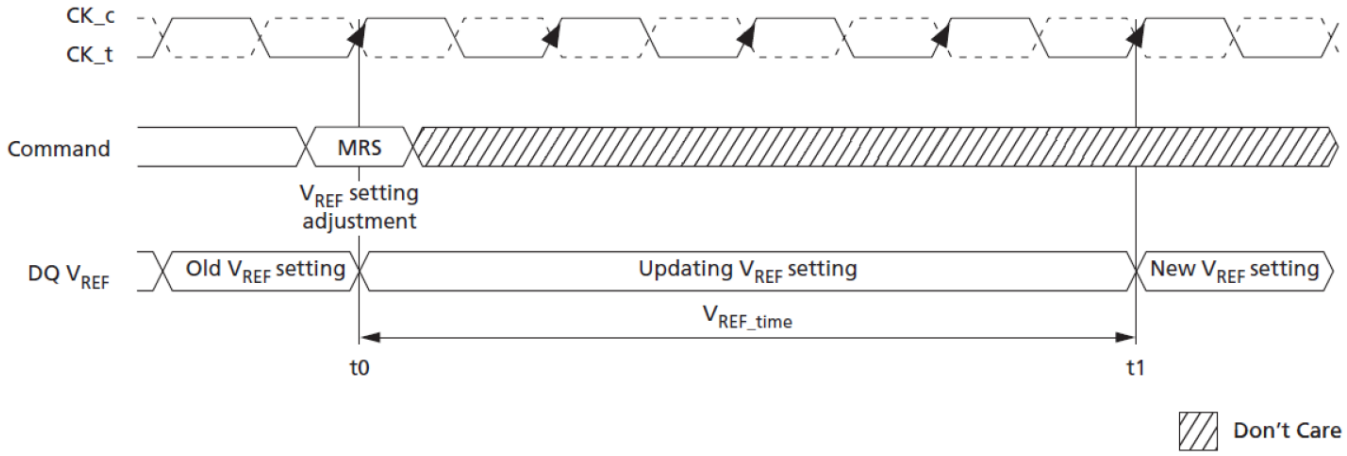

Figure 7: VREFDQ Timing Diagram for VREF,time Parameter

VREFDQ calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables VREFDQ calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After VREFDQ calibration mode has been entered, VREFDQ calibration mode legal commands may be issued once tVREFDQE has been satisfied. Legal commands for VREFDQ calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set VREFDQ values, and MRS to exit VREFDQ calibration mode. Also, after VREFDQ calibration mode has been entered, “dummy” WRITE commands are allowed prior to adjusting the VREFDQ value the first time VREFDQ calibration is performed after initialization. Setting VREFDQ values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired VREFDQ values. If MR6[7] is set to 0, MR6[6:0] are not written. VREF,time-short or VREF,time-long must be satisfied after each MR6 command to set VREFDQ value before the internal VREFDQ value is valid. If PDA mode is used in conjunction with VREFDQ calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only VREFDQ calibration mode legal commands noted above that may be used are the MRS commands: MRS to set VREFDQ values and MRS to exit VREFDQ calibration mode.

The last MR6[6:0] setting written to MR6 prior to exiting VREFDQ calibration mode is the range and value used for the internal VREFDQ setting. REFDQ calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit VREFDQ calibration mode has been issued, DES must be issued until tVREFDQX has been satisfied where any legal command may then be issued. VREFDQ setting should be updated if the die temperature changes too much from the calibration temperature. The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 1:

- MR6[7:6]10 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).
- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]10 [5:0]VVVVVV.
  - "VVVVVV" are desired settings for VREFDQ.
- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]10 [5:0]VVVVVV* where VVVVVV* = desired value for VREFDQ.
  - MR6[7]0 [6:0]XXXXXXX to exit VREFDQ calibration mode.

The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 2:

- MR6[7:6]11 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).
- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]11[5:0]VVVVVV.
  - "VVVVVV" are desired settings for VREFDQ.
- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]11 [5:0]VVVVVV* where VVVVVV* = desired value for VREFDQ.
  - MR6[7]0 [6:0]XXXXXXX to exit VREFDQ calibration mode.

Note:

Range may only be set or changed when entering VREFDQ calibration mode; changing range while in or exiting VREFDQ calibration mode is illegal.

VREFDQ Training Mode Entry and Exit Timing Diagram

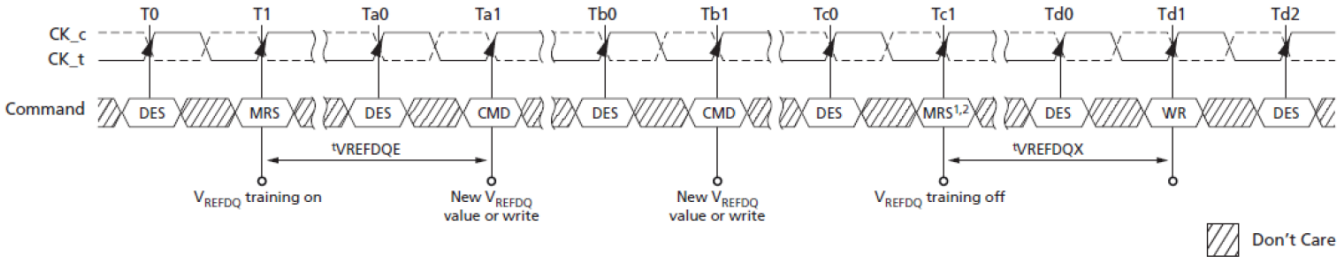

Figure 8: VREFDQ Training Mode Entry and Exit Timing Diagram

Notes:

1. New VREFDQ values are not allowed with an MRS command during calibration mode entry
2. Depending on the step size of the latest programmed VREF value, VREF must be satisfied before disabling VREFDQ training mode.

V_{REF} Step: Single Step Size Increment Case

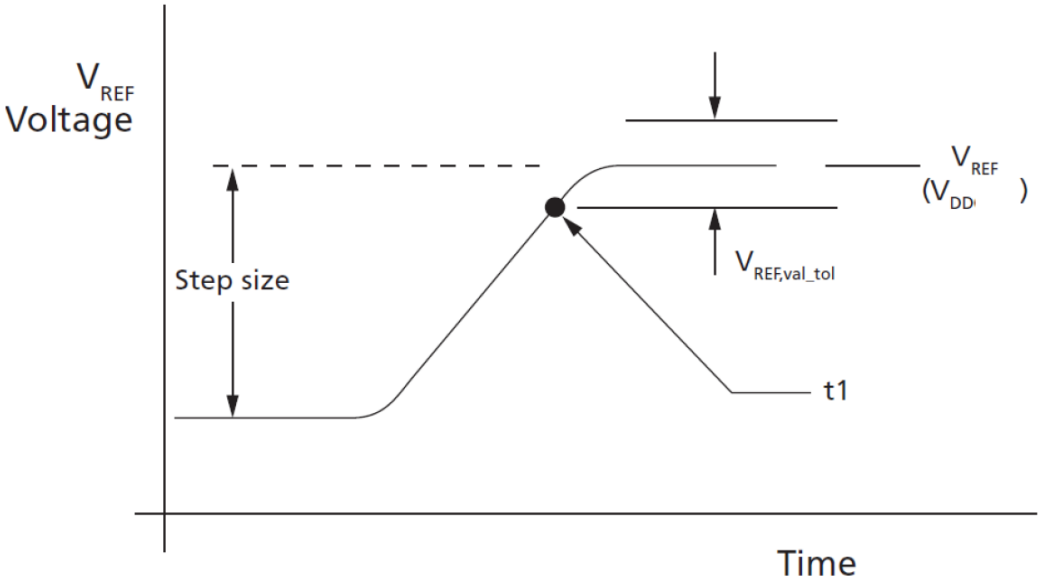

Figure 9: VREF Step: Single Step Size Increment Case

V_{REF} Step: Single Step Size Decrement Case

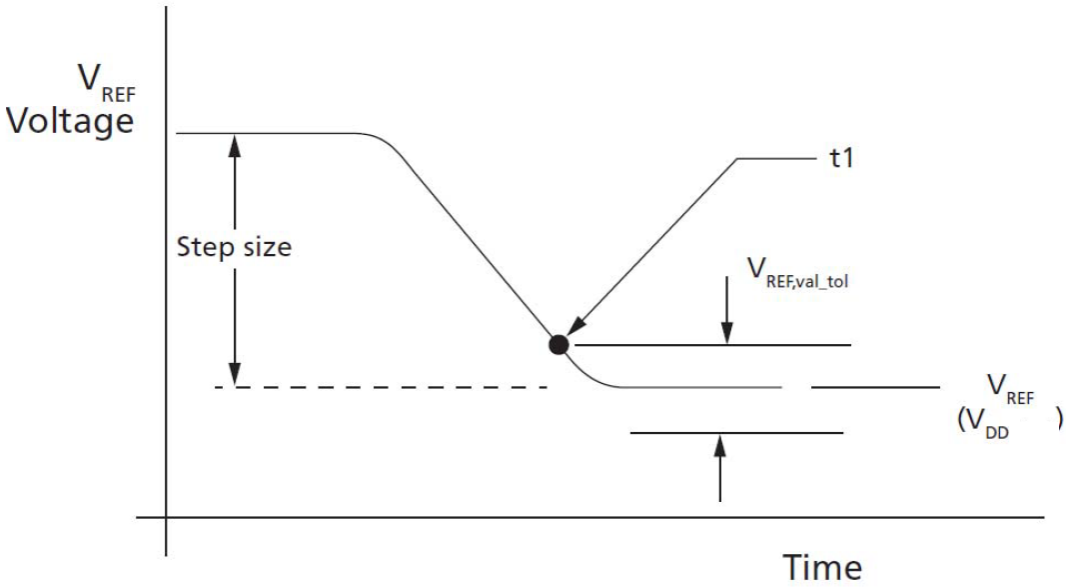

Figure 10: VREF Step: Single Step Size Decrement Case

V_{REF} Full Step: From VREF,min to VREF,maxCase

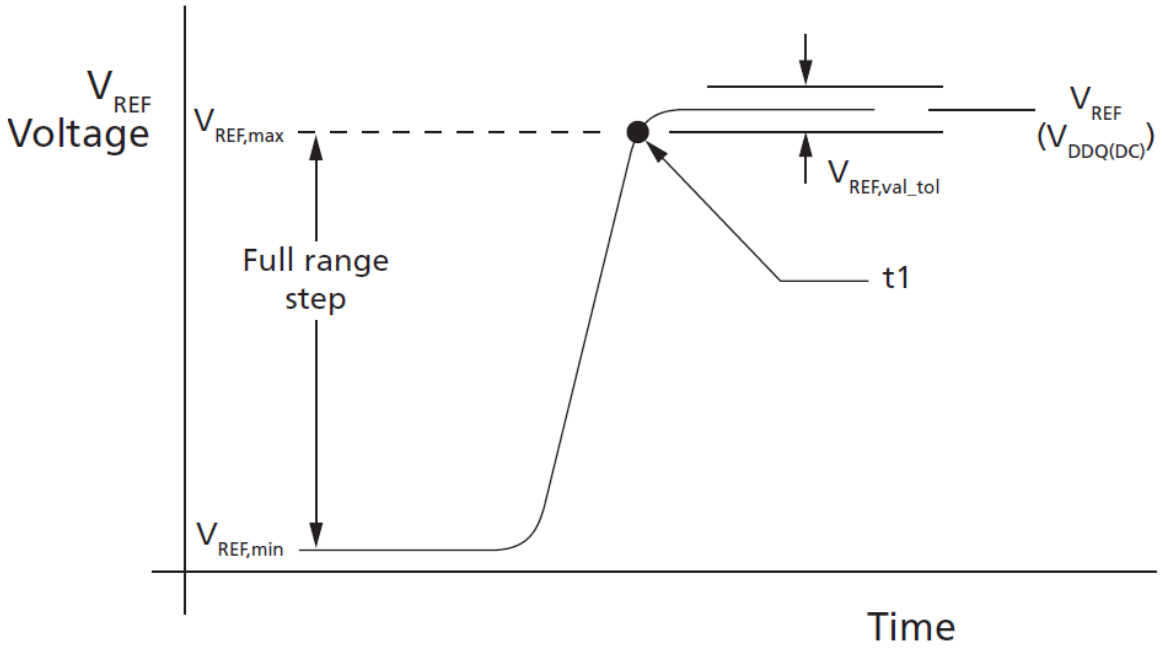

Figure 11: VREF Full Step: From VREF,min to VREF,maxCase

V_{REF} Full Step: From VREF,max to VREF,minCase

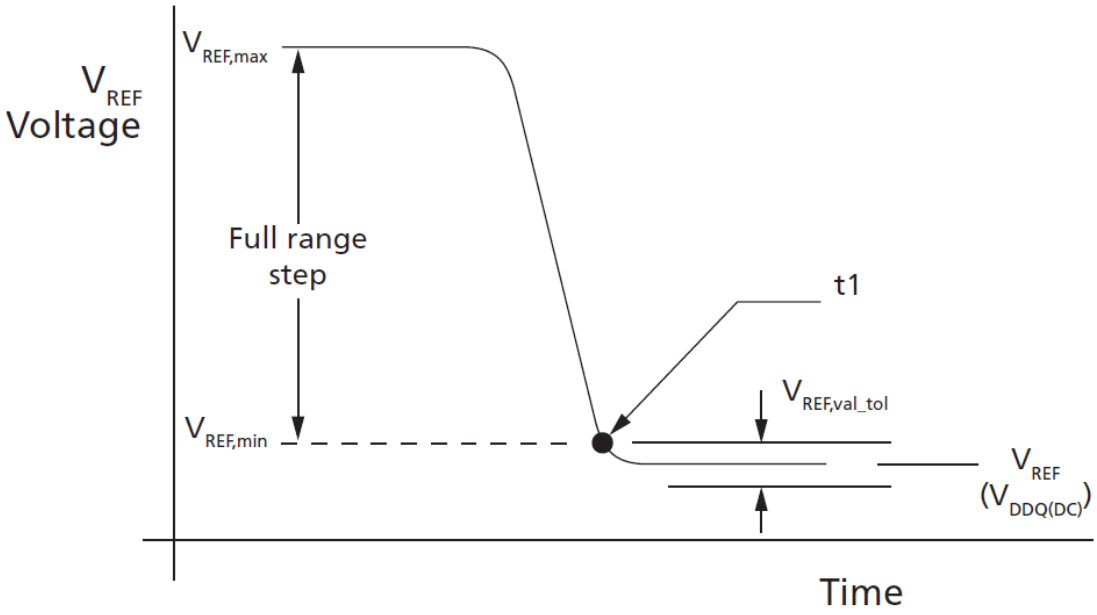

Figure 12: VREF Full Step: From VREF,max to VREF,minCase

VREFDQ Target Settings

The VREFDQ initial settings are largely dependent on the ODT termination settings. The table below shows all of the possible initial settings available for VREFDQ training; it is unlikely the lower ODT settings would be used in most cases.

Table 21: VREFDQ Settings (VDD = 1.2V)

RON	ODT	Vx – VIN LOW (mV)	VREFDQ (mv)	VREFDQ (%VDD)
34 Ohm	34 Ohm	600	900	75%
	40 Ohm	550	875	73%
	48 Ohm	500	850	71%
	60 Ohm	435	815	68%
	80 Ohm	360	780	65%
	120 Ohm	265	732	61%
	240 Ohm	150	675	56%
48 Ohm	34 Ohm	700	950	79%
	40 Ohm	655	925	77%
	48 Ohm	600	900	75%
	60 Ohm	535	865	72%
	80 Ohm	450	825	69%
	120 Ohm	345	770	64%
	240 Ohm	200	700	58%

VREFDQ Equivalent Circuit

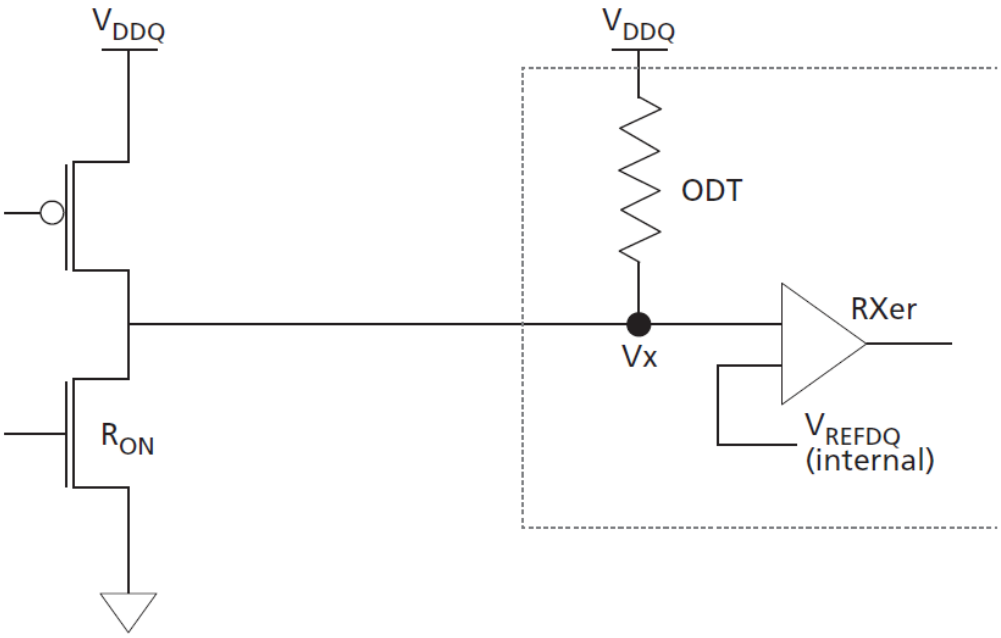

Figure 13: VREFDQ Equivalent Circuit

Absolute Maximum Ratings /1

Table 22: Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
VDD	Supply Voltage /2	-0.3	1.5	V
VPP	Supply Voltage /3	-0.3	3.0	V
PD	Max Power Dissipation /4		22.5	W
TJ	Junction Temperature		150	°C
θJC	Thermal resistance, junction-to-case		4	°C/W
θJB	Thermal resistance, junction-to-base		9	°C/W
TSTG	Storage Temperature /5	-55	150	°C
ESDHBM	ESD Protection /6		2000	V

NOTE:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. VREFCA must be not greater than 0.6 x VDD, When VDD is less than 500 mV; VREFCA may be equal to or less than 300 mV.
3. VPP must be equal or greater than VDD at all times
4. Per MIL-STD-883, method 1012.1, section 3.4.1, PD=[TJ(max)-TC(max))/θJC]. Using TC = 105°C.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, refer to JESD51- 2 standard.
6. Per MIL-STD-883, method 3015.9, Table 3.

Operational Environment

Table 23: Operational Environment

SYMBOL	PARAMETER	LIMIT	UNITS
TID	Total Ionizing Dose /1,2	50	krad(Si)
SEL	Single Event Latchup Event Rate /3	1.76E-9 (LEO) 4.91E-8 (MEO) 6.00E-8 (GEO)	Events/device▪day
SEU	Single Event Upset /4	8.93E-12	Errors/bit-day
SEFI	Single Event Functional Interrupt /5	High current –1.04E-4 dynamic – 5.87E-4	Events/device-day

NOTE:

1. For devices procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
2. Per MIL-STD-883, method 1019.9, condition A at 3.9 µs refresh rate.

3. SEL characterization is performed at VDD = 1.26 V at 105°C from LETs of 37 to 82. SEL threshold is 37 LET. Contact factory for radiation report for full test details. (Adams 90% worst case, 100mils Al)
4. SEU characterization is performed at VDD = 1.14 V at 25°C. (LEO, Adams 90% worst case, 100mils Al)
5. Dynamic SEFI characterization is performed at VDD = 1.14 V at 25°C. (LEO, Adams 90% worst case); High Current SEFI characterization is performed at VDD = 1.26 V at 105°C. (LEO, Adams 90% worst case, 100mils Al)

Recommended Operation Conditions

Table 24: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
TOP	Temperature Range	-55	+125	°C
TC	Case Operating Temperature Range	-55	+125	°C
VDD	Supply Voltage /1 /2 /3	1.14	1.26	V
VPP	Activation Supply Voltage /3	2.375	2.75	V
VTT	Termination Voltage	0.565	0.640	V

NOTE:

1. JESD8-24 specifies Vref to be 70% of VDD.
2. DC bandwidth is limited to 20MHz.,
3. PODI2 1.2V Pseudo Open Drain Interface has a VDD value of 1.2V but the reference voltage allows PODI2 to be used with other VDD values. POD12 signals have pull-up-only parallel input termination and have an asymmetric output drive impedance. For example, if the output drivers were using a 60 ohm pull-up drive impedance then the pull-down drivers would be expected to produce a 40 ohm pull-down drive impedance. PODI2 does not explicitly call for series termination resistors, so it is suitable for point-to-point as well as multi-drop stub environments which may require some additional termination.

General Electrical Characteristics

Unless otherwise noted, TC is per the temperature range ordered.

DC Characteristics

Table 25: DC Characteristics

(VDD =1.16 to 1.26V; -55°C < TC < +125°C)

Parameter	Symbol	MIN	MAX	UNITS	Notes
AC input high voltage	VIH(AC)_RESET	0.8 × VDD	VDD	V	1
DC input high voltage	VIH(DC)_RESET	0.7 × VDD	VDD	V	2
DC input low voltage	VIL(DC)_RESET	VSS	0.3 × VDD	V	3
AC input low voltage	VIL(AC)_RESET	VSS	0.2 × VDD	V	4

Parameter	Symbol	MIN	MAX	UNITS	Notes
Rising time	tR_RESET	–	1	µs	5
RESET pulse width after power-up	tPW_RESET_S	1	–	µs	6, 7
RESET pulse width during power-up	tPW_RESET_L	200	–	µs	6
AC input high voltage	VIH(AC)	VREF + 100	VDD5	mV	8, 9, 10
DC input high voltage	VIH(DC)	VREF + 75	VDD	mV	8, 9
DC input low voltage	VIL(DC)	VSS	VREF - 75	mV	8, 9
AC input low voltage	VIL(AC)	VSS5	VREF - 100	mV	8, 9, 10
Reference voltage for CMD/ADDR inputs	VREFFCA(DC)	0.49 × VDD	0.51 × VDD	V	11
IDD0	Operating One Bank Active-Precharge Current	–	513	mA	
IPP0	Operating One Bank Active-Precharge IPP Current	–	27	mA	
IDD1	Operating One Bank Active-Read-Precharge Current	–	612	mA	
IDD2N	Precharge Standby Current	–	378	mA	
IDD2NT	Precharge Standby ODT Current	–	432	mA	
IDD2P	Precharge Power-Down Current	–	342	mA	
IDD2Q	Precharge Quiet Standby Current	–	378	mA	
IDD3N	Active Standby Current	–	522	mA	
IPP3N	Active Standby IPP Current	–	18	mA	
IDD3P	Active Power-Down Current	–	423	mA	
IDD4R	Operating Burst Read Current	–	1242	mA	
IDD4W	Operating Burst Write Current	–	1008	mA	
IDD5R	Burst Refresh Current	–	612	mA	
IPP5R	Burst Refresh IPP current	–	36	mA	
IDD7	Operating Bank Interleave Read Current	–	1611	mA	
IPP7	Operating Bank Interleave Read IPP Current	–	72	mA	
IDD8	Maximum Power Down Current	–	324	mA	

Notes:

1. Overshoot should not exceed the VIN shown in the Absolute Maximum Ratings table.

2. After RESET_n is registered HIGH, the RESET_n level must be maintained above VIH(DC)_RESET, otherwise operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. After RESET_n is registered LOW, the RESET_n level must be maintained below VIL(DC)_RE- SET during tPW_RESET, otherwise the DRAM may not be reset.
4. Undershoot should not exceed the VIN shown in the Absolute Maximum Ratings table.
5. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
6. RESET is destructive to data contents.
7. See RESET Procedure at Power Stable Condition (figure 14).
8. For input except RESET_n. VREF = VREFCA(DC).
9. VREF = VREFCA(DC).
10. Input signal must meet VIL/VIH(AC) to meet tIS timings and VIL/VIH(DC) to meet tIH timings.
11. The AC peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than ±1% VDD (for reference: approximately ±12mV).

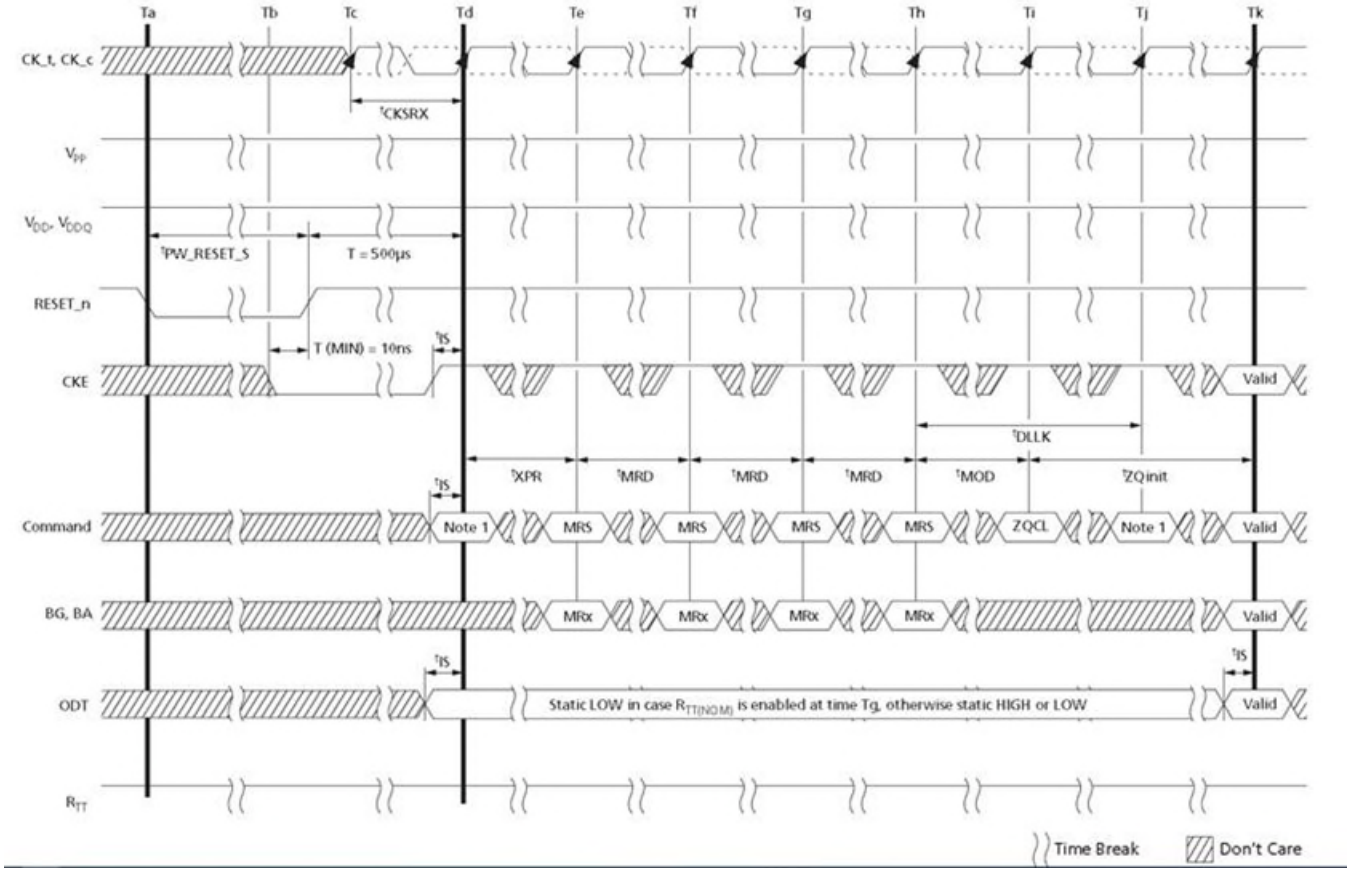

Figure 14: RESET Procedure at Power Stable Condition

AC Characteristics

Table 26: tREFI by Temperature

Parameter	Symbol		MIN	UNITS
Average periodic refresh interval	tREFI	-55°C ≤ Tcase ≤ 85°C (self/auto refresh)	7.8	µs
		85°C ≤ Tcase ≤ 95°C /1	3.9	µs
		95°C ≤ Tcase ≤ 105°C (manual refresh)	1.95	µs
		105°C ≤ Tcase ≤ 125°C (manual refresh)	0.4876	µs

Notes:

1. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range
2. 8192 cycle refresh is
   64ms between 0 to 85°C
   32ms between 85 to 95°C
   16ms between 95 to 105°C
   8ms between 105 to 125°C

Table 27: DDR4-2400 Speed Bins and Operating Conditions

Speed Bin				DDR4-2400		Unit	Note
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal read command to first data			^{t}AA	14.16[14] (13.75) [5,12]	19	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	^{t}AA(min) + 3nCK	^{t}AA(max) +3nCK	ns	
ACT to internal read or write delay time			^{t}RCD	14.16 (13.75) [5,12]	-	ns	
PRE command period			^{t}RP	14.16 (13.75) [5,12]	-	ns	
ACT to PRE command period			^{t}RAS	32	9 x ^{t}REFI	ns	
ACT to ACT or REF command period			^{t}RC	46.16 (45.75)[5,12]	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11	^{t}CK(AVG)	Reserved		ns	1,2,3,4,6,8
	CL=10	CL=12		1.5	1.9		
CWL=9, 11	CL=11	CL=13	^{t}CK(AVG)	1.25	<1.5	ns	1,2,3,4,5
	CL=12	CL=14					
CWL=10, 12	CL=13	CL=15	^{t}CK(AVG)	1.071	<1.25	ns	1,2,3,4,5
	CL=14	CL=16					
CWL=11, 14	CL=15	CL=17	^{t}CK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL=16	CL=18					

Speed Bin				DDR4-2400		Unit	Note
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
CWL=12, 16	CL=16	CL=19	^{t}CK(AVG)	Reserved		ns	1,2,3,4
	CL=17	CL=20		0.833	<0.937		
	CL=18	CL=21					
Supported CL Settings				10-18		nCK	7,8
Supported CL Settings with read DBI				12-16, 18-21		nCK	
Supported CWL Settings				9-12, 14, 16		nCK	

NOTE:

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. tREFI depends on TOPER.
6. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
7. The max values are system dependent.
8. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.

Table 28: Timing Parameters for Speed Grade DDR4-2400

Speed			DDR4-2400		Units	Note
Parameter		Symbol	Min	Max		
Clock period average (DLL off mode)		^{t}CK(DLL_OFF)	8	20	ns	
Average Clock Period		^{t}CK(avg,DLL_ON)	0.833	1.9	ns	3,13
Average high pulse width		^{t}CH(avg)	0.48	0.52	^{t}CK(avg)	
Average low pulse width		^{t}CL(avg)	0.48	0.52	^{t}CK(avg)	
Clock period jitter	Total	^{t}JITper_tot	-42	42	ps	17,18
	Deterministic	^{t}JITper_dj	-21	21	ps	17
	DLL locking	^{t}JITper_lck	-33	33	ps	
Absolute Clock Period		^{t}CK(abs)	tCK(avg)min + tJIT(per) min_tot	tCK(avg)max + tJIT(per)max_tot	ps	
Absolute clock HIGH pulse width		tCH(abs)	0.45	-	^{t}CK(avg)	
Absolute clock Low pulse width		tCL(abs)	0.45	-	^{t}CK(avg)	

Speed			DDR4-2400		Units	Note
Cycle to Cycle jitter	Total	^{t}JITcc_tot	-	83	ps	
	DLL locking	^{t}JITcc_lck	-	67	ps	
Cumulative error across	2 cycles	^{t}ERR(2per)	-61	61	ps	
	3 cycles	^{t}ERR(3per)	-73	73	ps	
	4 cycles	^{t}ERR(4per)	-81	81	ps	
	5 cycles	^{t}ERR(5per)	-87	87	ps	
	6 cycles	^{t}ERR(6per)	-92	92	ps	
	7 cycles	^{t}ERR(7per)	-97	97	ps	
	8 cycles	^{t}ERR(8per)	-101	101	ps	
	9 cycles	^{t}ERR(9per)	-104	104	ps	
	10 cycles	^{t}ERR(10per)	-107	107	ps	
	11 cycles	^{t}ERR(11per)	-110	110	ps	
	12 cycles	^{t}ERR(12per)	-112	112	ps	
	n = 13,14…49, 50 cycles	^{t}ERR(nper)	tERRnper MIN =(1+0.68ln[n]) x tJITper_tot MIN	tERRnper MAX =(1+0.68ln[n]) x tJITper_tot MAX	ps	
DQ Input Timing						
Data setup time to DQS_t,DQS_c	Base (calibrated V_{REF})	^{t}DS	Approximately 0.15^{t}CK to 0.28^{t}CK		-	
	Non-calibrated V_{REF}	^{t}PDA_S	Minimum of 0.5UI		UI	22
Data hold time from DQS_t,DQS_c	Base (calibrated V_{REF})	^{t}DH	Approximately 0.15^{t}CK to 0.28^{t}CK		-	
	Non-calibrated V_{REF}	^{t}PDA_H	Minimum of 0.5UI		UI	33
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	-	UI	
DQ Output Timing (DLL enabled)						
DQS_t, DQS_c to DQ skew, per gourp, per access		^{t}DQSQ	-	0.17	UI	
DQ output hold time from DQS_t,DQS_c		^{t}QH	0.74	-	UI	
Data Valid Window per device: ^{t}QH-^{t}DQSQ each device's output per UI		^{t}DVW$_{d}$	0.64	-	UI	
Data Valid Windo per device, per pin:^{t}QH-^{t}DQSQ each device's output per UI		^{t}DVW$_{p}$	0.72	-	UI	
DQ Low-Z time from CK_t,CK_c		^{t}LZDQ	-330	175	ps	
DQ High-Z time form CK_t,CK_c		tHZDQ	-	175	ps	
DQ Strobe Input Timing						
DQS_t,DQS_c rising edge to CK_t,CK_c rising edge for 1^{t}CKpreamble		^{t}DQSS$_{1ck}$	-0.27	0.27	CK	

Speed			DDR4-2400		Units	Note
DQS_t,DQS_c rising edge to CK_t,CK_c rising edge for 2tCKpreamble		$^{t}DQSS_{2ck}$	-0.50	0.50	CK	
DQS_t,DQS_c differential input low pulse width		$^{t}DQSL$	0.46	0.54	CK	
DQS_t,DQS_c differential input high pulse width		$^{t}DQSH$	0.46	0.54	CK	
DQS_t,DQS_c falling edge setup to CK_t,CK_c rising edge		^{t}DSS	0.18	-	CK	
DQS_t,DQS_c falling edge hold from CK_t,CK_c rising edge		^{t}DSH	0.18	-	CK	
DQS_t,DQS_c differential WRITE preamble for 1tCKpreamble		$^{t}WPRE_{1ck}$	0.9	-	CK	
DQS_t,DQS_c differential WRITE preamble for 2tCKpreamble		$^{t}WPRE_{2ck}$	1.8	-	CK	
DQS_t,DQS_c differential WRITE postamble		$^{t}WPST$	0.33	-	CK	
DQS Strobe Output Timing (DLL enabled)						
DQS_t,DQS_c rising edge output access time from rising CK_t,CK_c		$^{t}DQSCK$	-175	175	ps	
DQS_t,DQS_c rising edge output variance window per DRAM		$^{t}DQSCKi$	-	290	ps	
DQS_t,DQS_c differential output high time		^{t}QSH	0.4	-	CK	
DQS_t,DQS_c differential output low time		^{t}QSL	0.4	-	CK	
DQS_t,DQS_c Low-Z time (RL-1)		$^{t}LZDQS$	-330	175	ps	
DQS_t,DQS_c High-Z time (RL-1)		$^{t}HZDQS$	-	175	ps	
DQS_t,DQS_c differential READ preamble for 1tCKpreamble		$^{t}RPRE_{1ck}$	0.9	-	CK	20
DQS_t,DQS_c differential READ preamble for 2tCKpreamble		$^{t}RPRE_{2ck}$	1.8	-	CK	20
DQS_t,DQS_c differential READ postamble		$^{t}RPST$	0.33	-	CK	21
Command and Address Timing						
DLL locking time		$^{t}DLLK$	768	-	CK	2,4
CMD, ADDR setup time to CK_t, CK_c Base referenced to VIH(AC) and VIL(AC)	Base	^{t}IS	62	-	ps	
	VREFCA	$^{t}ISV_{REF}$	162	-	ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to VIH(AC) and VIL(AC)	Base	^{t}IH	87	-	ps	
	VREFCA	$^{t}IHV_{REF}$	162	-	ps	
CTRL,ADDR pulse width for each input		^{t}IPW	410	-	ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD		ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP		ns	
ACTIVATE to PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS		ns	12
ACTIVATE to ACTIVATE or REFcommand period		^{t}RC	See Speed Bin Tables for ^{t}RC		ns	12
ACTIVATE to ACTIVATE or command period to different bank groups for 1/2KB page size		$^{t}RRD_S$ (1/2KB)	MIN=greater of 4CK or 3.3ns		CK	1
ACTIVATE to ACTIVATE or command period to different bank groups for 1KB page size		$^{t}RRD_S$ (1KB)	MIN=greater of 4CK or 3.3ns		CK	1

Speed		DDR4-2400		Units	Note
ACTIVATE to ACTIVATE or command period to different bank groups for 2KB page size	^{t}RRD_S (1KB)	MIN=greater of 4CK or 5.3ns		CK	1
ACTIVATE to ACTIVATE or command period to same bank groups for 1/2KB page size	^{t}RRD_L (1/2KB)	MIN=greater of 4CK or 4.9ns		CK	1
ACTIVATE to ACTIVATE or command period to same bank groups for 1KB page size	^{t}RRD_L (1KB)	MIN=greater of 4CK or 4.9ns		CK	1
ACTIVATE to ACTIVATE or command period to same bank groups for 2KB page size	^{t}RRD_L (1KB)	MIN=greater of 4CK or 6.4ns		CK	1
Four ACTIVATE windows for 1/2KB page size	^{t}FAW (1/2KB)	MIN=greater of 16CK or 13ns		ns	
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN=greater of 20CK or 21ns		ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN=greater of 28CK or 30ns		ns	
WRITE recovery time	^{t}WR	MIN = 15ns		ns	5,9,1
	^{t}WR$_2$	MIN = 1CK + ^{t}WR		CK	5,10,1
WRITE recovery time when CRC and DM are both enabled	^{t}WR_CRC_DM	MIN = ^{t}WR + greater of (5CK or 3.75ns)		CK	6,9,1
	^{t}WR_CRC_DM$_2$	MIN = 1CK + ^{t}WR_CRC_DM		CK	6,10,1
Delay from start of internal WRITE transaction to internal READ command – Same bank group	^{t}WTR_L	MIN = greater of 4CK or 7.5ns		CK	5,9,1
	^{t}WTR_L$_2$	MIN = 1CK+^{t}WTR_L		CK	5,10,1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	^{t}WTR_L_CRC_DM	MIN = ^{t}WTR_L + greater of (5CK or 3.75ns)		CK	6,9,1
	^{t}WTR_L_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_L_CRC_DM		CK	6,10,1
Delay from start of internal WRITE transaction to internal READ command – different bank group	^{t}WTR_S	MIN = greater of (2CK or 2.5ns)		CK	5,7,8,9,1
	^{t}WTR_S$_2$	MIN = 1CK + ^{t}WTR_S		CK	5,7,8,10,1
Delay from start of internal WRITE transaction to internal READ command – different bank group when CRC and DM are both enabled	^{t}WTR_S_CRC_DM	MIN = ^{t}WTR_S + greater of (5CK or 3.75ns)		CK	6,7,8,9,1
	^{t}WTR_S_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_S_CRC_DM		CK	6,7,8,10,1
READ to PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns		CK	1
CAS_n to CAS_n command delay to different bank group	^{t}CCD_S	4	-	CK	
CAS_n to CAS_n command delay to same bank group	^{t}CCD_L	MIN = greater of 4CK or 5ns	-	CK	
Auto precharge write recovery + precharge time	^{t}DAK (MIN)	MIN = WR + ROUNDtRP/tCK (AVG); MAX=N/A		CK	8
MRS Command Timing					
MRS command cycle time	^{t}MRD	8	-	CK	
MRS command cycle time in PDA mode	^{t}MRD_PDA	MIN = greater of (16nCK, 10ns)		CK	1
MRS command cycle time in CAL mode	^{t}MRD_CAL	MIN=^{t}MOD + ^{t}CAL		CK	
MRS command update delay	^{t}MOD	MIN = greater of (24nCLK, 15ns)		CK	1

Speed		DDR4-2400		Units	Note
MRS command update delay in PDA mode	^{t}MOD_PDA	MIN = ^{t}MOD		CK	
MRS command update delay in CAL mode	^{t}MOD_CAL	MIN = ^{t}MOD + ^{t}CAL		CK	
MRS command to DGS drive in preamble training	^{t}SDO	MIN = ^{t}MOD + 9ns		ns	
MPR Command Timing					
Multipurpose register recovery time	^{t}MPRR	MIN = 1CK		CK	
Multipurpose register write recovery time	^{t}WR_MPR	MIN = ^{t}MOD + AL + PL			
CRC Error Reporting Timing					
CRC error to ALERT_n latency	^{t}CRC_ALERT	3	13	ns	
CRC Alert_n pulse width	^{t}CRC_ALERT_PW	6	10	CK	
Parity latency	PL	5	-	CK	
Command uncertain to be executed during this time	^{t}PAR_UNKNOWN	-	PL	CK	
Delay from errant command to ALERT_n assertion	^{t}PAR_ALERT_ON	-	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	^{t}PAR_ALERT_PW	72	144	CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^{t}PAR_ALERT_RS_P	-	64	CK	
CAL Timing					
CS_n to command address latency	^{t}CAL	5	-	CK	19
CS_n to command address latency in gear-down mode	^{t}CALg	N/A	-	CK	
MPSM Timing					
Command path disable delay upon MPSM entry	^{t}MPED	MIN = ^{t}MOD (MIN) + ^{t}CPED (MIN)		CK	1
Valid clock requirement after MPSM entry	^{t}CKMPE	MIN = ^{t}MOD (MIN) + ^{t}CPED (MIN)		CK	1
Valid clock requirement after MPSM exit	^{t}CKMPX	MIN = ^{t}CKSRX (MIN)		CK	1
Exit MPSM to commands not requiring a locked DLL	^{t}XMP	^{t}XS (MIN)		CK	
Exit MPSM to commands requiring a locked DLL	^{t}XMPDLL	MIN = ^{t}XMP (MIN) + ^{t}XSDLL (MIN)		CK	1
CS setup time to CKE	^{t}MPX_S	MIN – ^{t}IS (MIN) + ^{t}IH (MIN)		ns	
CS_n HIGH hold time to CKE rising edge	^{t}MPX_HH	MIN = ^{t}XP		ns	
CS_n LOW hold time to CKE rising edge	^{t}MPX_LH	12	tXMP-10ns	ns	
Connectivity Test Timing					
TEN pin HIGH to CS_n LOW – Enter CT mode	^{t}CT_Enable	200	-	ns	
CS_n LOW and valid input to valid output	^{t}CT_Valid	-	200	ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH	^{t}CTCKE_Valid	10	-	ns	
Calibration and V_{REFDQ} Train Timing					

Speed			DDR4-2400		Units	Note
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	1024	-	CK	
	Normal operation	^{t}ZQoper	512	-	CK	
ZQCS command: Short calibration time		^{t}ZQCS	128	-	CK	
The V_{REF} increment/decrement step time		V_{REF_time}	MIN = 150 ns		ns	
Enter V_{REFDQ} training mode to the first write or VREFDQ MRS command delay		^{t}VREFDQE	MIN = 150 ns		ns	
Exit V_{REFDQ} training mode to the first write command delay		^{t}VREFDQX	MIN = 150 ns		ns	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		^{t}XPR	MION = greater of 5CK or ^{t}RFC (MIN) + 10 ns		CK	1
RESET_L pulse low after power stable		^{t}PW_RESET_S	1.0	-	µs	
RESET_L pulse low at power up		^{t}PW_RESET_L	200	-	µs	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200		ms	
RESET_n LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 0		ns	
Refresh Timing						
Refresh to ACTIVATE or REFRESH command period (all banki groups)		^{t}RFC1	MIN = 350		ns	1,11
		^{t}RFC2	MIN = 260		ns	1,11
		^{t}RFC4	MIN =160		ns	1,11
Average periodic refresh interval	-55°C ≤ T_C ≤ 85°C	^{t}REFI	MIN = N/A;MAX = 7.8		µs	11
	85°C ≤ T_C ≤ 95°C	^{t}REFI	MIN = N/A;MAX = 3.9		µs	11
	95°C ≤ T_C ≤ 105°C	^{t}REFI	MIN = N/A;MAX = 1.95		µs	11
Self Refresh Timing						
Exit self refresh commands not requiring a locked DLL		^{t}XS	MIN = ^{t}RFC + 10-ns		ns	1
Exit self refresh commands not requiring a locked DLL in self refresh abort		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10-ns		ns	1
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and geardown)		^{t}XS_FAST	MIN= ^{t}RFC4 + 10-ns		ns	1
Exit self refresh commands requiring a locked DLL		^{t}XSDLL	MIN= ^{t}DLLK (MIN)		CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + 1nCK		CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled		^{t}CKESR_PAR	MIN = ^{t}CKE (MIN) + 1nCK + PL		CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)		^{t}CKSRE	MIN=greater of (5CK, 10ns)		CK,ns	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled		^{t}CKSRE_PAR	MIN = greater (5CK, 10ns) + PL		CK,ns	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit		^{t}CKSRX	MIN = greater of (5CK, 10ns)		CK,ns	1

Speed		DDR4-2400		Units	Note
Power-Down Timing					
Exit power-down with DLL on to any valid command	^{t}XP	MIN = greater of 4CK or 6ns		CK,ns	1
Exit power-down with DLL on to any valid command when CA parity is enabled	^{t}XP_PAR	MIN = (greater of 4CK or 6ns) + PL		CK,ns	1
CKE MIN pulse width	^{t}CKE (MIN)	MIN = greater of 3CK or 5ns		CK,ns	1
Command pass disable delay	^{t}CPDED	4	-	CK	
Power-down entry to power-down exit timing	^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 x ^{t}REFI		CK	
Begin power-down period prior to CKE registered HIGH	^{t}ANPD	WL-1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^{t}ANPD or ^{t}RFC – REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	^{t}ANPD + ^{t}XSDLL		CK	
Power-Down Entry Minimum timing					
ACTIVATE command to power-down entry	^{t}ACTPDEN	2	-	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	^{t}PRPDEN	2	-	CK	
REFRESH command to power-down entry	^{t}REFDEN	2	-	CK	
MRS command to power-down entry	^{t}MRSDEN	MIN= ^{t}MOD (MIN)		CK	1
READ/READ with auto precharge command to power-down entry	^{t}RDPDEN	MIN = RL + 4 + 1		CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)		CK	1
WRITE command to power-down entry (BC4MRS)	^{t}WRPBC4DEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)		CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRAPDEN	MIN = WL + 4 + WR + 1		CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1		CK	1
ODT Timing					
Direct ODT turn-on latency	DODTLon	WL -2 = CWL + AL + PL -2		CK	
Direct ODT turn-off latency	DODTLoff	WL -2 = CWL + AL + PL -2		CK	
R_{tt} dynamic change skew	^{t}ADC	0.3	0.7	CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	^{t}AONAS	1	9	ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	^{t}AOFAS	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1^{t}CK	6	-	CK	
	ODTH8 2^{t}CK	7	-		
ODT HIGH time without WRITE command or with WRITE command and BC8	ODTH4 1^{t}CK	4	-	CK	
	ODTH4 2^{t}CK	5	-		
Write Leveling Timing					

Speed		DDR4-2400		Units	Note
First DQS_t, DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	CK	
DQS_t, DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	CK	
Write leveling setup from rising CK_t. CK_c crossing ro rising DQS_t, DQS_c crossing	tWLS	0.13	-	tCK (AVG)	
Write leveling hold from rising CK_t. CK_c crossing ro rising DQS_t, DQS_c crossing	tWLH	0.13	-	tCK (AVG)	
Write leveling output delay	tWLO	0	0.95	ns	
Write leveling output error	tWLOE	0	2	ns	

Notes:

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See 0.1.3 “Power-Down clarifications - Case 2” in RB11112 . — DQ Receiver(Rx) compliance mask
9. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
10. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
11. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
12. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
13. The max values are system dependent.
14. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.
15. The deterministic component of the total timing.
16. DQ to DQ static offset relative to strobe per group.
17. This parameter will be characterized and guaranteed by design.
18. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output) Deratings are relative to the SDRAM input clock).
19. DRAM DBI mode is off.
20. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
21. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
23. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
24. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge

25. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
26. Total jitter includes the sum of deterministic and random jitter terms for a specified BER.
27. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
28. This parameter has to be even number of clocks
29. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
30. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
31. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
32. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
33. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width). UI=tCK(avg).min/2

Packaging

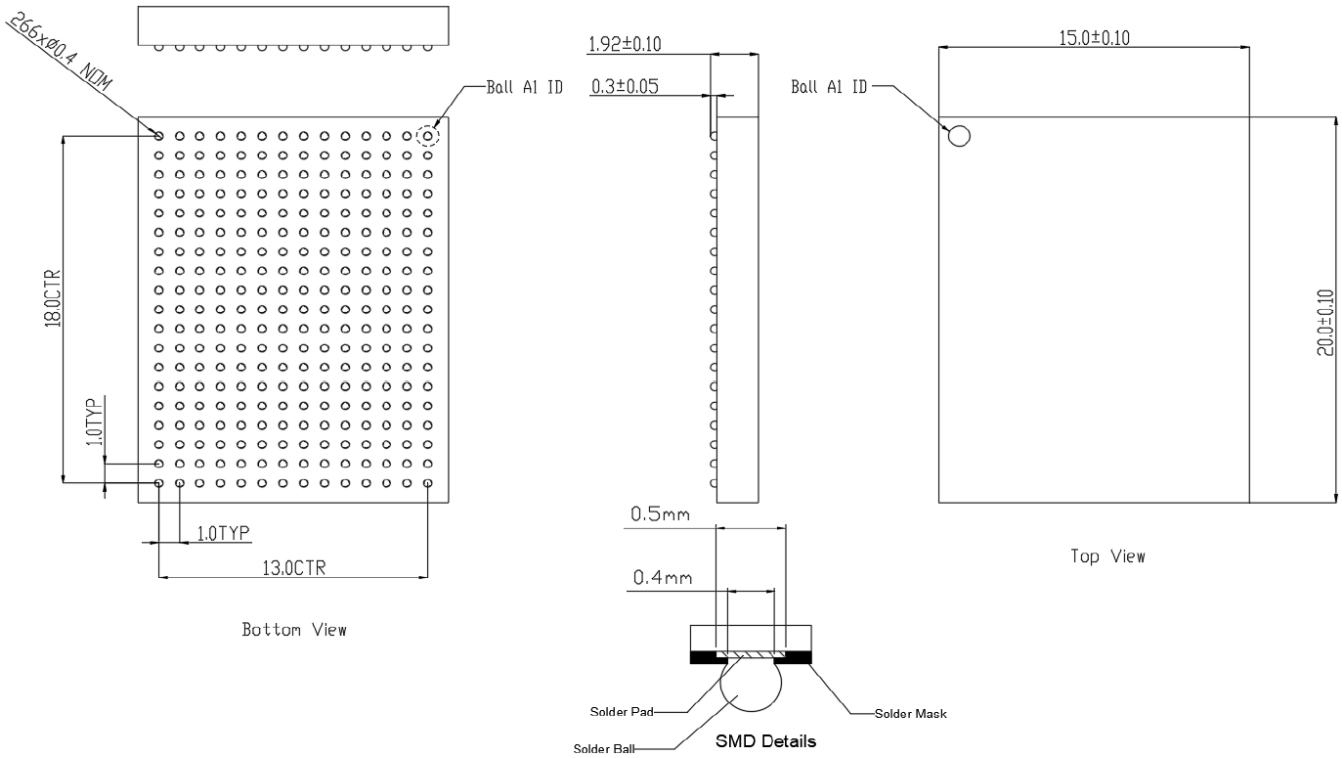

Figure 15: 266 pin CCGA/LCGA Package Outline (Bottom View)

Note: The weight is 1.1703 grams

Ordering information

Frontgrade Part Number Ordering information

Generic Data Sheet Part Numbering

UT8SD4MQ2G72 * * * *

Lead Finish:

(H)	**=**	**Eutectic Solder Ball (63 Sn 37 Pb)**
(G)	**=**	**SAC305 Solder Ball**

Screening Level: (Notes: 1,2)

(P)	**=**	**Prototype Flow**	**(Temperature Range: 25°C only)**
(I)	**=**	**PEM QD Flow**	**(Temperature Range: -55°C to 125°C)**
(L)	**=**	**Space PEM QD Flow**	**(Temperature Range: -55°C to 125°C)**
(X2)	**=**	**Space PEM Level 2 Flow**	**(Temperature Range: -55°C to 125°C)**

Case Outline:

(M)	**=**	**266-lead Ball Grid Array Package (BGA)**

Radiation Harness Assurance

(-)	**=**	**No RHA**
(L)	**=**	**50krad(Si)**

UT8SD4MQ2G72 = 18GB DDR4 DRAM

Notes:

1. Prototype Flow per Frontgrade Manufacturing Flows Document.
2. For Prototype and PEM QD Flows, radiation is neither tested nor guaranteed.

Revision History

Date	Revision	Change Description
12/04/25	1.0.0	Initial Release. Updated TID ratings from Adv Datasheet

Datasheet Definitions

	DEFINITION
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change. Specifications can be TBD and the part package and pinout are not final.
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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