DATASHEET

REV D: 03/08/21

SCD8540

64-Channel Analog Multiplexer, 32-Channel Kelvin

RHD8540

Features

- 64 channels (32 Kelvin measurement channels) provided by six 16-channel multiplexers
- Single power supply operation at +5V
- Radiation performance
  - Total Dose: >1 Mrad(Si), Dose rate = 50-300 rad(Si)/s
  - ELDRS Immune
  - SEL Immune: >100 MeV-cm^2/mg
  - Neutron Displacement Damage: >10^{14} neutrons/cm^2
- Full military temperature range
- Low power consumption < 33.6 mW
- CMOS analog switching allows rail to rail operation and low switch impedance
- Two address busses A(0-3) & B(0-3) and four enable lines afford flexible organization
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 96 leads, 1.320"Sq x 0.200"Ht quad flat pack
  - Weight - 15 grams max
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

The RHD8540 is a radiation hardened, single supply, 64-Channel Multiplexer MCM (multi-chip module). The RHD8540 design uses specific circuit topology and layout methods to mitigate total ionization dose effects and single event latchup. These characteristics make the RHD8540 especially suited for the harsh environment encountered in Deep Space missions. It is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD8540 is ideal for demanding military and space applications.

Organization and Application

The RHD8540 consists of six single supply, 16-Channel Multiplexers arranged as shown in the Block Diagram. The RHD8540 design is inherently radiation tolerant. The device will not latch with SEU events to above 100MeV-cm^2/mg. Total dose degradation is minimal to above 1Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

A Section

Thirty-two (32) channels addressable by bus A_0~A_3, in two 16 channel blocks, each block enabled separately. Each block connects the addressed channel to two outputs, "Output" and "Current". This technique enables selecting and reading a remote resistive sensor without the multiplexer resistance being part of the measurement. For grounded sensors, this is done by passing current to the sensor by means of the "Current" pin and reading the resultant voltage (proportional to the sensor resistance) at the "Output" pin.

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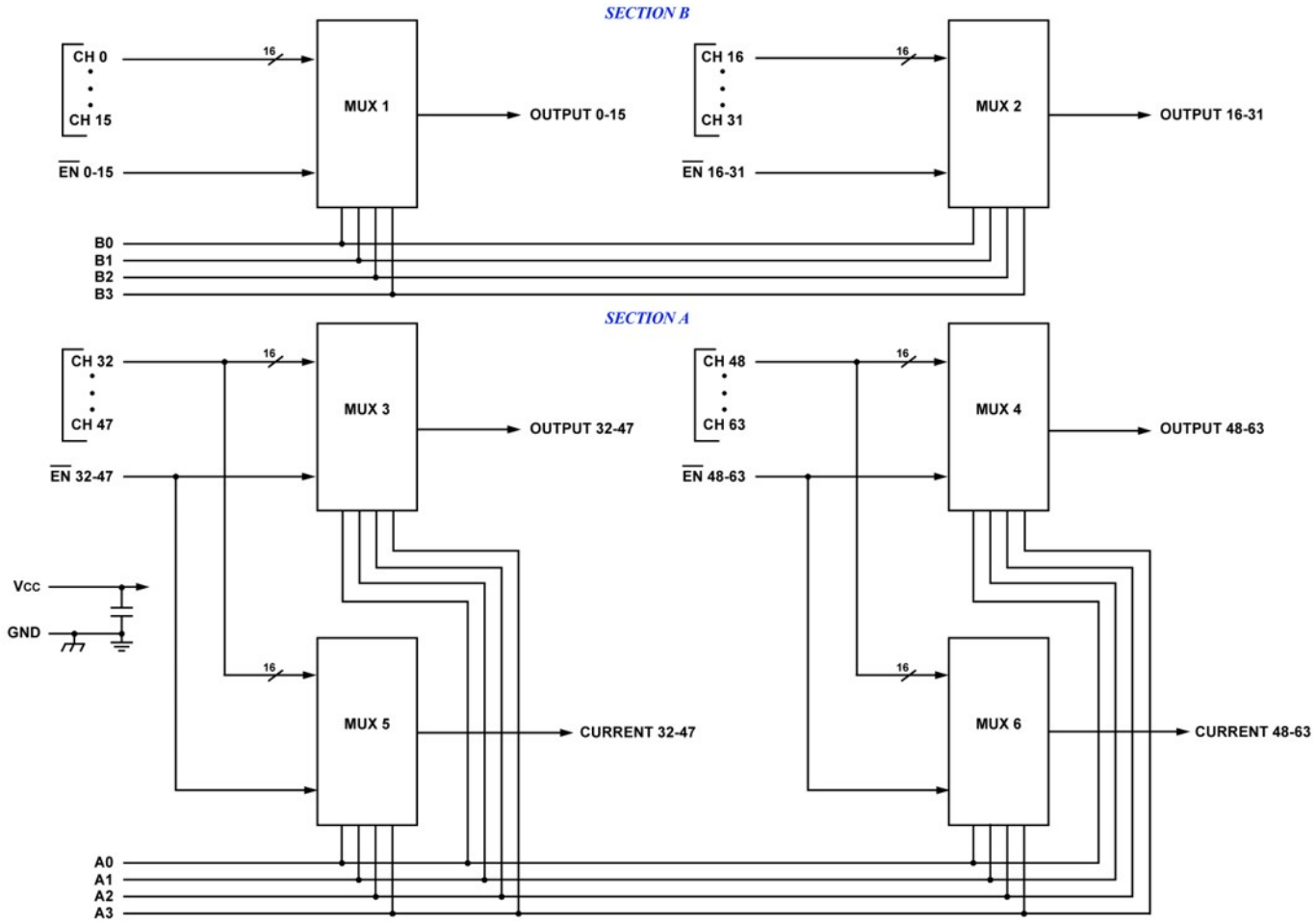
B Section

Thirty-two (32) channels addressable by bus B_0~B_3, in two 16 channel blocks, each block enabled separately. Each block connects the addressed channel to one output. By paralleling the channel inputs and enables, this section can be converted to act like one of the 16 channel blocks of the A section.



RHD8540 64 –Channel Analog MUX Block Diagram

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Absolute Maximum Ratings 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Supply Voltage $+V_{CC}$ (Pin 44)	+7.0	V
Digital Input Overvoltage V_{EN} (Pins 5, 6, 91, 92), V_A (Pins 1, 3, 93, 95), V_B (Pins 2, 4, 94, 96)	< V_{CC} +0.4 > GND -0.4	V V
Analog Input Over Voltage V_{IN} (CH0-CH63)	< V_{CC} +0.4 > GND - 0.4	V
Input Current	±10	mA

Note:

1) All measurements are made with respect to ground.

Notice: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress rating only; functional operation beyond the 'Operation Conditions' is not recommended and extended exposure beyond the 'Operation Conditions' may affect device reliability.

Recommended Operating Conditions 1/

Symbol	Parameter	Typical	Units
$+V_{CC}$	Power Supply Voltage	+5.0	V
V_{EN_L}, V_{A_L}	Logic Low Level	GND to 30% V_{CC}	V
V_{EN_H}, V_{A_H}	Logic High Level	70% V_{CC} to V_{CC}	V

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DC Electrical Performance Characteristics 1/

(T_C = -55°C to +125°C, $+V_{CC}$= +5V - Unless Otherwise Specified)

Parameter	Symbol	Conditions		MIN	MAX	Units
Supply Current $+V_{CC}$	$+I_{CC}$	$\overline{EN}$ = 30% V_{CC}		0	4.8	mA
	$+I_{SBY}$	$\overline{EN}$ = 70% V_{CC}		0	1.2	mA
Address Input Current A(0-3)	$I_{AL}(0\text{-}3)_A$	V_A = 30% V_{CC}, 7/	+25°C	-20	20	nA
			+125°C	-200	200	nA
	$I_{AL}(0\text{-}3)_B$	V_A = 30% V_{CC}, 7/	+25°C	-10	10	nA
			+125°C	-100	100	nA
	$I_{AH}(0\text{-}3)_A$	V_A = 70% V_{CC}, 7/	+25°C	-20	20	nA
			+125°C	-200	200	nA
	$I_{AH}(0\text{-}3)_B$	V_A = 70% V_{CC}, 7/	+25°C	-10	10	nA
			+125°C	-100	100	nA
Enable Input Current $\overline{EN}$	$I_{ENL}(0\text{-}15)$ $I_{ENL}(16\text{-}31)$	V_{EN} = 30% V_{CC}	+25°C	-5	5	nA
			+125°C	-50	50	nA
	$I_{ENL}(32\text{-}47)$ $I_{ENL}(48\text{-}63)$	V_{EN} = 30% V_{CC}, 7/	+25°C	-10	10	nA
			+125°C	-100	100	nA
	$I_{ENH}(0\text{-}15)$ $I_{ENH}(16\text{-}31)$	V_{EN} = 70% V_{CC}	+25°C	-5	5	nA
			+125°C	-50	50	nA
	$I_{ENH}(32\text{-}47)$ $I_{ENH}(48\text{-}63)$	V_{EN} = 70% V_{CC}, 7/	+25°C	-10	10	nA
			+125°C	-100	100	nA
High Input Leakage Current (CH0-CH31)	I_{INLK_5}	V_{IN} = +5V, V_{EN} = 80% V_{CC}, Output and all unused MUX inputs under test = 0V	+25°C	-5	5	nA
			+125°C	-50	50	nA
High Input Leakage Current (CH32-CH63), 7/			+25°C	-10	10	nA
			+125°C	-100	100	nA
Low Input Leakage Current (CH0-CH31)	I_{INLK_0}	V_{IN} = 0V, V_{EN} = 80% V_{CC}, Output and all unused MUX inputs under test = +5V	+25°C	-5	5	nA
			+125°C	-50	50	nA
Low Input Leakage Current (CH32-CH63), 7/			+25°C	-10	10	nA
			+125°C	-100	100	nA
Output Leakage Current V_{OUT} (pins 25,26, 68 & 70) CURRENTS (pins 67 & 69)	I_{OUTLK}	V_{OUT} = +5V, V_{EN} = 80% V_{CC}, All inputs grounded. 3/, 4/	+25°C	-5	5	nA
			+125°C	-50	50	nA
Switch ON Resistance OUTPUTS (pins 25,26, 68 & 70) CURRENTS (pins 67 & 69)	$R_{DS(ON)}$	V_{IN} = 0V, V_{EN} = 30% V_{CC}, I_{OUT} = +1mA V_{IN} = +2.5V, V_{EN} = 30% V_{CC}, I_{OUT} = -0.6mA V_{IN} = +5V, V_{EN} = 30% V_{CC}, I_{OUT} = -1mA 2/, 3/, 5/, 6/	-55°C	-	500	Ω
			+25°C	-	750	Ω
			+125°C	-	1000	Ω

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Notes:

1) Measure inputs sequentially. Ground all unused inputs of the device under test. V_A is the applied input voltage to the address lines A(0-3). V_B is the applied input voltage to the address lines B(0-3).
2) V_{IN} is the applied input voltage to the input channels (CH0-CH63).
3) V_{EN} is the applied input voltage to the enable lines $\overline{EN}$ (0-15), $\overline{EN}$ (16-31), $\overline{EN}$ (32-47) and $\overline{EN}$ (48-63).
4) V_{OUT} is the applied input voltage to the output lines OUTPUT1(0-15), OUTPUT2(16-31), OUTPUT3(32-47) and OUTPUT4(48-63), CURRENT(32-47) and CURRENT(48-63).
5) Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.
6) The RHD8540 cannot be operated with analog inputs below 0 volts.
7) For these signals, the leakage current is the sum of the individual leakage currents.

Switching Characteristics

(T_C = -55°C to +125°C, $+V_{CC}$ = +5V - Unless otherwise specified)

Parameter	Symbol	Conditions	TEMP	MIN	MAX	Units
Address to Output Delay	t_AHL	V_{OUT} High to Low Transition	-55°C	10	150	ns
			+25°C	10	150	ns
			+125°C	10	200	ns
	t_ALH	V_{OUT} Low to High Transition	-55°C	10	150	ns
			+25°C	10	150	ns
			+125°C	10	200	ns
Enable to Output Delay	$t_{ON}EN$	V_{EN} = 30% V_{CC} (Enabled)	-55°C	10	150	ns
			+25°C	10	150	ns
			+125°C	10	200	ns
	$t_{OFF}EN$	V_{EN} = 70% V_{CC} (Disabled)	ALL	10	200	ns

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Truth Table (CH0 – CH15)

B3	B2	B1	B0	$\overline{EN}$(0-15)	"ON" Channel 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between (CH0-CH15) and OUTPUT1(0-15)

Truth Table (CH16 – CH31)

B3	B2	B1	B0	$\overline{EN}$(16-31)	"ON" Channel 2/
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

2/ Between (CH16-CH31) and OUTPUT2 (16-31)

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Truth Table (CH32 – CH47)

A3	A2	A1	A0	$\overline{EN}$(32-47)	"ON" Channel 3/
X	X	X	X	H	NONE
L	L	L	L	L	CH32
L	L	L	H	L	CH33
L	L	H	L	L	CH34
L	L	H	H	L	CH35
L	H	L	L	L	CH36
L	H	L	H	L	CH37
L	H	H	L	L	CH38
L	H	H	H	L	CH39
H	L	L	L	L	CH40
H	L	L	H	L	CH41
H	L	H	L	L	CH42
H	L	H	H	L	CH43
H	H	L	L	L	CH44
H	H	L	H	L	CH45
H	H	H	L	L	CH46
H	H	H	H	L	CH47

3/ Between (CH32-CH47) and OUTPUT3 (32-47)

Truth Table (CH48 – CH63)

A3	A2	A1	A0	$\overline{EN}$(48-63)	"ON" Channel 4/
X	X	X	X	H	NONE
L	L	L	L	L	CH48
L	L	L	H	L	CH49
L	L	H	L	L	CH50
L	L	H	H	L	CH51
L	H	L	L	L	CH52
L	H	L	H	L	CH53
L	H	H	L	L	CH54
L	H	H	H	L	CH55
H	L	L	L	L	CH56
H	L	L	H	L	CH57
H	L	H	L	L	CH58
H	L	H	H	L	CH59
H	H	L	L	L	CH60
H	H	L	H	L	CH61
H	H	H	L	L	CH62
H	H	H	H	L	CH63

4/ Between (CH48-CH63) and OUTPUT4 (48-63)

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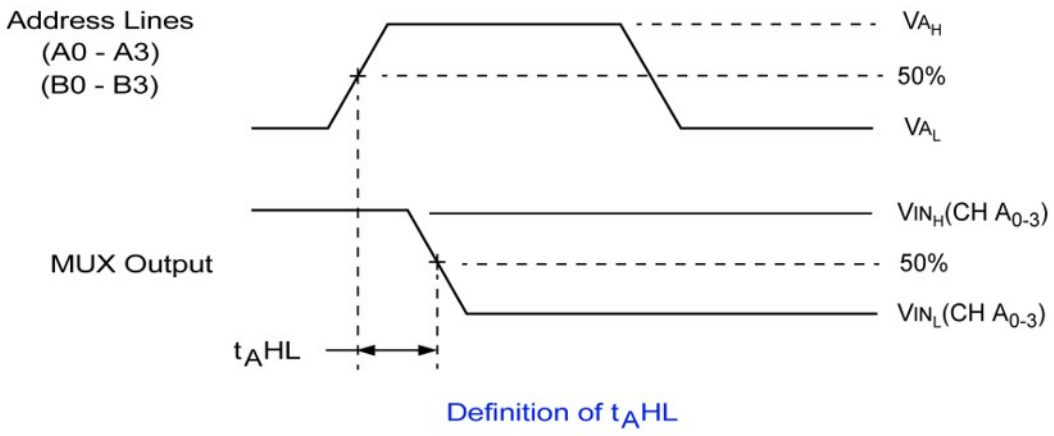
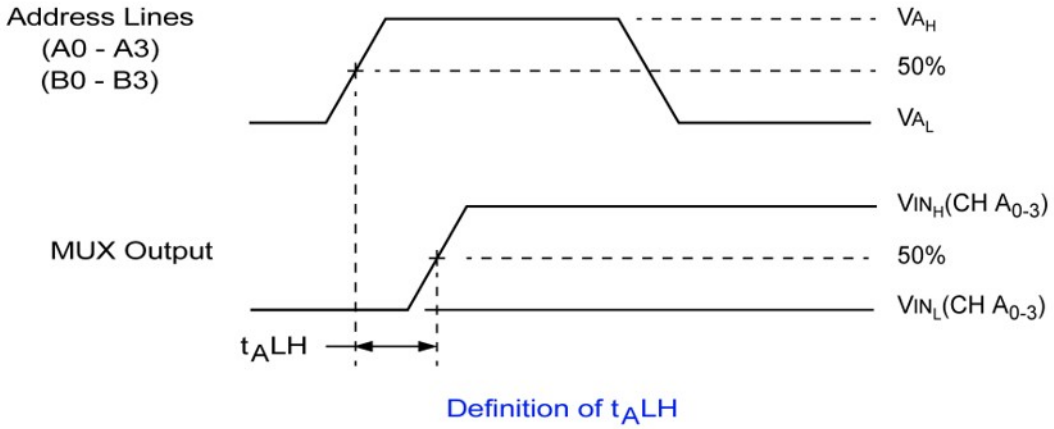
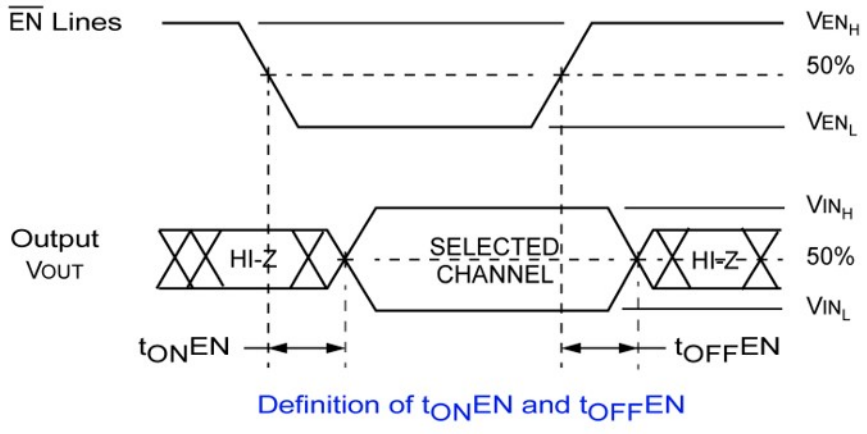


Definition of t_AHL



Definition of t_ALH



Definition of $t_{ON}EN$ and $t_{OFF}EN$

RHD8540 Switching Diagrams

Notes:

1) f = 10KHz, Duty cycle = 50%.

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Pin Numbers & Functions

RHD8540 – 96 Leads Ceramic QUAD Flat Pack

Pin #	Function	Pin #	Function	Pin #	Function
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	Output I(48-63)
4	B3	36	CH28	68	Output V(48-63)
5	$\overline{EN}$ (0-15)	37	CH13	69	Output I(32-47)
6	$\overline{EN}$ (16-31)	38	CH29	70	Output V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	$+V_{CC}$	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	NC	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	NC	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	CASE GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	Output1 (0-15)	57	CH57	89	GND
26	Output2 (16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ (48-63)
28	CH24	60	CH54	92	$\overline{EN}$ (32-47)
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

Note:

1) It is recommended that all "NC" or "no connect" pins be grounded. This eliminates or minimizes any ESD or static buildup.

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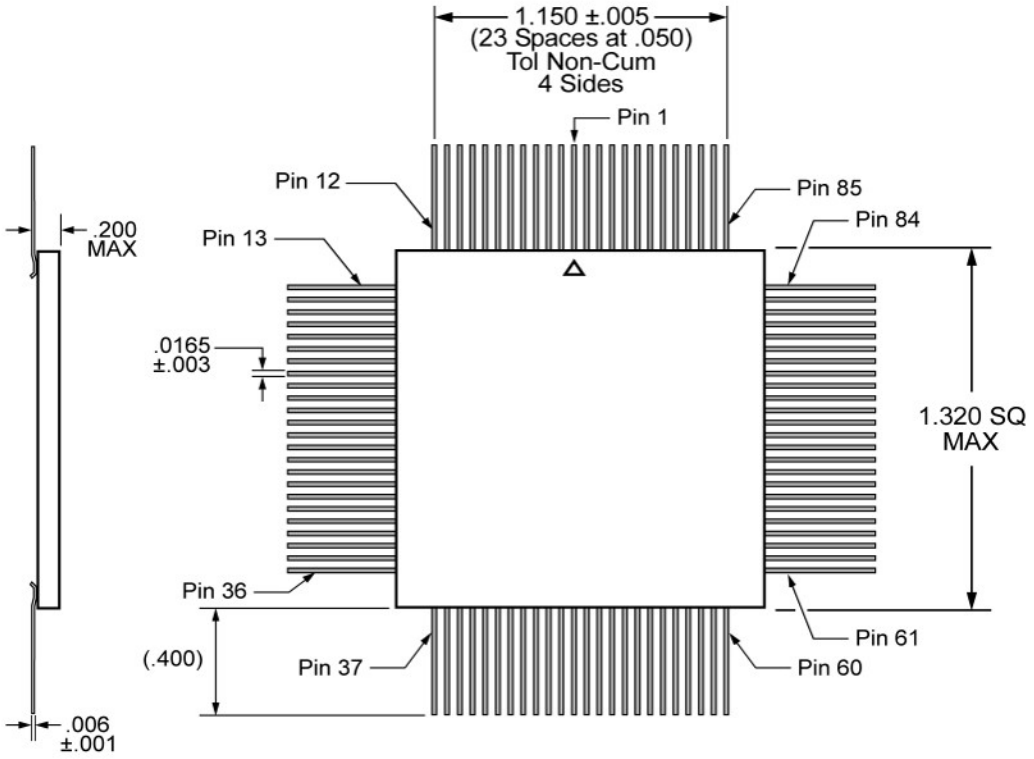

Flat Package Outline

Note:

1) Outside ceramic tie bars not shown for clarity. Contact factory for details.

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Ordering Information

Model Number	DLA SMD #	Screening	Package
RHD8540-7	-	Commercial Flow, +25°C testing only	QUAD Flat Pack
RHD8540-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD8540-201-1S	5962-1124001KXC	In accordance with DLA SMD	
RHD8540-901-1S	5962H1124001KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "H", 1 Mrad(Si)	

Revision History

Date	Revision	Change Description
03/30/2016	B	Import into CAES format
03/29/2017	C	Change status to Advanced, Remove 3.3V references, Correct Section A, Remove the resistor in the V_{CC} line, Add Max Input Current, Typical ranges in Recommended table, Add note 7/, Update switching diagram
03/08/2021	D	Revised Per ECN 23542

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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