SCD5032

High Speed PWM Controller

# PWM5031/5032/5034

## Features

- Radiation performance
  - Total dose      > 1 Mrad(Si),    Dose rate = 50 – 300 rad(Si)/s
  - ELDRS          > 50 Krad(Si),   Dose rate = 10 mrad(Si)/s
  - SEL:            Immune to 100 MeV-cm$^2$ / mg
  - SEU:           Immune up to 20 MeV-cm$^2$ / mg
    (Upsets found were benign and non-stressful to the PWM or supporting electronic components)
    (Neutron Testing Not Performed)
- CMOS low power design
- Sleep & enable control lines
- Optimized for applications: buck, boost, flyback, forward and center tapped push-pull converters
- Supports current mode or voltage mode operations
- Selectable 50% / 100% duty cycle
- Under-Voltage lockout with hysteresis
- Dual ±1Amp peak totem pole outputs
- 1 MHz maximum – user selectable
- Low Rho error amp
- Auxiliary op amp with shut down pin
- Power OK indicator
- PWM5034 - Same as PMW5032 except straight leads
- Designed for commercial, aerospace and high reliability space applications
- Ceramic 24-lead, hermetic package, .606"L x .293"W x .105"H
  - PWM5032 Gull Wing leads
  - PWM5034 Straight leads
  - Weight: 1.0 g max
- Evaluation board available for test and evaluation. See Application Note AN5031-1
  *Developed in Partnership with JHU/APL and the Technology Application Group for the Mars Technology Program; Part of NASA's Mars Exploration Program*
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

## Introduction

The chip is a fixed frequency Pulse Width Modulator based on the industry standard UC1843x Series with significant enhancements in performance and functionality. The chip operates in either the voltage or current mode and can support a wide variety of converter topologies.

Radiation hardened by design techniques ensure the chip's outstanding radiation tolerance, > 1 Mrad(Si), while reducing operating current by more than an order of magnitude over comparable parts.

The PWM5032 provides an under-voltage lockout feature with hysteresis that also provides an output to indicate Power is OK. An input called Sleep is used to power down the entire chip, the Enable input is used to shut down the Oscillator / Output Drives, and the Soft input drives the Output to zero. There is also a signal input called ENAUX that is used to disable the output to the auxiliary op-amp. The dual output drivers are designed using a Totem Pole output capable of sinking and sourcing 50mA constant current and peak currents up to 1 Amp to support a large variety of Power MOSFETs.

## SCD5032

High Speed PWM Controller

# PWM5031/5032/5034

Additional features that boost the appeal and utility of the part are:

- Dual break-before-make Totem Pole output stage is employed that virtually eliminates cross conduction and current shoot through
- Logic level input that allows the user to select either 50% or 100% maximum duty cycle operation
- Improved oscillator stage that vastly increases waveform linearity and reduces output voltage error
- Uncommitted on-board op-amp which can be used for signal conditioning, pulse feedback, or any other user defined purpose
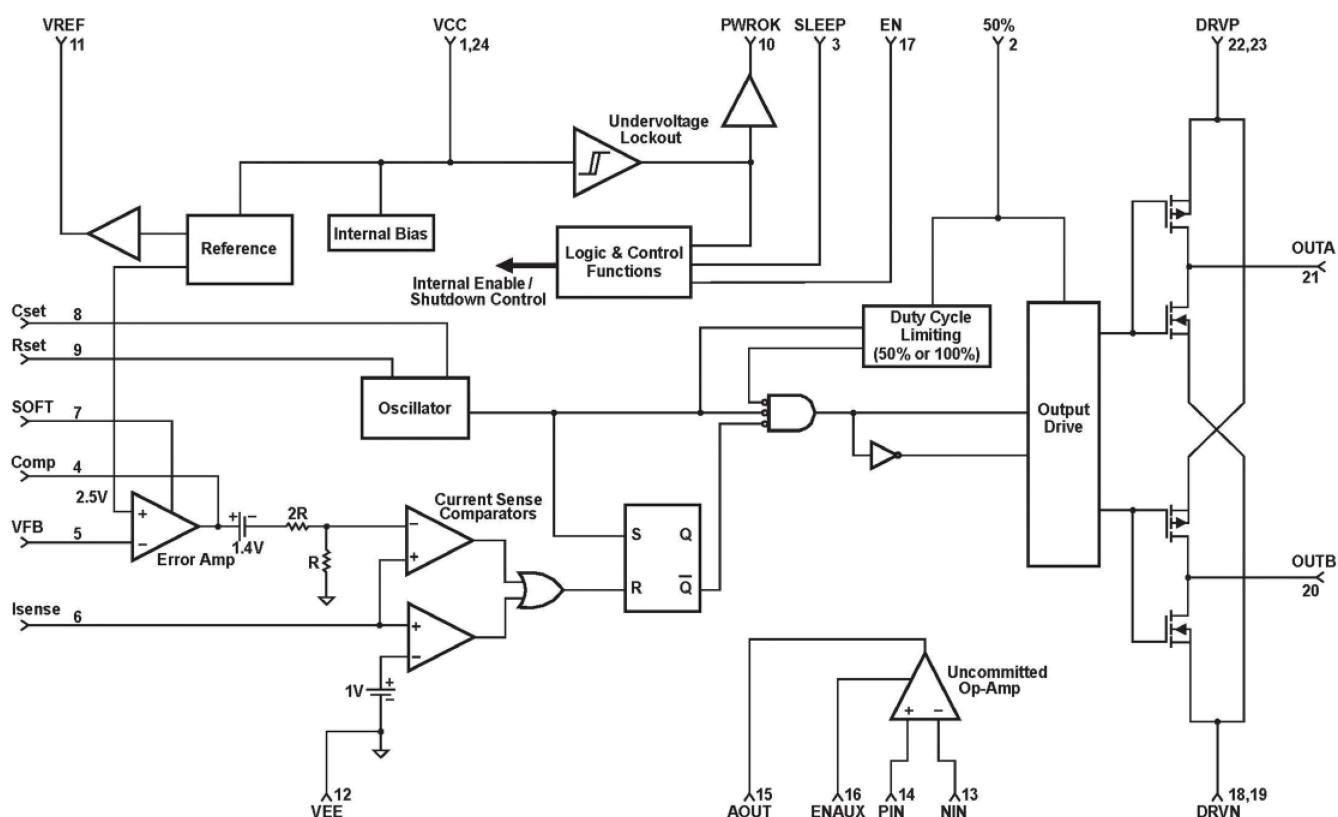
## Block Diagram



Figure 1: Block diagram

## SCD5032

High Speed PWM Controller

# PWM5031/5032/5034

**Pinlist**

**Table 1: PWM5032 PWM PIN Description**

| Number | Name | Description |
|--------|------|-------------|
| 1<br>24 | VCC | Logic Power |
| 2 | 50% | Input selects maximum duty cycle (50% or 100%). Logic "1" selects 50% max duty cycle and Output B is the complement of Output A. Logic "0" selects 100% and Output A is in-phase with Output B. |
| 3 | SLEEP | This Input shuts down all functions on chip when asserted (Active Hi) |
| 4 | COMP | Output of the error amplifier. Place compensation network from this pin to VFB to stabilize converter. |
| 5 | VFB | Negative Input to the error amplifier |
| 6 | ISENSE | Input Current sense pin used for current mode control |
| 7 | SOFT | This High impedance Input is used to limit the error amplifier output voltage. Applying an RC circuit to this pin provides the standard softstart function. Pull this pin to ground to force zero duty cycle. **NOTE: Do not tie this pin directly to VCC. Pull to VCC through a 1K minimum resistor. This input is internally routed to ground when Enable (pin 17) is low, Sleep (pin 3) is high or an Under Voltage is detected. |
| 8 | CSET | Works with Rset to establish oscillator free running frequency. Place cap from this Input pin to ground. Can synchronize oscillator by overdriving this pin with an external frequency source. |
| 9 | RSET | Works with Cset to establish oscillator free running frequency. Place resistor from this Input pin to ground. |
| 10 | PWROK | Logical output of UV lockout circuit -- logic "1" indicates chip has valid $V_{CC}$ |
| 11 | VREF | Buffered 3V Output reference voltage |
| 12 | VEE | Logic Ground |
| 13 | NIN | Auxiliary Op-Amp Inverting Input |
| 14 | PIN | Auxiliary Op-Amp Non-Inverting Input |
| 15 | AOUT | Auxiliary Op-Amp Output (Short circuit protected) |
| 16 | ENAUX | Input Enable of Auxiliary Op-Amp (Active Hi) |
| 17 | EN | Logic Input that enables the oscillator and output drivers. Reference voltage remains valid (Active Hi). |
| 18<br>19 | DRVN | Output stage negative rail |
| 20 | OUT B | Totem pole Output B |
| 21 | OUT A | Totem pole Output A |
| 22<br>23 | DRVP | Output stage positive rail |

## SCD5032
High Speed PWM Controller

# PWM5031/5032/5034

## Absolute Maximum Ratings 1/, 4/

### Table 2: Absolute Maximum Ratings

| | |
|---|---|
| Operating Temperature Range | -55°C to +125°C |
| Maximum Junction Temperature | -135°C |
| Storage Temperature Range | -65°C to +150°C |
| $V_{CC}$ Supply Voltage | $7.0V_{DC}$ |
| DVRP Supply Voltage      PWM5031 <br> PWM5032 | $7.0V_{DC}$ <br> $14.0V_{DC}$ |
| Steady State Output Current | ±50mA |
| Peak Output Current (Internally Limited) | ±1.0A |
| Analog Inputs (Pins 5, 6, 13, 14) | $V_{EE} - 0.5V$ to $V_{CC} + 0.5V$ |
| Power Dissipation at $T_A$ = +25°C | 500mW |
| ESD Rating 2/ | 450V |
| Lead Temperature (soldering, 10 seconds) | 300°C |
| Digital Inputs | -0.5V to $V_{CC} + 0.5V$ |

**Note:**
Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

## Operating Conditions 1/, 4/

### Table 3: Operating Conditions

| Parameter | | Condition | Symbol | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| DC Operating Voltage | | - | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Quiescent Current    PWM5031 <br> PWM5032 | | SLEEP @ '0'; EN & ENAUX @ '1': No loads on Outputs PWROK, AOUT and VREF | $I_{CC}$ | - <br> - | - <br> - | 5.8 <br> 7.8 | mA <br> mA |
| Output Drive Voltage    PWM5031 <br> PWM5032 | | - | DRVP | - <br> - | - <br> - | 5.0 <br> 12.0 | V <br> V |
| Output Duty Cycle – Maximum <br>     50% Pin = Logic 0 <br>     50% Pin = Logic 1 | | 100% Duty Cycle <br> 50% Duty Cycle | - <br> - | - <br> 97* <br> - | - <br> - <br> - | - <br> - <br> 50 | % <br> % |
| Thermal Resistance $T_{JC}$ | | - | - | - | - | 6.0 | °C/W |
| Sleep Mode | | - | $I_{CCS}$ | - | - | 20 | µA |

**\*** Dependent on Value of $C_{SET}$ & Operating Frequency

CAES PIONEERING ADVANCED ELECTRONICS

## SCD5032
### High Speed PWM Controller
# PWM5031/5032/5034

## Electrical Characteristics 1/, 4/

4.5 V < $V_{CC}$ < 5.5 V, -55°C < $T_A$ < +125°C, unless otherwise specified, EN = 1, Frequency = 209KHz 6/

### Table 4: DC Electrical Characteristics

| Parameter | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| **Reference Section** | | | | | |
| Pre Rad Reference Voltage | $T_A$ = 25°C, $I_O$ = -1 mA, DRVP = 12V | 2.993 | 3.06 | 3.13 | V |
| Reference Voltage Delta | 50KRad(Si) $T_A$=25°C | - 0.35 | | .49 | % |
| | 100KRad(Si) $T_A$=25°C | - 1.66 | | + 1.18 | |
| | 300KRad(Si) $T_A$=25°C | - 3.39 | | + 2.33 | |
| | 1000KRad(Si) $T_A$=25°C | - 8.83 | | + 6.13 | |
| Line Regulation | - | - | ±.1 | ±.12 | % |
| Load Regulation | $0 \leq I_O \leq 3mA$ 3/ | - | ±.05 | ±.075 | % |
| Thermal Regulation | - | - | ±1 | ±1.6 | % |
| Output Short Circuit | 3/ | - | - | -40 | mA |
| **Oscillator Section** | | | | | |
| Pre Rad Initial Accuracy Range | $T_A$ = 25°C | 197 | 205.5 | 214 | KHz |
| Frequency Range | 3/, 5/ | 20 | - | 1,000 | KHz |
| Frequency Delta | 50KRad(Si) $T_A$=25°C | -1.1 | | +.41 | % |
| | 100KRad(Si) $T_A$=25°C | - 1.46 | | +1.0 | |
| | 300KRad(Si) $T_A$=25°C | - 2.64 | | + 3.11 | |
| | 1000KRad(Si) $T_A$=25°C | - 4.88 | | + 6.21 | |
| Frequency Stability (Part to Part) | 3/ | - | ±2.0 | ±3.8 | % |
| Temperature Stability | $T_{MIN} \leq T_A \leq T_{MAX}$ 3/ | - 2 | | +0.5 | % |
| $R_{SET}$ Range | 3/ | 50 | - | - | KΩ |
| $C_{SET}$ Range | | - | - | 600 | pF |
| **Error Amp Section** | | | | | |
| Input Offset Voltage | 3/ | - 3.3 | - | ±3.3 | mV |
| Input Common Mode Voltage Range | | $V_{EE}$ + 0.2 | - | $V_{CC}$ − 0.2 | V |
| Input Bias Current | | - | - | -1.0 | µA |
| Open Loop Voltage Gain (AVOL) | | 100 | - | - | dB |
| Unity Gain Bandwidth | | 1.0 | 2.0 | - | MHz |
| Power Supply Rejection Ratio (PSRR) | | 60 | - | - | dB |
| Output Sink Current | $V_{FB}$ = 3.0V, $V_{SOFT}$ = 1.1V, 3/ | - | - | +10 | mA |
| Output Source Current | $V_{FB}$ = 2.0V, $V_{SOFT}$ = 5V, 3/ | - | - | -28 | mA |
| $V_{OUT}$ High (Limited by $V_{SOFT}$) | $V_{FB}$ = 2.0V, $R_L$ = 15K to GND | $V_{SOFT}$ - 0.2 | - | - | V |
| $V_{OUT}$ Low | $V_{FB}$ = 3.0V, $R_L$ = 15K to +5V | - | - | $V_{EE}$ + 0.2 | V |
| Gain ($V_{COMP}$/$VI_{SENSE}$) | 3/ | 2.85 | 3 | 3.15 | V/V |
| **Current Sense Section** | | | | | |
| Input Offset Voltage | 3/ | - | - | 3.3 | mV |
| Common Mode Input Voltage | $V_{SOFT}$ = 5V, 3/ 4/ | 0.1 | - | 1.0 | V |
| Input Bias Current | 3/ | - | - | 1.0 | µA |
| $I_{SENSE}$ to Output Delay | | - | 80 | 100 | ns |

## SCD5032
High Speed PWM Controller

# PWM5031/5032/5034

## Electrical Characteristics 1/, 4/ cont.

4.5 V < $V_{CC}$ < 5.5 V, -55°C < $T_A$ < +125°C, unless otherwise specified, EN = 1, Frequency = 209KHz 6/

### Table 4: Electrical Characteristics cont.

| Parameter | Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| **Output Section** | | | | | |
| Output Low Level | $I_{SINK}$ = 1.0mA | - | - | 0.16 | V |
| | $I_{SINK}$ = 50mA PWM5031 | - | - | 0.25 | V |
| | $I_{SINK}$ = 50mA PWM5032 | - | - | 0.63 | V |
| Output High Level-PWM5031 | $I_{SOURCE}$ = 1.0mA, DRVP = 5V | 4.9 | - | - | V |
| | $I_{SOURCE}$ = 50mA, DRVP = 5V | 4.6 | - | - | V |
| Output High Level-PWM5032 | $I_{SOURCE}$ = 1.0mA, DRVP = 12V | 11. 8 | - | - | V |
| | $I_{SOURCE}$ = 50mA, DRVP = 12V | 11. 2 | - | - | V |
| Peak Output Current | 3/ | ±1.0 | ±1.35 | - | A |
| Steady State Output Current | - | - | - | 50 | mA |
| Rise Time | $T_A$ = 25°C, $C_L$ = 20pF, DRVP = 5V 3/ | - | 8 | 18 | ns |
| Fall Time | | - | 6 | 28 | ns |
| Enable Output Off Delay | 3/ | - | - | 100 | ns |
| Sleep Output Off Delay | | - | - | 100 | ns |
| Under Voltage Output Off Delay | | - | - | 100 | ns |
| **Auxiliary Amp Section** | | | | | |
| Input Offset Voltage | - | -3.5 | - | +3.5 | mV |
| Input Common Mode Voltage Range | Off $V_{EE}$ or $V_{CC}$ Rail, 3/ | $V_{EE}$ + 0.2 | - | $V_{CC}$ − 0.2 | V |
| Input Bias Current | 3/ | - | - | 1.0 | µA |
| AVOL | f = 40KHz, 2V < $V_O$ < 4V, 3/ | 100 | - | - | Db |
| Unity Gain Bandwidth | 3/ | 1.0 | - | - | MHz |
| PSRR | 4.5V < $V_{CC}$ < 5.5V, 3/ | 60 | 70 | - | dB |
| Output Sink Current | $V_{PIN}$ < $V_{NIN}$, ENAUX = Hi, 3/ | - | - | +45 | mA |
| Output Source Current | | - | - | -28 | mA |
| $V_{OUT}$ High | $V_{PIN}$ > $V_{NIN}$, ENAUX = Hi, IO = 2mA | $V_{CC}$ - 0.32 | - | - | V |
| $V_{OUT}$ Low | | - | - | $V_{EE}$ + 0.2 | V |
| **Under-Voltage Lockout Section** | | | | | |
| Start Threshold | - | 3.60 | 4.1 | 4.60 | V |
| Operating Voltage After Turn On | - | 3.10 | 3.5 | 4.0 | V |
| **Digital Inputs** | | | | | |
| $V_{IL}$ | Logic Low, 3/ | - | - | 0.8 | V |
| $V_{IH}$ | Logic High, 3/ | 2.0 | - | - | V |
| Leakage Current - $I_{IN}$ | 3/ | - | - | 100 | nA |
| Digital Output (PWROK) | | | | | |
| $V_{OL}$ | Logic low at 1.6mA | - | - | $V_{EE}$ + 0.3 | V |
| $V_{OH}$ | Logic high at -1.6mA | $V_{CC}$ - 0.6 | - | - | V |

## SCD5032
High Speed PWM Controller
# PWM5031/5032/5034

**Notes:**
1) All voltages are with respect to Pin 12. All currents are positive into the specified terminal.
2) Meets ESD testing per MIL-STD-883, method 3015, Class 1A.
3) Parameters are guaranteed by design, not tested.
4) All electrical characterizations for the PWM5034 are the same as the PWM5032.
5) Due to minimum duty cycle limitations the max Functional Operating Frequency is dependent on dynamic range requirements. The recommended max operating frequency is 400KHz.
6) Unless otherwise specified all limits are post 1MRad(Si).

## Detailed Component Operation and Performance

### Power Supplies
1) Four I/O pins are used to supply power to the chip: Two pins for DRVP (referenced to DRVN) and two pins for $V_{CC}$ (referenced to $V_{EE}$)
2) $V_{CC}$ & DRVP can be powered up in any sequence without damage to the chip.
   a. If $V_{CC}$ is applied first, the output will float until the DRVP voltage is applied.
      i. If the application requires the outputs to be off during power-up conditions, the VCC must be turned on before DRVP.
   b. If DRVP is applied before the VCC, the output will go to the potential on DRVP.
3) For protection against inadvertent over / undervoltages, the chip's input pins are diode clamped to the supply rails through current limiting resistors.

### Undervoltage Lockout

The chip includes an internal undervoltage lockout circuit with built in hysteresis and a logic level power good indicator. The positive and negative going thresholds are nominally 4.1V and 3.5V, respectively. If $V_{CC}$ is below this range, the oscillator, error amplifier, main comparators, and output drive circuits are all disabled. The power OK indicator is active high (logic "1") when a valid supply voltage is applied.
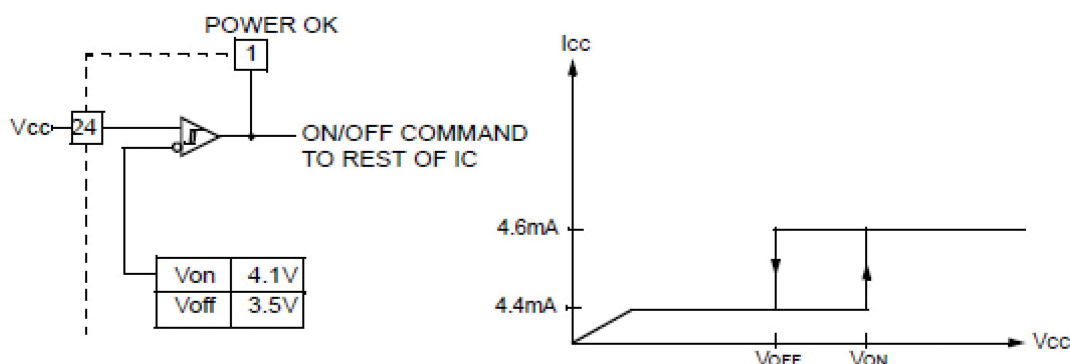


Figure 2: Undervoltage Lockout

### Shutdown Logic

The chip has two logic level inputs for implementing shutdown functions. Asserting a logic "1" on the SLEEP pin disables all chip functions and puts the chip into a very low power consumption mode. Asserting a logic "0" on the EN pin shuts down all functions except the reference, bias generators, and auxiliary amplifier.

# SCD5032
High Speed PWM Controller
# PWM5031/5032/5034

**Table 5: Truth Table**

| Input | | | Output | | | | |
|---|---|---|---|---|---|---|---|
| Sleep | EN | ENAUX | OUTA&B | AOUT | COMP | PWROK | Vref |
| 0 | 0 | 0 | 0 | 0 | 0 | Active | 3 $V_{DC}$ |
| 0 | 0 | 1 | 0 | Active | 0 | Active | 3 $V_{DC}$ |
| 0 | 1 | 0 | Active | 0 | Active | Active | 3 $V_{DC}$ |
| 0 | 1 | 1 | Active | Active | Active | Active | 3 $V_{DC}$ |
| 1 | X | X | 0 | 0 | 0 | 0 | 0 |

X = Not Applicable

## Oscillator

The chip uses two precision current mirrors that alternately charge and discharge an external capacitor to generate an extremely linear sawtooth oscillator waveform. At the start of each cycle, the charging current, set by the choice of resistor at the Rset pin, is 1:1 mirrored over to the Cset pin where it charges an external capacitor. When the capacitor voltage reaches the comparator's upper threshold (nominally VREF), the comparator switches current mirrors and begins to discharge the external capacitor. The discharge current is set at roughly five times the charging current to result in fast discharge and minimal Dead Time. When the voltage reaches the comparator's lower threshold (0.9V), the comparator switches back to the charging mirror, powers down the discharge mirror, and the whole process repeats. The frequency is set by choosing Rset and Cset such that:

$$Fosc = \frac{1}{Charge\ Time + Dead\ Time} = \frac{1}{(.7 \times R_{SET} \times (C_{SET} + 16_{PF})) + (5250 \times (C_{SET} + 12_{PF}))}$$

$$20KHz \leq F_{OSC} \leq 1MHz$$

Suggested Ranges for Cset and Rset are:
20K ohms < Rset < 300K
10pf < Cset < 600pF

Rset 9
Cset 8
GND 12
Ct
Rt
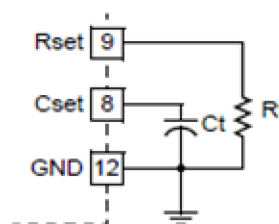
## SCD5032
High Speed PWM Controller
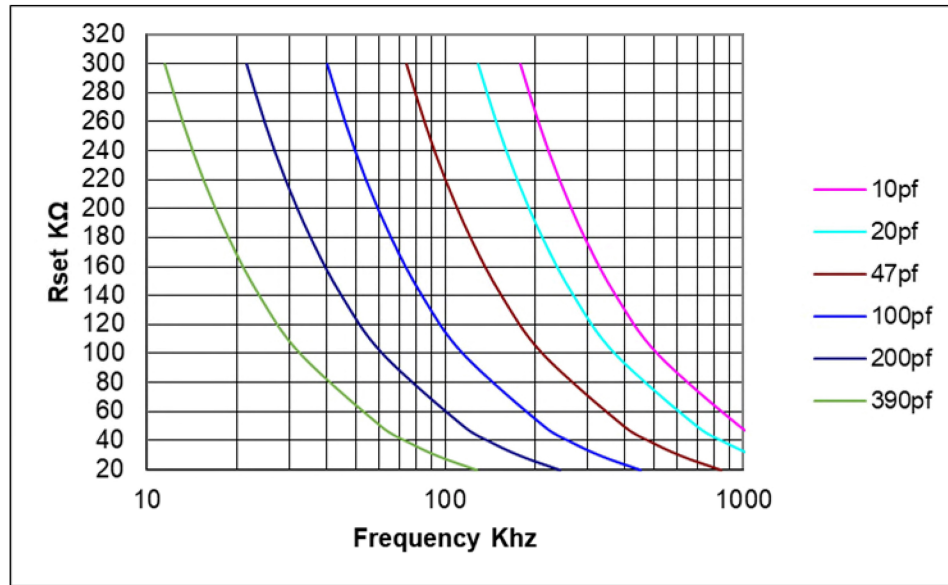# PWM5031/5032/5034



Figure 3: Timing Resistance vs Frequency

### Dead Time

The amount of dead time determines the maximum duty cycle that can be achieved. The Dead Time and the frequency of operation will determine the duty cycle.

$$Dead\ Time = 5250\,(C_{set} + 12pF) \qquad Duty\ Cycle = 1 - \left(\frac{Dead\ Time}{1/F_{OSC}}\right)$$

### Selecting $R_{SET}$ and $C_{SET}$

To select values for RSET and CSET perform the following steps to insure the smallest Dead Time.
1) Determine what frequency is required for your design.
2) Use Figure 4 to select a capacitor value for Cset that will provide the highest duty cycle (shortest Dead Time) at the frequency required.
3) Calculate the value of Rset using the formula:

$$R_{SET} = \frac{(1/F_{OSC}) - (5250 \times (C_{SET} + 12PF))}{.7 \times (C_{SET} + 16PF)}$$

Note small values of Rset increase power consumption for the PWM5032 and small values of Cset may make PCB and stray capacitance a source of error.

**CAES** PIONEERING ADVANCED ELECTRONICS

35 South Service Road | Plainview, NY 11803-0622 | 88379 | 1-800-843-1553 | cobhamaes.com
**APPROVED FOR PUBLIC RELEASE**

# SCD5032
High Speed PWM Controller
# PWM5031/5032/5034
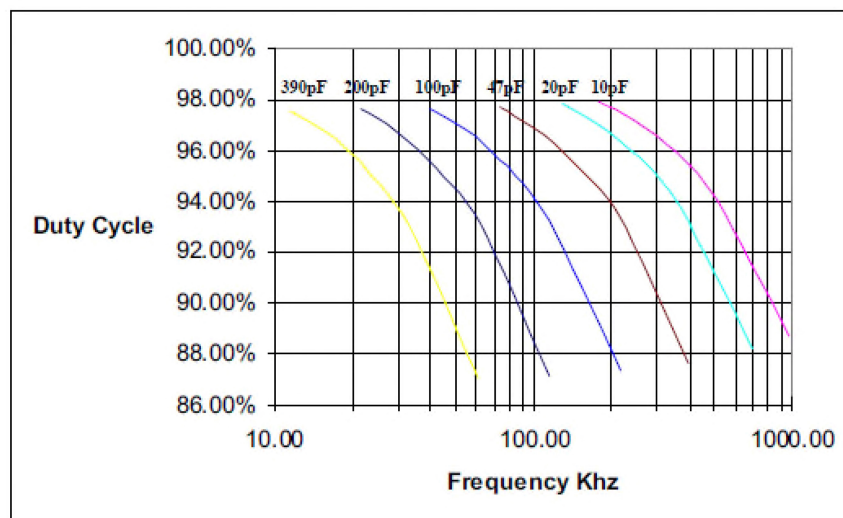


Figure 4: Duty Cycle vs Frequency

If desired, the user can synchronize the oscillator to an external frequency source by coupling a pulse train to the Cset pin:
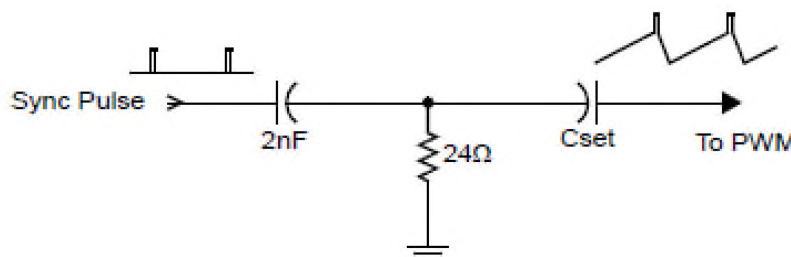


Figure 5: PWM can be synchronized to external source with just two additional components.

Operation is similar to the free running case. Cset is alternately charged and discharged by the same current mirrors and the same comparator and thresholds are used. The only difference is that when a sync pulse is received, the capacitor voltage is level shifted up and reaches the comparator's upper threshold voltage *before it normally would in the free running case*. If a series of pulses are received with shorter period than that of the free running oscillator, the comparator will trip in response to the sync pulse and the oscillator will be synchronized. *(NOTE: The user must ensure that the sync pulse does not induce a voltage on CSET that exceeds the PWM5032 voltage rating. If this cannot be guaranteed, a simple diode clamp to the positive rail should be used to prevent damage to the PWM)*

## Error Amplifier

The main error amplifier is a N-type input folded cascade configuration with a few interesting additions. The positive input is internally tied to 2.5V derived from the on chip reference. The negative input typically draws less than 1µA and has a voltage offset of less than 2mV. At 20µA bias current, the amplifier exceeds 2MHz bandwidth and 120dB open loop gain (see Figure 7).
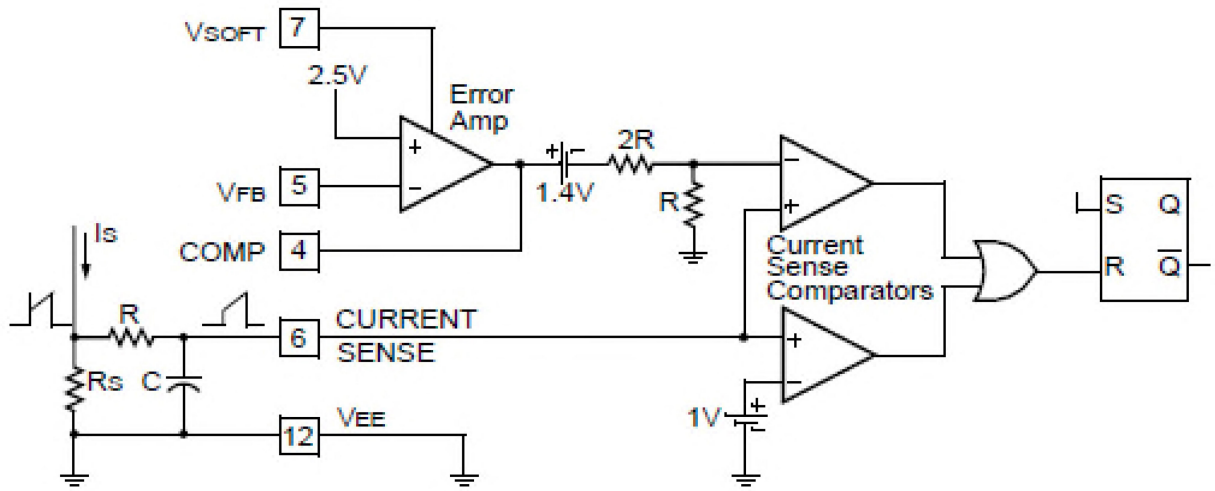
The amplifier is designed to limit at whatever voltage is applied to the SOFT pin. As mentioned previously, this function will allow the user to implement a softstart circuit, a controlled turn-on delay, or any number of other useful functions.

Peak Current (Is) is determined by the formula:

$$I_S MAX = \frac{1.0V}{R_S} \quad \text{or if } V_{R_S} < 1Volt \text{ then } I_S MAX = \frac{V_{SOFT} - 1.4}{3R_S}$$

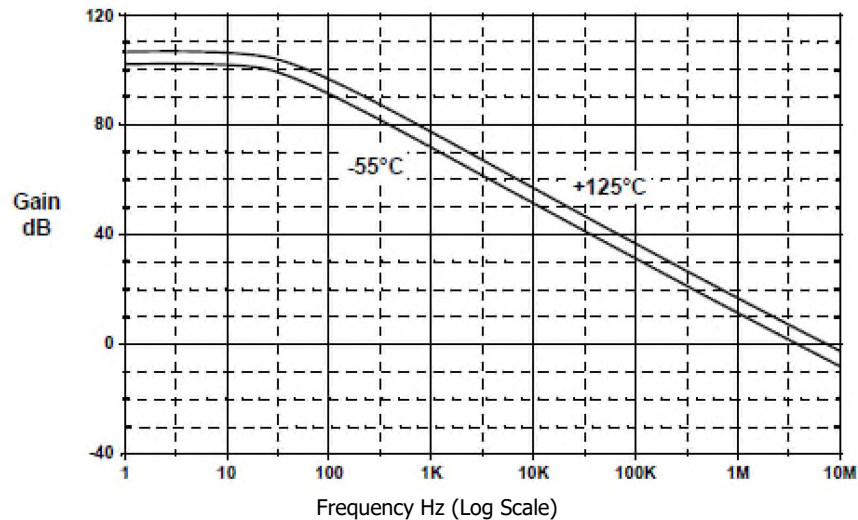A small RC filter may be required to suppress switch transients



Figure 6: Error Amplifier Open-Loop Frequency Response at +125°C & -55°C

## Output Drive

Dual push-pull outputs OutA and OutB are provided for driving off chip switches. The output stages are identical:

- u Totem Pole configuration
- u Break-before-make switching to prevent harmful cross-conduction spikes
- u Separate positive and negative supply connections to decouple power stage and sensitive logic
- u Near rail-to-rail voltage swing
- u ±1A maximum peak current capability (capacitive load)

## SCD5032

High Speed PWM Controller

# PWM5031/5032/5034

The outputs have two modes of control depending on whether the 50% toggle option is selected. In the case where the 50% pin is logic low, the outputs are in-phase with each other and the duty cycle is free to take on any value up to 100%. However, when the 50% pin is asserted high (logic "1"), the outputs become limited to a maximum 50% duty cycle by turning off each output on every other clock period of the oscillator. In addition Output A and Output B will never turn on during the same clock cycle, see Figure 7A below. This would lend itself to a two phase switching system that would be 180° out of phase.
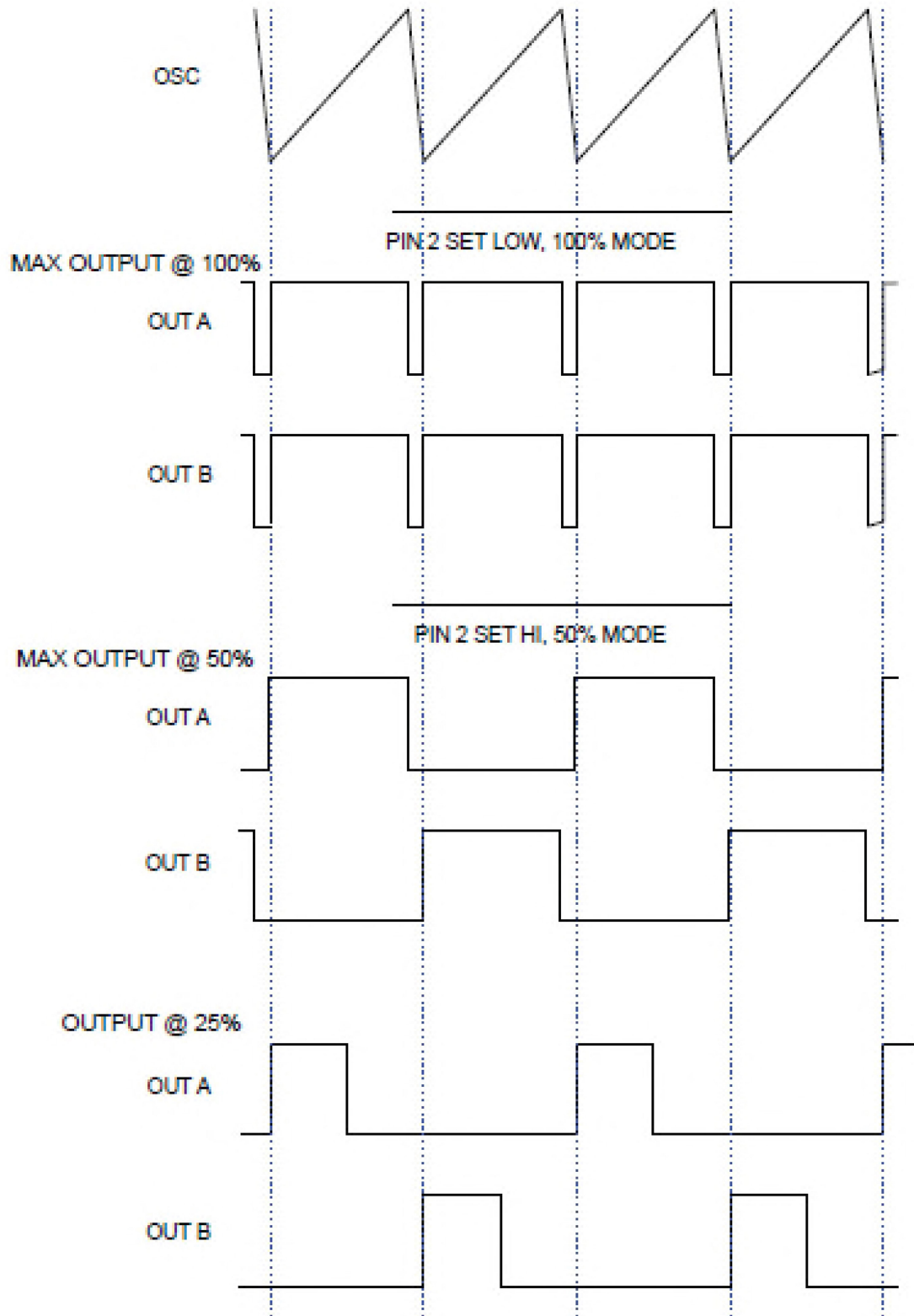
Figure 7: Output Drive Options

# SCD5032
High Speed PWM Controller
# PWM5031/5032/5034
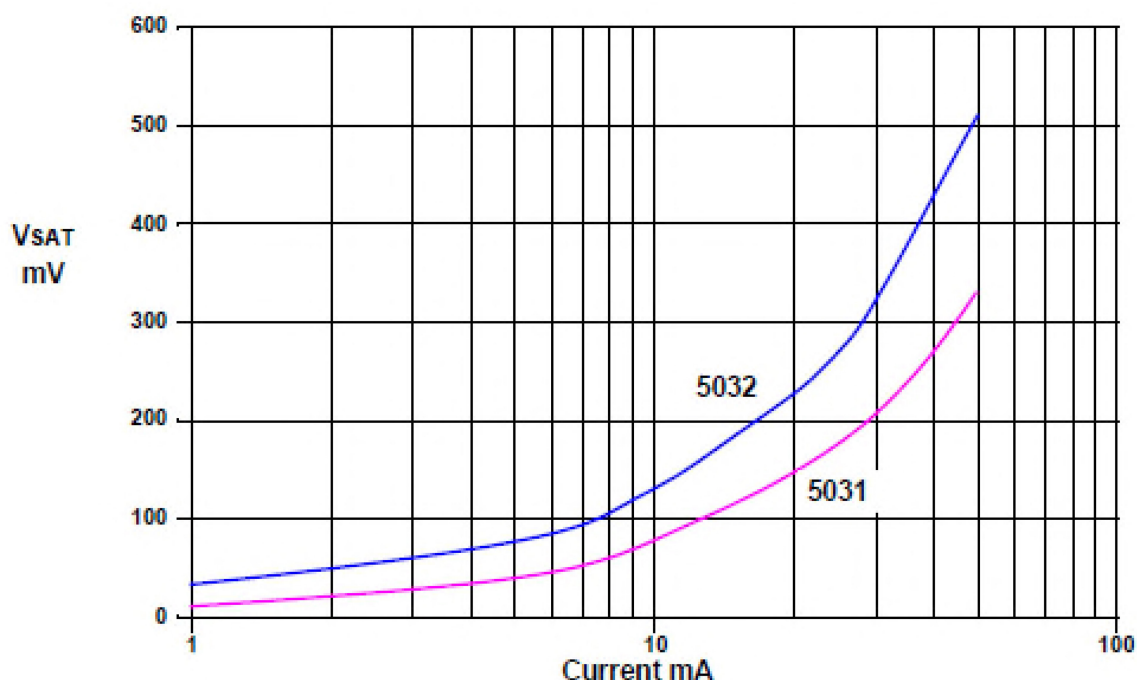


Figure 8: Output Sink and Source Saturation Characteristics at +25°C

**Auxiliary Amplifier**

The chip includes an uncommitted op-amp with independent shutdown feature for use in any user-defined application. Some possibilities are:

u Signal conditioning of an isolated configuration feedback voltage
u Implementation of more sophisticated compensation networks for control loop optimization

The Auxiliary amplifier has a unity gain bandwidth greater than 1MHz and an open loop gain greater than 100dB. The ENAUX pin is active high such that a logic "1" enables the amplifier and logic "0" disables it. The amplifier has near rail-to-rail capability on both the input and output.

A typical single output forward converter application is shown in Figure 9 to aid in the following operational description.

During normal operation, the oscillator jumpstarts each switching cycle by resetting the RS latch, causing the output stage to go high and turn on M1. Current begins to build linearly through T1 and M1 and a proportional voltage is developed across the small sense resistor Rs. Switching spikes are filtered by C1 and R1, and the resulting sawtooth waveform is passed into the PWM to serve as the current comparator input. Meanwhile, a portion of the output voltage is sensed and compared to the PWM's internal precision 2.5V reference. The difference is then amplified and level shifted to serve as the comparator threshold. When the voltage on the ISENSE pin exceeds this threshold, the comparator fires and resets the latch. The output then turns off until the beginning of the next oscillator cycle when the process repeats.

# SCD5032

High Speed PWM Controller
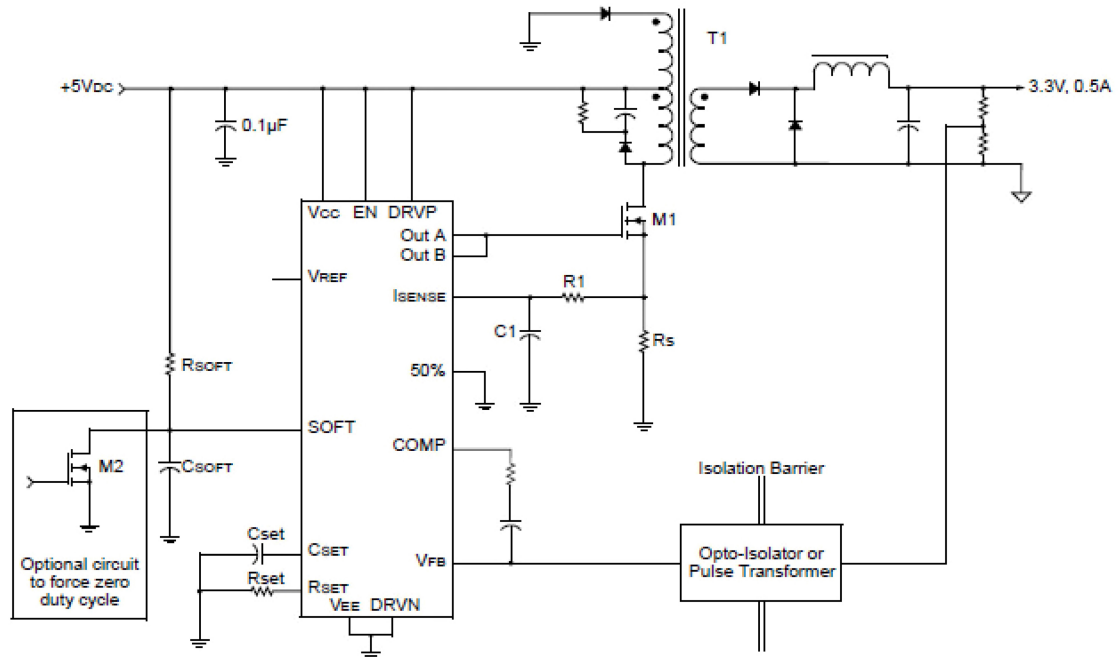
# PWM5031/5032/5034

## Typical Applications



Figure 9: Typical Forward Converter Application

Like all current mode PWMs, the chip provides built in fault protection by limiting peak switch current on a cycle by cycle basis. When an overload condition occurs, the sensed current reaches the current trip threshold earlier in the switching cycle than it otherwise would and thus forces the PWM latch off until the start of the next cycle. The process repeats until the overload condition is removed and the PWM can return to a normal duty cycle. The chip is capable of operating in this mode indefinitely without sustaining damage.

There are two ways to set the current limit trip point. One is to simply tailor the sense resistor Rs:

$$I_{pk} = \frac{1.0 Vdc}{R_S}$$

Some users may find the power is dissipated in Rs to be unacceptably high. In this case, the user can fix Rs at a small value and vary the current comparator threshold instead. Fortunately, the PWM chip provides a very convenient method for doing so. Because the error amplifier output is internally clamped to the SOFT pin, the user need simply apply the desired voltage level to the SOFT pin to arbitrarily lower the current comparator threshold.

Recalling that the EA output is level shifted and divided before being applied to the comparator input, the peak current limit is chosen by applying a voltage VSOFT such that:

$$I_{pk} = \frac{V_{soft} - 1.4}{3 \times R_S} \qquad\qquad 1.4V \leq V_{soft} \leq 4.4V$$

Clamping the EA output to the soft pin also makes implementing a softstart ciruit easy. Rsoft and Csoft are connected as in Figure 9 to provide the SOFT pin an asymptotically rising voltage. Because of the internal clamp on the EA output, the PWM duty cycle will increase only as fast as the chosen time constant will allow. In this way, excessive duty cycle and surge currents into the output capacitors are avoided. A transistor may be optionally connected across the soft start capacitor to force zero duty cycle on command. This is a particularly convenient method for implementing an externally controlled turn-on delay.

## SCD5032
High Speed PWM Controller
# PWM5031/5032/5034

The discussion so far assumes the user operates the chip in the current mode: switch current is sensed and compared to the error between the output voltage and a precision reference. Alternatively, the user may wish to implement voltage mode control in which the control loop is dependent only on the output voltage. The PWM chip readily supports this configuration with the following modification:
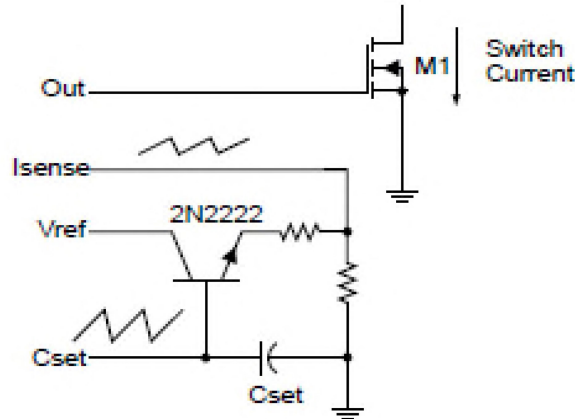


Figure 10: Circuit for implementing voltage mode control.

A portion of the oscillator's sawtooth waveform is coupled to the ISENSE pin and becomes the input to the comparator stage. The operation is now identical to the current mode application: when the sawtooth voltage exceeds the amplified difference between the output and a voltage reference, the comparator fires and latches off the output until the start of the next cycle.

### Selected Application Examples

The flexibility and performance of the chip makes it suitable for an enormous range of power converter applications – step-up, step-down, DC-DC, AC-DC, isolated/non-isolated, and many more. This section will cover two of the more popular power converter applications for which this chip is particularly well suited although many more can be envisioned.

### 5v Input, 3.3v Isolated Output (Single Ended Forward Converter)

The isolated step down DC/DC converter is a staple of many satellite and aerospace systems. A common bus distributes raw primary power to various system loads which must then convert the primary to one or more low voltage secondary outputs. These outputs are filtered, regulated, and ground isolated from the primary side to keep EMI and undesired subsystem interaction at a minimum. Figure 9 is one example of a circuit that very efficiently performs this conversion. The values here were chosen to work for a 5V input and 3.3V output but the circuit topology is general enough to support an infinite variety of applications. For example, output voltages can be adjusted by changing values of just a few components. A wider input voltage range can be supported by varying the transformer's turns ratios and by proper selection of M1. Thus, a very wide range of power converter applications can be satisfied by simple variations of the circuit.

At the start of each switching cycle, the PWM output goes high and turns on M1. Energy is coupled across T1's turns ratios to the secondary side where it is caught, rectified, and filtered to produce a clean DC voltage. A sampling network on the output side feeds back a portion of the output across the isolation barrier into the error amplifier negative input. This feedback can be accomplished in a number of different ways: pulse transformers, optocouplers, or capacitive coupling are a few methods. The compensation network may need modification depending on the feedback method chosen. The additional winding and rectifier on T1 are used to reset the transformer core after the PWM latches off M1 to prevent staircase saturation of the core.

## SCD5032

High Speed PWM Controller

# PWM5031/5032/5034

Note the chip is powered directly from the main power bus (via a zener and current limit resistor) without the need for additional bootstrap transformer windings. This is one of the main advantages this PWM chip provides over other products. This scheme could not be implemented with other chips which draw significantly more current. On the other hand, supplying bias to our PWM chip is about as simple as it gets.

### 5V to 1.8V Buck Converter

A second application is a secondary side, non-isolated buck converter. The circuit takes a high voltage (5V in this case) and steps down to a lower voltage (5V to 1.8V in this example, although as pointed out above, these values are completely adjustable with proper component selection). If the output voltage is less than 2.5V the auxiliary amplifier can be used to provide the gain necessary to get $V_{FB}$ back up to 2.5V.
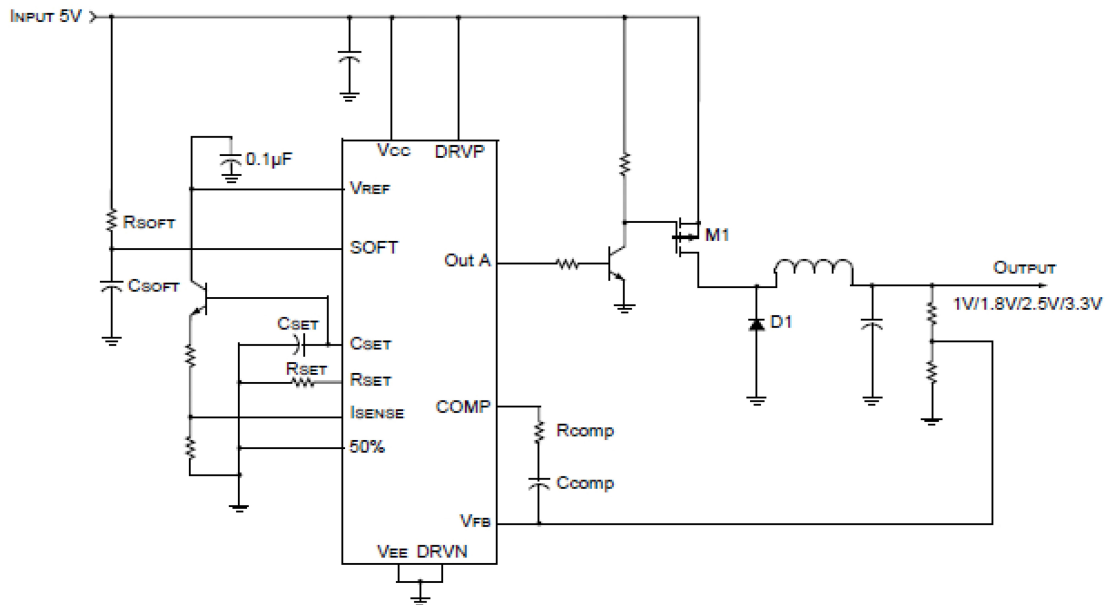


Figure 11: Buck Converter

The circuit switches M1 twice per cycle, chopping the $5V_{DC}$ input into a fixed frequency pulse train whose DC average is the desired output voltage. The LC filter then simply smoothes this pulse train to produce a clean DC output. The control loop regulates against operating point perturbations (temperature, line, load) by adjusting M1's duty cycle. The circuit is operated in the voltage mode since switch current is not referenced to circuit ground. Alternatively, a current transformer may be used to properly reference the $I_{SENSE}$ signal to permit current mode control. An inverter is needed in the output path to properly drive the P-channel MOSFET. For low current applications (less than -50mA output current), it may be possible to use the PWM's output drive stage as the switching elements and eliminate M1 and D1 altogether.
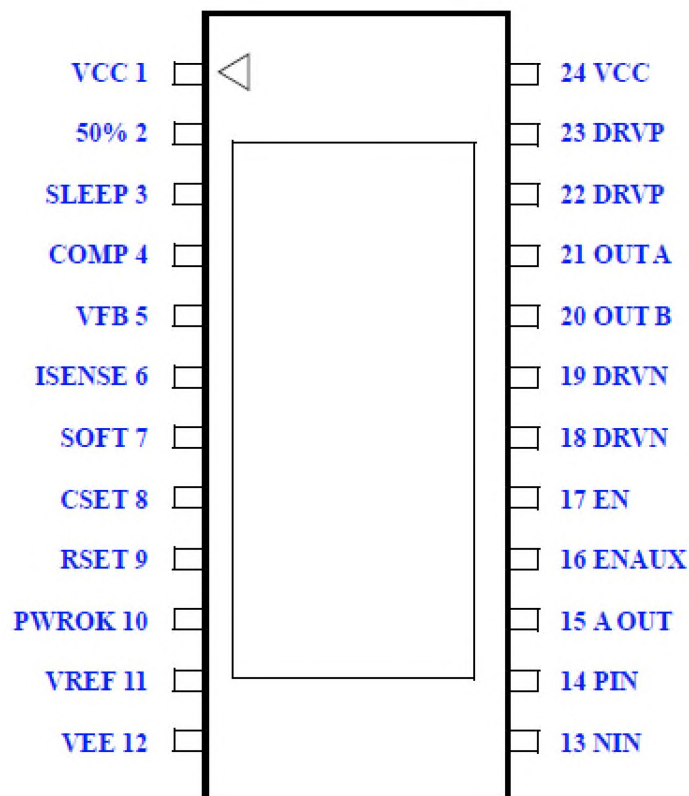
# SCD5032
High Speed PWM Controller
# PWM5031/5032/5034



Figure 12: Package Pin vs Function
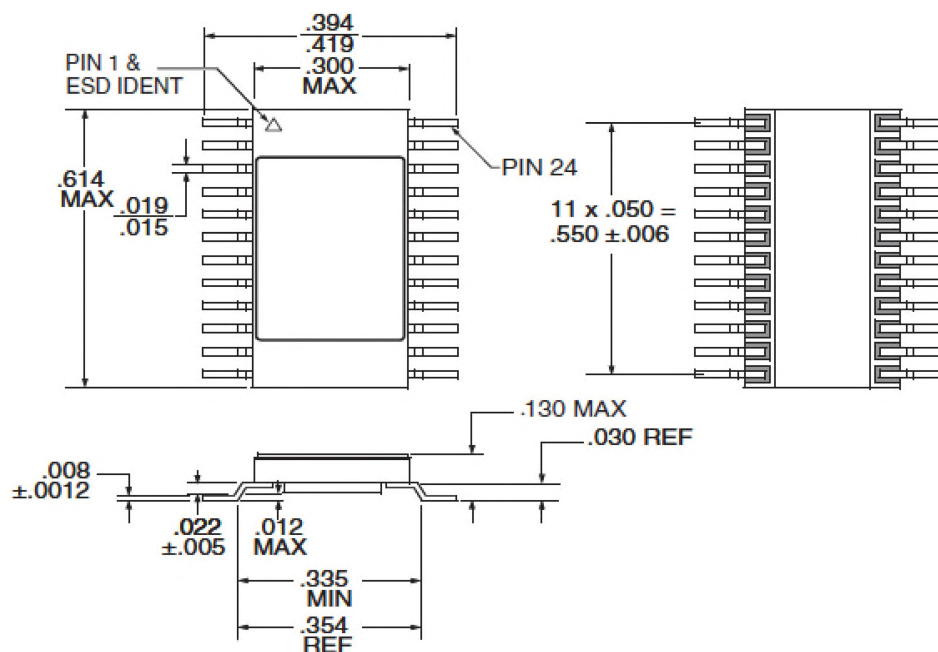
**Note**: The Lid is connected to pin 12



Figure 13: PWM5031 /PWM5032 Flat Package (Gull Wing) Configuration Outline
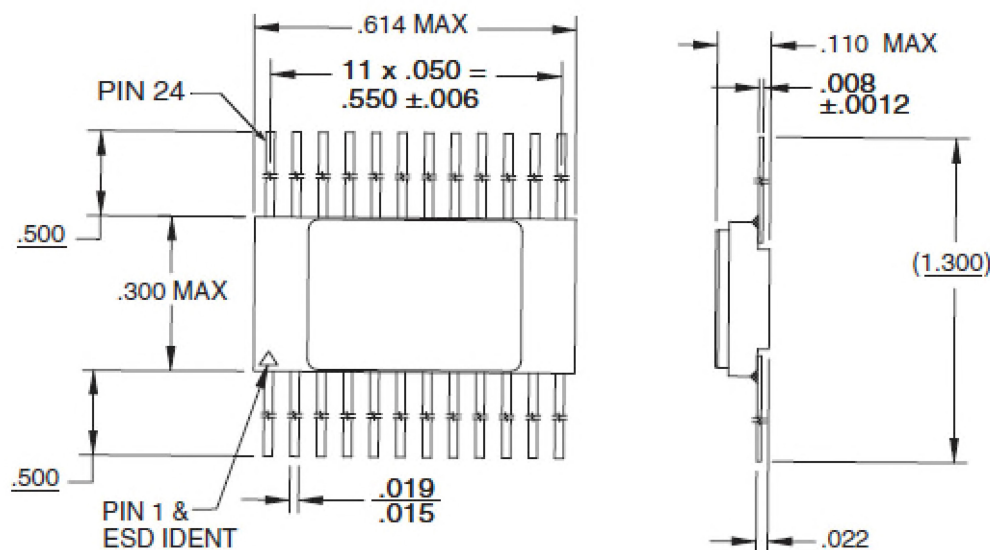
# SCD5032
High Speed PWM Controller

# PWM5031/5032/5034



Figure 14: PWM5034 Flat Package (Straight Leads) Configuration Outline

## Ordering Information
### Figure 15: Ordering Information

| Model | DLA SMD # | Screening | Package |
|---|---|---|---|
| PWM5032-7 | | Commercial Flow, +25°C testing only | Flat Package Gull Wing |
| PWM5032-S | - | Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications | |
| PWM5032- 001-1S | 5962-0625102KXC | In accordance with DLA SMD | |
| PWM5032- 001-2S | 5962-0625102KXA | | |
| PWM5034-7 | | Commercial Flow, +25°C testing only | Flat Package Straight Lead |
| PWM5034-S | - | Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications | |
| PWM5034- 001-1S | 5962-0625102KYC | In accordance with DLA SMD | |
| PWM5032-EVAL | - | See Application note AN5031-1 1/ | 8" x 11" x 3.25"ht |

## Revision History
### Table 6: Revision History

| Date | Rev. # | Change Description | Initials |
|---|---|---|---|
| 04/xx/2019 | H | Add ELDRS Feature, Change Voltage Ref and Initial Accuracy to Pre Rad levels, Add Ref Delta and Frequency Delta percentages, Change Figure 3 to incorporate 20kHz range, Update limits for $I_{CC}$, Output H/L levels, Undervoltage Lockout, add footnotes 5 and 6, change Table 16 to 6. | CL |
| 03/26/2021 | J | Revised per ECN 23566. | CL |
| 12/22/22 | K | Revised per ECN 24520 | CL |

# SCD5032
## High Speed PWM Controller
# PWM5031/5032/5034

## Datasheet Definitions

| | DEFINITION |
|---|---|
| Advanced Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice.  The product is still in the development stage and the datasheet **is subject to change**.  Specifications can be **TBD** and the part package and pinout are **not final**. |
| Preliminary Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice.  The product is in the characterization stage and prototypes are available. |
| Datasheet | Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes. |

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.:  These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations.  Diversion contrary to U.S. law is prohibited.

**CAES** PIONEERING ADVANCED ELECTRONICS

35 South Service Road | Plainview, NY 11803-0622 | 88379 | 1-800-843-1553 | cobhamaes.com
**APPROVED FOR PUBLIC RELEASE**