

SCD8508

32-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

ACT8508

Features

- 32 Channels provided by two independent 16-channel multiplexers
- Radiation performance
 - Total dose: 300 krads(Si), Dose rate = 50 - 300 rads(Si)/s
 - SEU: Immune up to 120 MeV-cm²/mg
 - SEL: Immune by process design
- Full military temperature range
- Low power consumption <30mW
- Two address busses (A0-3 & B0-3), and two enable lines afford flexible organization
- All channel inputs are protected by ±20V nominal Transorbs
- Fast access time 1500ns typical
- Break-Before-Make switching
- High analog input impedance (power on or off)
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
 - 96 leads, 1.32"Sq x 0.20"Ht quad flat pack
 - Typical Weight 15 grams
- **CAES Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

CAES ACT8508 is a radiation tolerant, 32 channel multiplexer MCM (multi-chip module) with electrostatic discharge (ESD) protection on all channel inputs.

The ACT8508 has been specifically designed to meet exposure to radiation environments. It is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the ACT8508 is ideal for demanding military and space applications.

Organization and Application

The ACT8508 consists of two 16 channel multiplexers arranged as shown in the Block Diagram. The ACT8508 design is inherently radiation tolerant.

A Section

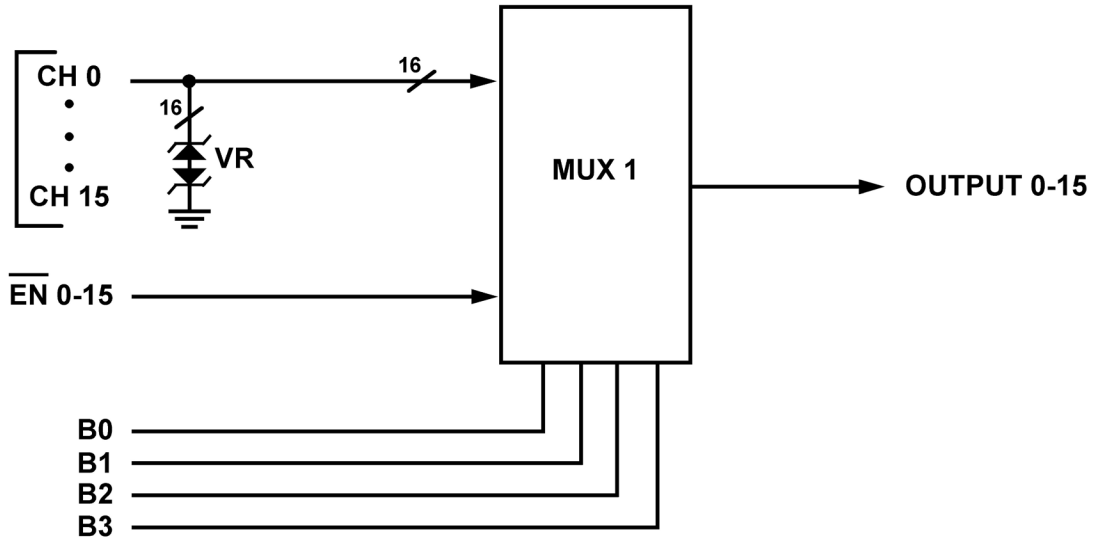
Sixteen (16) channels addressable by bus A₀~A₃, in one 16 channel block including enable.

B Section

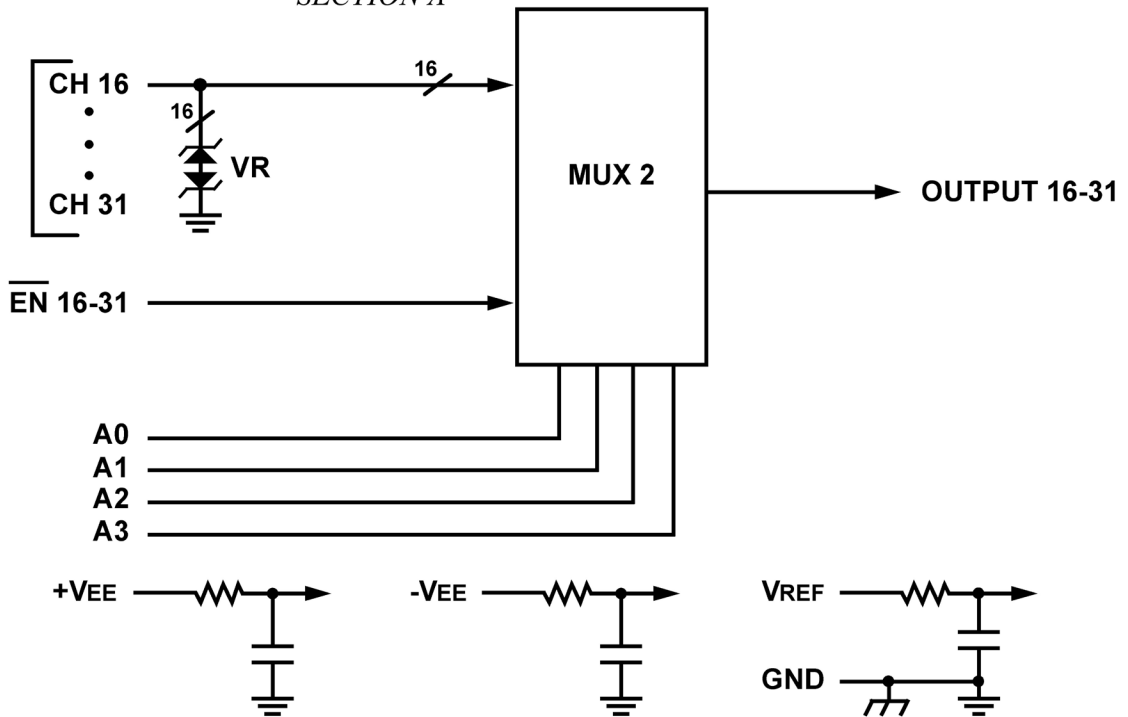
Sixteen (16) channels addressable by bus B₀~B₃, in one 16 channel block including enable.

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SECTION B



SECTION A



ACT8508 32 – Channel Analog Mux Block Diagram

Absolute Maximum Ratings 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Supply Voltage		
+V _{EE} (Pin 44)	+16.5	V
-V _{EE} (Pin 46)	-16.5	V
V _{REF} (Pin 48)	+16.5	V
Digital Input Overvoltage	< V _{REF} +4	V
V _{EN} (Pins 5, 92), V _A (Pins 1, 3, 93, 95), V _B (Pins 2, 4, 94, 96)	> GND -4	V
Analog Input Over Voltage		
V _S	±18V	V

Note:

- 1) All measurements are made with respect to ground.

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions 1/

Symbol	Parameter	Typical	Units
+V _{EE}	+15V Power Supply Voltage	+15.0	V
-V _{EE}	-15V Power Supply Voltage	-15.0	V
V _{REF}	Reference Voltage	+5.00	V
V _{AL}	Logic Low Level	+0.8	V
V _{AH}	Logic High Level	+4.0	V

Note:

- 1) Power Supply turn-on sequence shall be as follows: +V_{EE}, -V_{EE}, followed by V_{REF}.

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DC Electrical Performance Characteristics 1/

(Tc = -55°C To +125°C, +V_{EE} = +15V, -V_{EE} = -15V, V_{REF} = +5.0V -- Unless otherwise specified)

Parameter	Symbol	Conditions	MIN	MAX	Units	
Supply Current	+I _{EE}	V _{EN(0-31)} = V _{A(0-3)A} = V _{A(0-3)B} = 0	0.2	1	mA	
	-I _{EE}	V _{EN(0-31)} = V _{A(0-3)A} = V _{A(0-3)B} = 0	-1	-0.2	mA	
	+I _{SBY}	V _{EN(0-31)} = 4V, V _{A(0-3)A} = V _{A(0-3)B} = 0 <u>6/</u>	0.2	1	mA	
	-I _{SBY}	V _{EN(0-31)} = 4V, V _{A(0-3)A} = V _{A(0-3)B} = 0 <u>6/</u>	-1	-0.2	mA	
Address Input Current	I _{AL(0-3)A}	V _A = 0V <u>7/</u>	-1	1	μA	
	I _{AH(0-3)A}	V _A = 5V <u>7/</u>	-1	1	μA	
	I _{AL(0-3)B}	V _B = 0V <u>7/</u>	-1	1	μA	
	I _{AH(0-3)B}	V _B = 5V <u>7/</u>	-1	1	μA	
Enable Input Current	I _{ENL(0-15)}	V _{EN(0-15)} = 0V <u>7/</u>	-1	1	μA	
	I _{ENH(0-15)}	V _{EN(0-15)} = 5V <u>7/</u>	-1	1	μA	
	I _{ENL(16-31)}	V _{EN(16-31)} = 0V <u>7/</u>	-1	1	μA	
	I _{ENH(16-31)}	V _{EN(16-31)} = 5V <u>7/</u>	-1	1	μA	
Positive Input Leakage Current CH0-CH31	+ISOFFOUTPUT	V _{IN} = +10V, V _{EN} = 4V, output and all unused MUX inputs under test = -10V <u>2/</u> , <u>3/</u> , <u>7/</u>	-100	+700	nA	
Negative Input Leakage Current CH0-CH31	-ISOFFOUTPUT	V _{IN} = -10V, V _{EN} = 4V, output and all unused MUX inputs under test = +10V <u>2/</u> , <u>3/</u> , <u>7/</u>	-100	+700	nA	
Output Leakage Current OUTPUTS (pins 25 & 70)	+IDOFFOUTPUT	V _{OUT} = +10V, V _{EN} = 4V, output and all unused MUX inputs under test = -10V <u>3/</u> , <u>4/</u> , <u>7/</u>	-100	+100	nA	
Output Leakage Current OUTPUTS (pins 25 & 70)	-IDOFFOUTPUT	V _{OUT} = -10V, V _{EN} = 4V, output and all unused MUX inputs under test = +10V <u>3/</u> , <u>4/</u> , <u>7/</u>	-100	+100	nA	
Input Clamped Voltage CH0 – CH31	+V _{CLMP}	V _{EN} = 4V, all unused MUX inputs under test are open. <u>3/</u>	+25°C	18.0	23.0	V
			+125°C	18.0	23.5	V
			-55°C	17.5	22.5	V
Input Clamped Voltage CH0 – CH31	-V _{CLMP}	V _{EN} = 4V, all unused MUX inputs under test are open. <u>3/</u>	+25°C	-23.0	-18.0	V
			+125°C	-23.5	-18.0	V
			-55°C	-22.5	-17.5	V
Switch ON Resistance OUTPUTS (pins 25 & 70)	R _{DS(ON)(0-31)_A}	V _{IN} = +15V, V _{EN} = 0.8V, I _{OUT} = -1mA <u>2/</u> , <u>3/</u> , <u>5/</u>	500	3000	Ω	
	R _{DS(ON)(0-31)_B}	V _{IN} = +5V, V _{EN} = 0.8V, I _{OUT} = -1mA <u>2/</u> , <u>3/</u> , <u>5/</u>	500	3000	Ω	
	R _{DS(ON)(0-31)_C}	V _{IN} = -5V, V _{EN} = 0.8V, I _{OUT} = +1mA <u>2/</u> , <u>3/</u> , <u>5/</u>	500	3000	Ω	

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Notes:

- 1) Measure inputs sequentially. Ground all unused inputs of the device under test. V_A is the applied input voltage to the address lines A(0-3). V_B is the applied input voltage to the address lines B(0-3).
- 2) V_{IN} is the applied input voltage to the input channels CH0-CH31.
- 3) V_{EN} is the applied input voltage to the enable lines En(0-15), En(16-31).
- 4) V_{OUT} is the applied input voltage to the output lines OUTPUT(0-15), OUTPUT(16-31).
- 5) Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX Pin.
- 6) Not tested, guaranteed to the specified limits.
- 7) These parameters for $T_c = -55^\circ\text{C}$ are guaranteed by design, characterization, or correlation to other test parameters but not production tested.

Switching Characteristics

$T_c = -55^\circ\text{C To } +125^\circ\text{C}$, $+V_{EE} = +15\text{V}$, $-V_{EE} = -15\text{V}$, $V_{REF} = +5.0\text{V}$ -- Unless otherwise specified)

Parameter	Symbol	Conditions	MIN	MAX	Units
Switching Test MUX	t_{aHL}	$R_L = 10\text{K}\Omega, C_L = 50\text{pF}$	10	1500	ns
	t_{aLH}	$R_L = 10\text{K}\Omega, C_L = 50\text{pF}$ $T_c = +25^\circ\text{C}, +125^\circ\text{C}$ $T_c = -55^\circ\text{C}$	10 10	2000 5000	ns ns
	t_{ONEN}	$R_L = 1\text{K}\Omega, C_L = 50\text{pF}$	10	1500	ns
	t_{OFFEN}		10	1000	ns

Truth Table (CH0 – CH15)

B3	B2	B1	B0	EN(0-15)	"ON" Channel <u>1</u> /
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT (0-15)

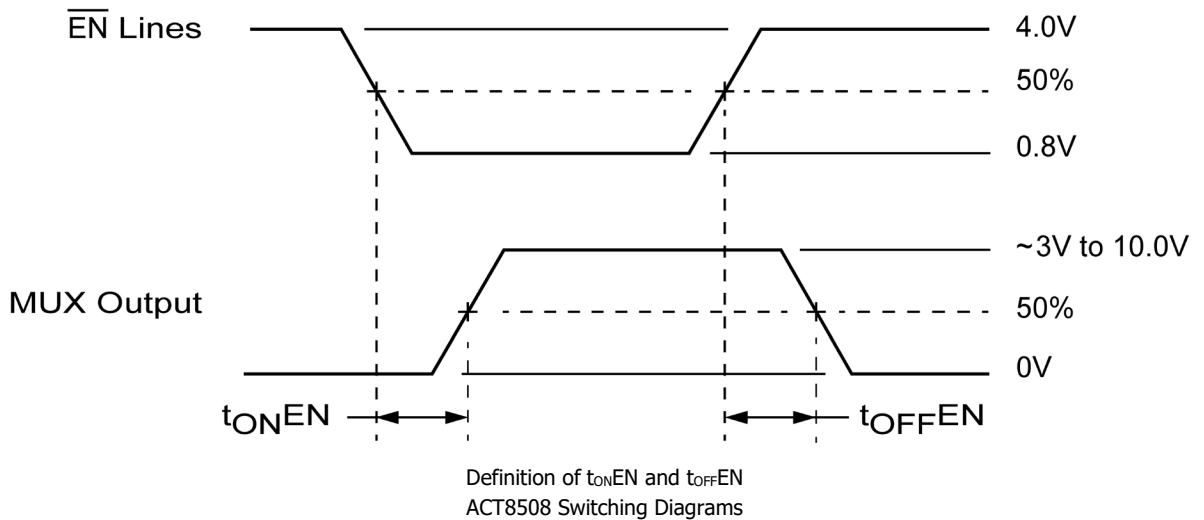
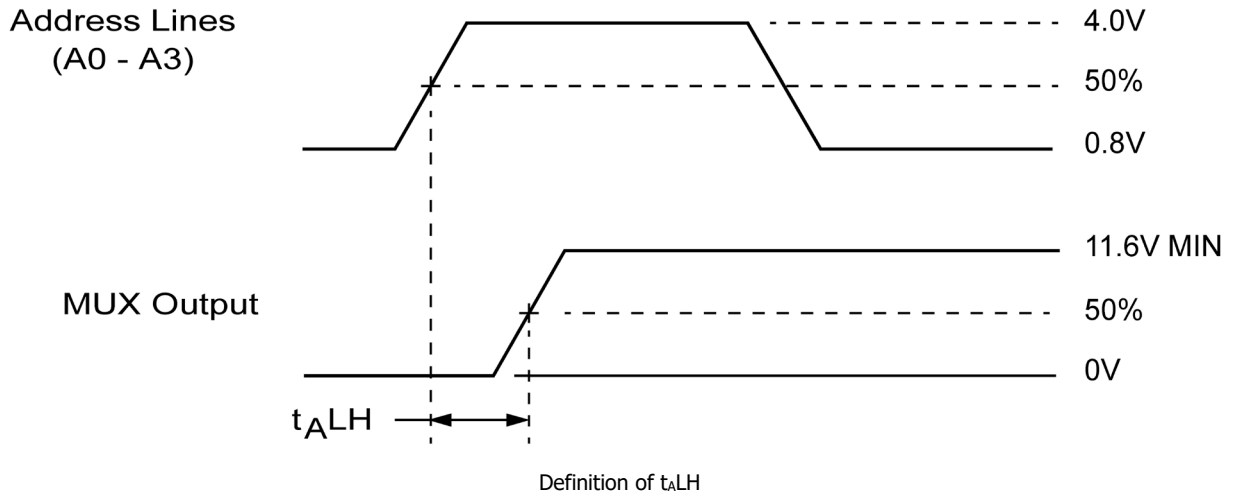
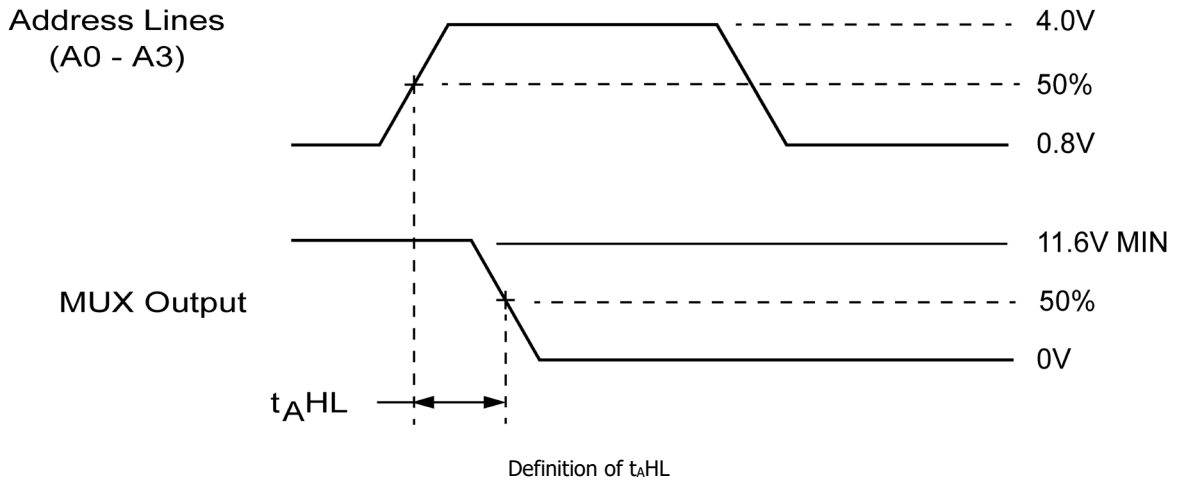
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Truth Table (CH16 – CH31)

A3	A2	A1	A0	EN(16-31)	"ON" Channel <u>1</u> /
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between CH16-31 and OUTPUT (16-31)

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Note: $f = 10\text{kHz}$, Duty cycle = 50%.

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Pin Numbers & Functions

ACT8508 – 96 Leads Ceramic QUAD Flat Pack

Pin #	Function	Pin #	Function	Pin #	Function
1	A2	33	CH11	65	GND
2	B2	34	GND	66	GND
3	A3	35	CH12	67	NC
4	B3	36	GND	68	NC
5	$\overline{\text{EN}}$ 0-15	37	CH13	69	NC
6	NC	38	GND	70	Output V(16-31)
7	CH0	39	CH14	71	GND
8	GND	40	GND	72	GND
9	CH1	41	CH15	73	CH31
10	GND	42	GND	74	CH30
11	CH2	43	NC	75	CH29
12	GND	44	+V _{EE}	76	CH28
13	CH3	45	NC	77	CH27
14	GND	46	-V _{EE}	78	CH26
15	CH4	47	NC	79	CH25
16	GND	48	V _{REF}	80	CH24
17	CH5	49	NC	81	CH23
18	GND	50	CASE GND	82	CH22
19	CH6	51	GND	83	CH21
20	GND	52	GND	84	CH20
21	CH7	53	GND	85	CH19
22	GND	54	GND	86	CH18
23	GND	55	GND	87	CH17
24	GND	56	GND	88	CH16
25	Output V(0-15)	57	GND	89	GND
26	NC	58	GND	90	GND
27	CH8	59	GND	91	NC
28	GND	60	GND	92	$\overline{\text{EN}}$ 16-31
29	CH9	61	GND	93	A0
30	GND	62	GND	94	B0
31	CH10	63	GND	95	A1
32	GND	64	GND	96	B1

Note: It is recommended that all "NC" or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.

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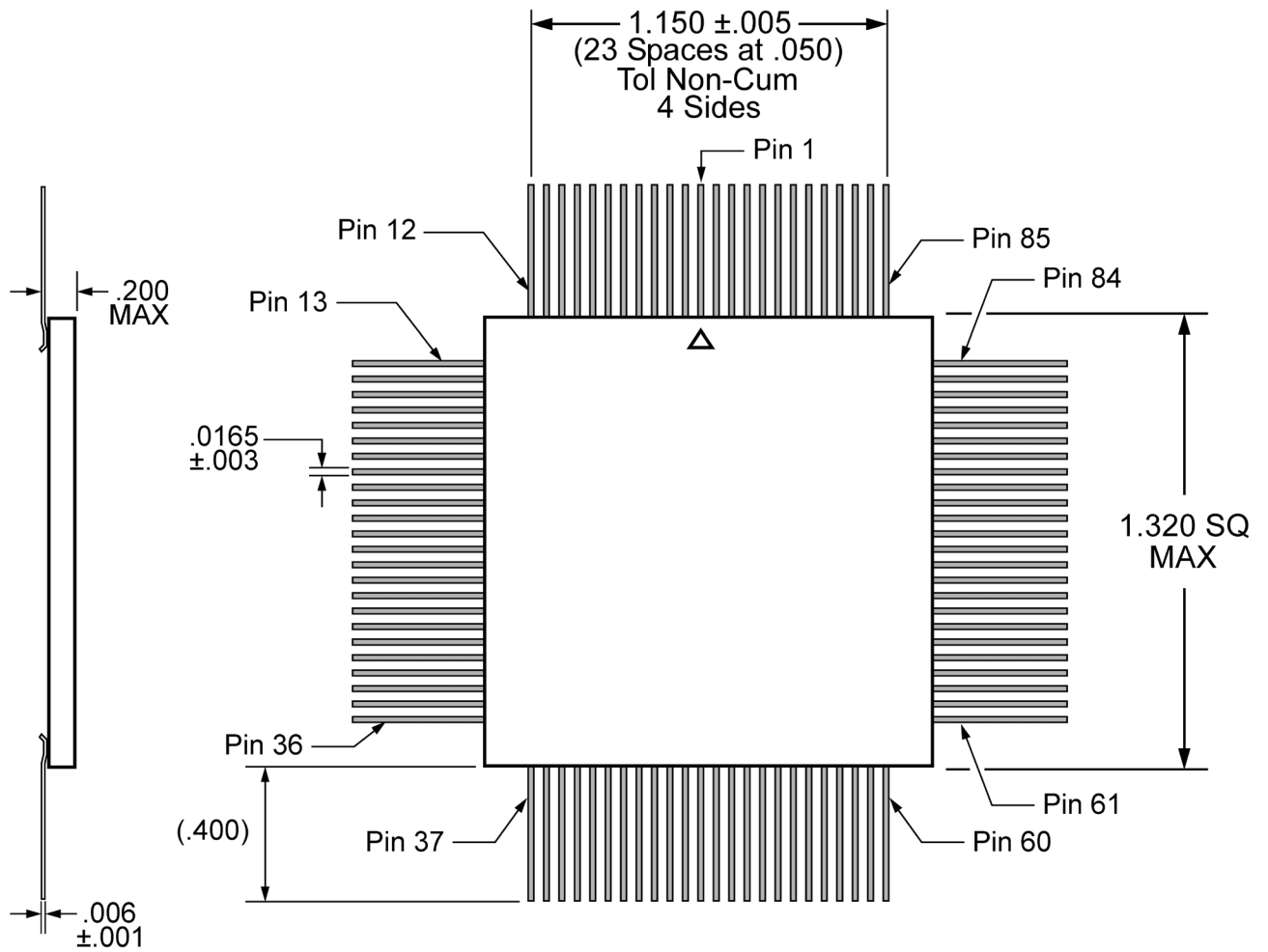
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Ordering Information

Model	DLA SMD #	Screening	Package
ACT8508-7	-	Commercial Flow, +25°C testing only	QUAD Flat Pack
ACT8508-S	5962-0822601KXC	In accordance with DLA SMD	
ACT8508-901-1S	5962F0822601KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "F", 300krad(Si)	

Flat Package Outline



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

REVISION HISTORY

Date	Rev. #	Change Description	Initials
12/8/08	D	REVISED PER ECN 8508-6	KAM
4/15/14	E	REVISED PER ECN 8508-10	KM
3/4/21	F	REVISED PER ECN 23534	

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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