



FRONTGRADE

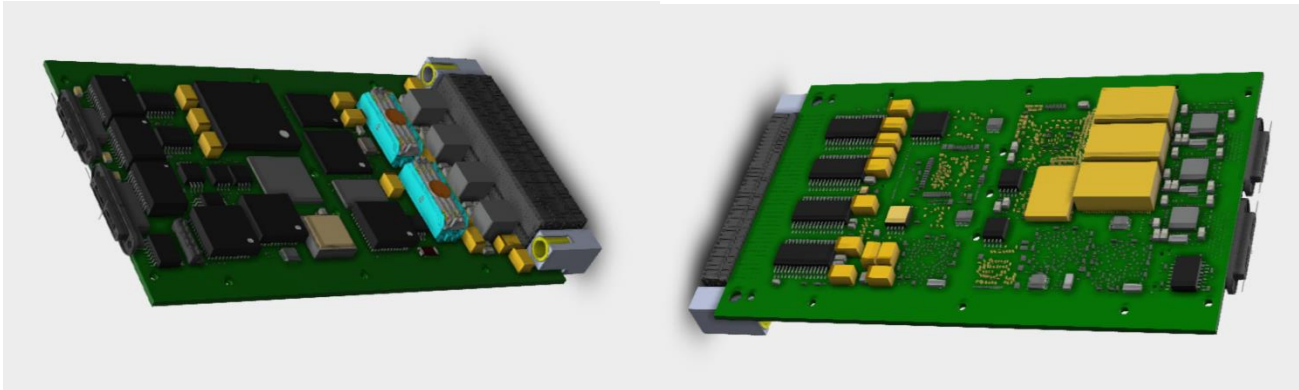
ADVANCED PRODUCT BRIEF

Generation 8 SBC

Generation 8 Single Board Computer

8/23/2024

Version #: 1.3.2



Introduction

The Frontgrade™ SBC8 Single Board Computer is a perfect mix of high-performance processing, interface flexibility, and low power, in a SWaP optimized design that is ideal for your space processing or C&DH needs now and into the future. This compact 3U SpaceVPX design is small, lightweight, and power efficient while offering the processing power and flexibility you need to succeed in today's competitive space markets.

The Frontgrade SBC8 design features the latest Radiation Hardened and field tested Quad Core LEON4FT SPARC V8 processor (GR740) that provides up to 1800 DMIPS of processing power and pairs that with our latest Low Power, High Performance Radiation Tolerant CertusPro-NX-RT FPGA. SBC8 provides 512MB of Reed-Solomon EDAC protected SDRAM directly connected to the GR740 processor along with 256MB Dual-QSPI MRAM - providing directly connected persistent RAM storage to user applications. Additional 512MB-1GB of local expansion persistent-RAM (MRAM) is available via PCI DMA transactions from the GR740 through the Frontgrade CertusPro-NX-RT FPGA. All told, the SBC8 implements a robust memory architecture based on highly reliable, space assured, memories yielding a total of 512MB volatile SDRAM and up to 1.25GB of non-volatile MRAM. SBC8 also optionally includes up to 171GB of EDAC Corrected Non-Volatile User Data Storage.

Additionally, SBC8 features a VITA 88.0 XMC+ Mezzanine interface to allow you to use the same base SBC for all your missions but have the flexibility to add custom mezzanine CCAs to tailor front panel interfaces and processing to each individual mission's requirements. This not only allows for the flexibility you need but allows for reuse of your valuable software code base as you move from mission to mission.

To collect and report telemetry as well as oversee the major components of the design and allow for implementation of additional radiation mitigation and error handling strategies, the SBC8 includes a Radiation Hardened ARM Cortex M0+ based Microcontroller with its own independent boot and application Flash Memory.

Finally, a development "Dongle" is available to access the JTAG resources of the MCU, FPGA, and Processor as well as providing Ethernet or SpW Debug capabilities for your software development team.

Features

Performance

- GR740 Quad Core Radiation Hardened SoC from Industry Leader Frontgrade Gaisler
 - 2MB Level2 cache SDRAM Interface
 - High Speed Processing up to 1800 DMIPS (250MHz system clock @ 1.84DMIPS/MHz/Core)
 - Excellent Fight Heritage and Code Base
 - SW Compatibility: VxWorks, Linux, RTEMS
 - JTAG, Ethernet and SpaceWire debug links with GRMON and TSIM3 capabilities
- State of the art Radiation Tolerant, Low Power, High Performance FPGA used for IO and Memory expansion.
- Independent Rad Hard MCU to monitor Processor, FPGA, and board health as well as control resets, power sequencing and boot image selection.
 - Supports advanced upset and error mitigation strategies

Memory

Customize the SBC8 Memory Configuration to your specific needs with options of 512MB or 1GB of FPGA connected MRAM and the option to include 171GB of NAND Flash with BCH EDAC.

- 512MB of EDAC Corrected SDRAM
- 128KB SEU Immune MRAM (Processor Boot Memory)
- 256MB QSPI MRAM with ECC (FPGA Boot and App Storage)
- 512MB or 1GB of High Speed, Non-Volatile, 32-bit Parallel MRAM with ECC accessible over PCI from the CPU
- Up to 171GB of ECC Corrected User Accessible Non-Volatile Memory (NAND)

Front Panel Interfaces

The SBC8 Front Panel offers options of SpW, Ethernet, UART, or CAN interfaces for communications to the Spacecraft Bus and other devices as well as PPS and GPS clock inputs for mission synchronization.

- 2x SpW
- 3x 10/100/1000Base-T Ethernet Ports

- 2x FPGA connected with 1 that also operates as an Ethernet Debug Port
- 1x CPU connected (user + debug)

- 2x RS-422 UARTs
- 2x CAN
- PPS Input (RS-422)

Backplane Panel Interfaces

SBC8 is primarily targeted for use as a System Controller, so it adheres to a SpaceVPX Controller Backplane profile, but can be used as peripheral with all the available Backplane IO.

- 8x SpW
- 4 lanes multi-purpose SERDES (6.25Gbps)
- 2 lanes of SGMII SERDES
- 8x I2C for IPMB
- 8x Slot Resets for other boards in the chassis
- 4x PPS Outputs
- 4x 100MHz Sync Clk Outputs (can come from on board clock or GPS Reference clock implemented on a Mezzanine)
- PCIe 100MHz Clk Output
- SpaceVPX Controller (Slot Profile: SLT3-CON-8T-14.6.2 Module Profile: MOD3-CON-8T8U-16.6.2-1-16.12)
- 12V Power Input (with optional 3.3V Aux usage)

Mezzanine Interfaces

A distinguishing feature of the SBC8 is its ability to adapt to your specific mission via custom mezzanines. Gone are the days of needing new SBC designs for every mission. Instead, maintain the same base SBC allowing maximum reuse of your investment in software and add features you need to make the next mission a success.

- PCI
- 4 lanes multi-purpose SERDES (6.25Gbps)
- SpW (can also be used as 4x LVDS GPIO or 8 SE GPIO)
- 1x GR740 GPIO
- PPS to/from Mez
- 4x Differential 100MHz Sync Clk from Mez + 1x Differential from Mez to Clock Network Manager
- 50MHz, 100MHz and 125MHz Clocks to Mez
- Mezzanine JTAG (to program FPGAs on Mez) – can be used as GPIO

Software & Firmware

The SBC8 SBC is delivered with a fully tested FPGA firmware package enabling the customer choice of interfaces from those available. Source Code along with the Gaisler GRLIB IP Core Library is available. (See Ordering Options)

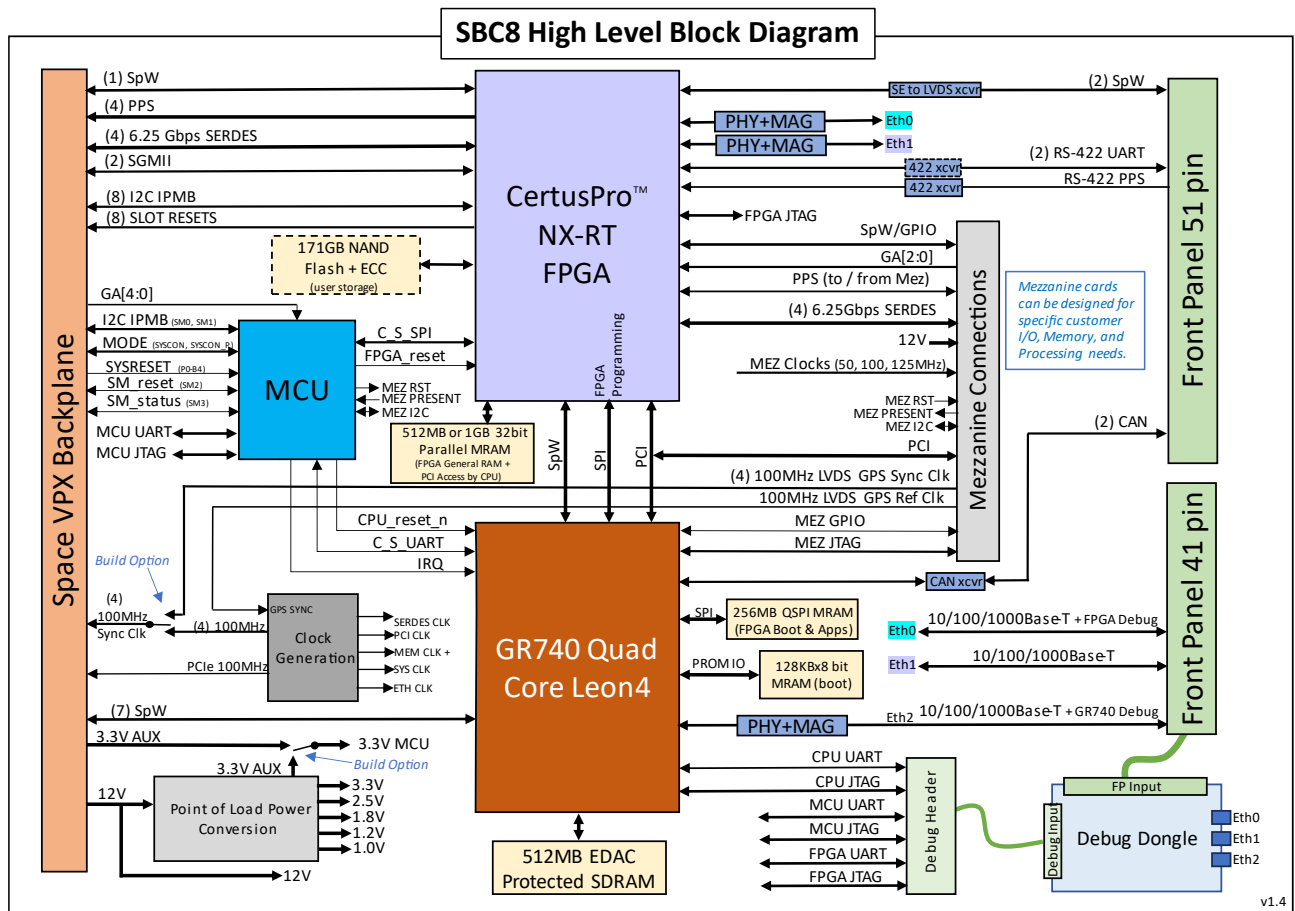
SBC8 can also delivered with a GRBOOT SBC8 BSP, VxWorks BSP, Linux SBC8 BSP, and/or a Demonstration Application based on RTEMS generic, and a User's Manual.

Developers will also have SBC8 support in the FG Gaisler TSIM3 and GRMON development tools.

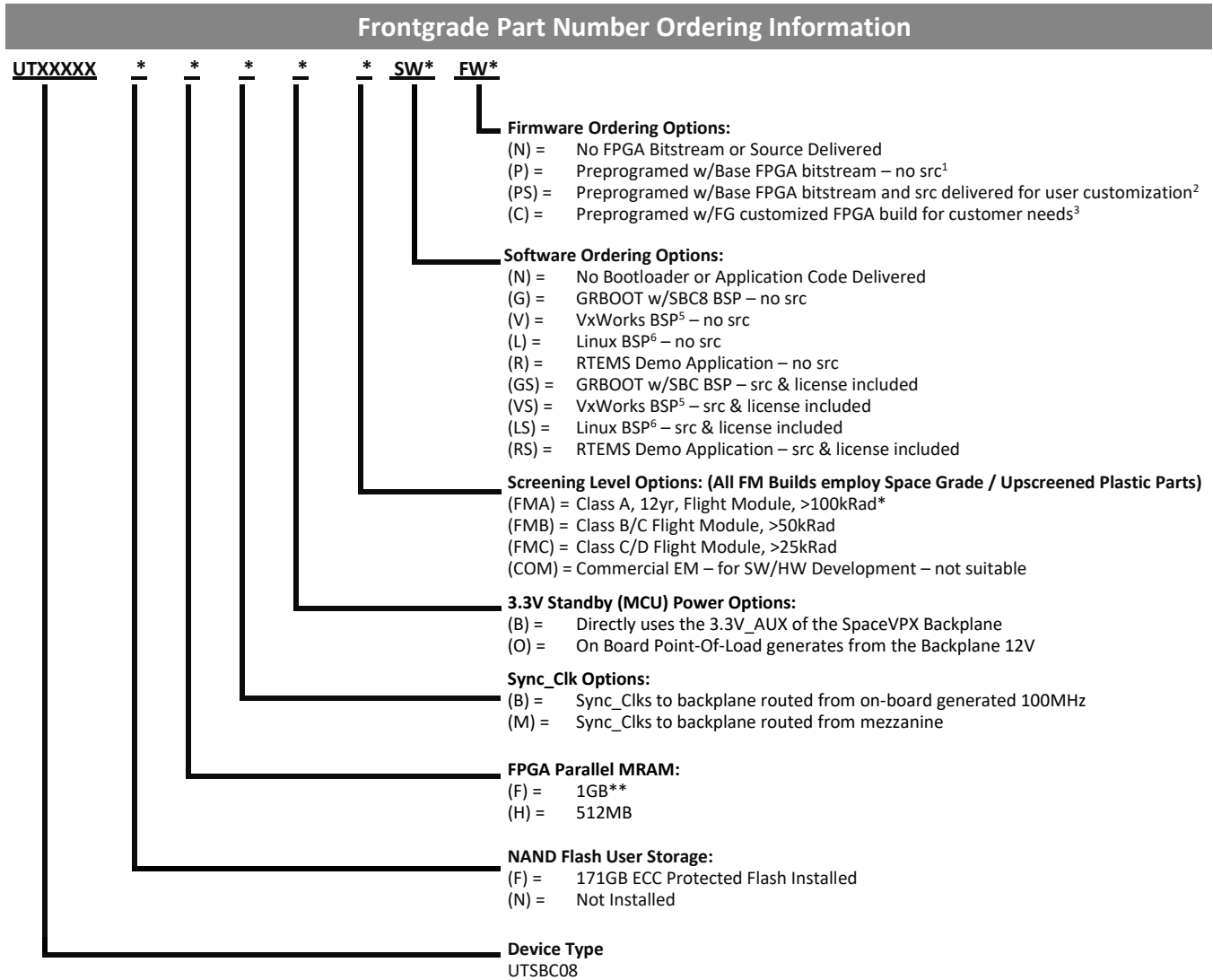
Mass & Thermal

- Mass: <0.65kg, standard 3U VPX form factor
- -25°C to +65°C operational
- Power consumption: 12.8W Typical

Block Diagram



Example Ordering Information (Not yet approved part numbering)



* Not currently a standard offering, but a custom version based on SBC8 can be created if needed by your project.

** Initial release will have 512MB until the 1GB MRAM has completed Qualification (expected April 2025)

1. Base FPGA Bitstream is designed to allow GR740 access to all ports, memories, etc
2. For user to make changes to the src code, they will need to separately purchase licensing for the GRLIB IP used or develop their own in its place
3. Frontgrade will bid the NRE and per board royalty cost of custom FPGA code in a separate quote in response to a RFP
4. User needs to purchase a separate source license from WindRiver for VxWorks, the SW delivery includes the architectural port (BSP) for VxWorks
5. Linux Distribution not included

Revision History

Date	Revision #	Author	Change Description	Page #
12/29/23	1.0.0	CPM	Initial DRAFT for Internal Review	All
01/09/24	1.0.1	CPM	Updates from reviews of 12/29 version – out for wider audience review	All
1/16/24	1.0.2	CPM	Update from 1/9 draft reviews - Initial Draft for Release	All
2/09/24	1.0.3	CPM	Remove NDA note from footer	All
2/20/24	1.1.0	CPM	Update to new format	All
3/27/24	1.1.1	CPM	Fix typo removing “dual in line” from Ordering info of FMB & FMC	All
4/2/24	1.2.0	CPM	Updates for latest design status R8 Schematic	All
4/3/24	1.2.1	CPM	Update BP Interfaces list to match block diagram	All
5/6/24	1.2.2	CPM	Update Export Control Message	6
5/28/24	1.3.0	CPM	Update Block Diagram and write-ups for latest design, Build Options Update	All
6/20/24	1.3.1	CPM	Update wording for memory configuration in Introduction	2
8/23/24	1.3.2	TLM	Sheet 1, added notional image of SBC8 Sheets 3,4, reformatted feature set summary Sheet 5, added clarification to indicate ordering information an “Example” and should not be treated as official at this time. Sheet 6, Removed Export Controlled statement pursuant to Global Trade Compliance content review and approval and added new unlimited distribution statement.	1, 3, 4, 5, 6

Datasheet Definitions

	Definition
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